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A 14-b Two-step Inverter-based $\Sigma\Delta$ ADC for CMOS Image Sensor

Pierre Bisiaux · Caroline Lelandais-Perrault · Anthony Kolar · Filipe Vinci Dos Santos · Philippe Benabes

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Abstract This paper presents a 14-bit Incremental Sigma Delta analog-to-digital converter suitable for column wise integration in a CMOS image sensor. A two step conversion is performed to improve the conversion speed. As the same $\Sigma\Delta$ modulator is used for both steps, the overall complexity is reduced. Furthermore, the use of inverter-based amplifiers instead of operational transconductance amplifier facilitates the integration within the column pitch and decreases power consumption. MonteCarlo simulations have been done in order to validate the design of the inverter. The proposed ADC is designed in 0.18 μm CMOS technology. The simulation shows that for a 1.8 V voltage supply, a 20 MHz clock frequency and an oversampling ratio (OSR) of 70, the power consumption is 460 μW, achieving an SNDR of 85.4 dB.

Keywords ADC · incremental · sigma-delta · CMOS Image Sensor · column-parallel · inverter-based

1 Introduction

High quality CMOS imaging sensor (CIS) arrays are reaching performance levels close to scientific CCD arrays. Frame rate and pixel pitch have increased, while read-out noise level has quickly dropped. These developments are considerably raising the requirements on the analog-to-digital converter (ADC) necessarily present in the image processing chain. Several improvements have been tried and developments in this field have arguably converged to column parallel ADC converter arrays, because this configuration has been shown to yield the best tradeoff among pitch, conversion rate, conversion resolution and power consumption.

Fitting the ADC in the ever narrower pixel pitch has driven the converter architectures from straightforward cyclic towards successive approximation register and single slope converters. The latter converters are widely used because of their simplicity and low power consumption. However, they are slow, and it's difficult to achieve more than 10-bit resolution. To raise the resolution above this, the trend is to move towards hybrid converters, where two kinds of converters work in tandem.

Conceptually, the conversion is done in two steps: first the most significant bits (MSBs) are extracted generating an analog residue. In the second step, this residue is converted by the second stage and the least significant bits (LSBs) are obtained. In the Nyquist converters, the analog residue in intermediate steps is proportional to the original analog input. In oversampling converters, such as Sigma-Delta ($\Sigma\Delta$) ADCs, the residue at every step is proportional to the integral of an error signal. In imaging sensor applications, one uses incremental $\Sigma\Delta$ (I$\Sigma\Delta$) ADCs, where the integrators are reset before each conversion. I$\Sigma\Delta$ converters are able to achieve very high resolution while using simple circuits that can be easily scaled down.

For example, Seo *et al.*[9] have developed a 17-bit I$\Sigma\Delta$ + cyclic ADC, and Shin *et al.* [10] introduced a 14.3-bits I$\Sigma\Delta$+SAR ADC, both focusing imaging systems. However, these architectures still require moderately complex circuitry due to the use of Nyquist converters in one of the steps. The works reported in Oike et al.[8] and Chen *et al.*[3] have pushed the concept further by using I$\Sigma\Delta$ ADCs for both steps. The overall OSR is then decreased compared to a

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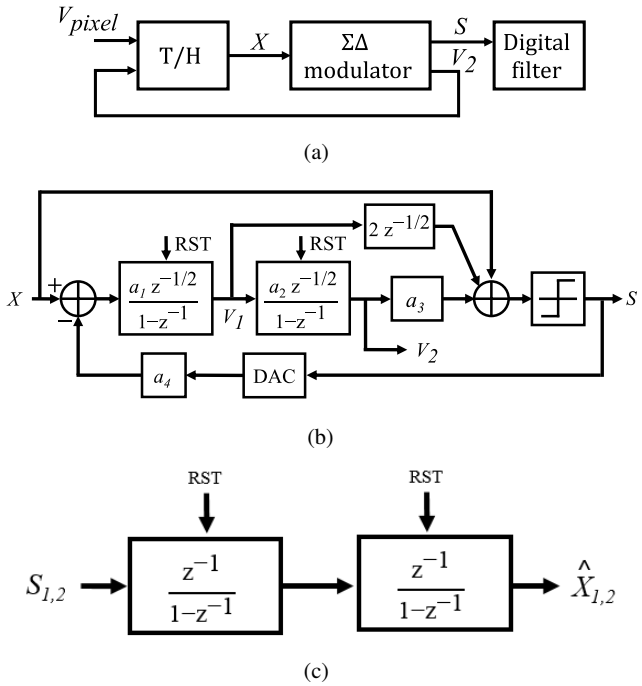


Fig. 1 (a) High-level view of two-steps architecture, schematic of the track and hold, (b) I$\Sigma\Delta$ second order modulator with feed-forward and (c) schematic of the digital filter of the ADC

standard I$\Sigma\Delta$ ADC and the implementation of the hybrid ADC takes less area and power. A further improvement of I$\Sigma\Delta$ ADCs was the use of inverters to implement the integrator of the $\Sigma\Delta$ loop, as reported by Chae *et al.*[2], as well as Wang *et al.*[13] and Tang *et al.*[12]. However, ensuring a high DC gain over an appreciable output voltage range is a challenging task. Still, the key advantage of inverter-based I$\Sigma\Delta$ ADC is the reduction in area and power consumption.

In this paper, a 14-bit two-step inverter-based I$\Sigma\Delta$ using a second-order cascaded integrators feed-forward (CIFF) is introduced. The main contribution of our proposal is the reuse of a second-order modulator for both steps, in addition to the use of gain-boosted inverter-based integrators. *With the use on double-sided ADCs above and below pixel array, the required ADC width can be twice the pitch of the pixel, so up to 25 µm. The important specifications set on this ADC are the resolution and the sampling frequency. This sampling frequency, which is the ADC frequency conversion, must be at least 230 kS/s with a resolution of 14-bit. No requirements have been set at that moment on the power dissipation and the length of the ADC*

This paper is organized as follows; In section 2, the high-level I$\Sigma\Delta$ architecture is presented. In section 3, the circuit implementation of the ADC is shown. In section 4, results from simulations are shown and compared to similar work. Section 5 concludes this paper.

2 Proposed two-step ADC architecture

2.1 Two-step theory

The high-level view of the proposed ADC architecture is shown in fig.1(a). The architecture is composed with a track and hold (T/H), a $\Sigma\Delta$ modulator and a digital filter. The chosen modulator is a second-order CIFF architecture [6] shown in fig.1(b).

Our two-step I$\Sigma\Delta$ ADC first performs a coarse conversion of the pixel value stored in the T/H, giving an analog residue V_2 loaded into the T/H. Then a fine conversion is performed on this residue, using the same modulator. The residue of the coarse conversion can be expressed as follows,

$$V_2[M1] = a_1 a_2 \sum_{K=1}^{M_1-1} \sum_{i=1}^{K-1} (X[i] - a_4 S_1[i]) \tag{1}$$

with a_1 and a_2 coefficients in the modulator, M_1 the number of samples for the first step, X the input signal stored and held by the T/H at the start of the conversion and S_1 the bitstream of the coarse conversion. The fine conversion is then realized on this residue. The final reconstructed signal is then a linear combination of both bitstreams and it can be written as,

$$\hat{X} = K_1 \sum_{K=1}^{M_1-1} \sum_{i=1}^{K-1} S_1[i] + \frac{K_1 K_2}{a_1 a_2} \sum_{K=1}^{M_2-1} \sum_{i=1}^{K-1} S_2[i] \tag{2}$$

with,

$$K_i = \frac{2}{(M_i - 1)(M_i - 2)} \tag{3}$$

where i=1,2, M_2 is the number of samples for the second step, S_2 the bitstream of the fine conversion and K_i the coefficient associated with the coarse and fine conversion. To maximize the resolution, M_1 and M_2 must be equal[1]. We take $M_1 = M_2 = 35$ to reach the aimed resolution.

2.2 Modulator scaling

In a two-step ADC the difference between the output of the first step of the conversion ($V_2[M_1]$) and the effective input of the second step can highly deteriorate the overall resolution. To optimize this range difference , the I$\Sigma\Delta$ must be analyzed in the time domain instead of the frequency domain.

One can see from (1) that the residue depends on the modulator coefficients a_1, a_2 and a_4. They must be adjusted to maximize the residue range within the input range. This optimization must also guarantee a non-saturation of the amplifier and a tolerance to possible offsets. For this design, the amplifier input range is limited to 85% of the reference scale and integrators levels do not go above 90% of

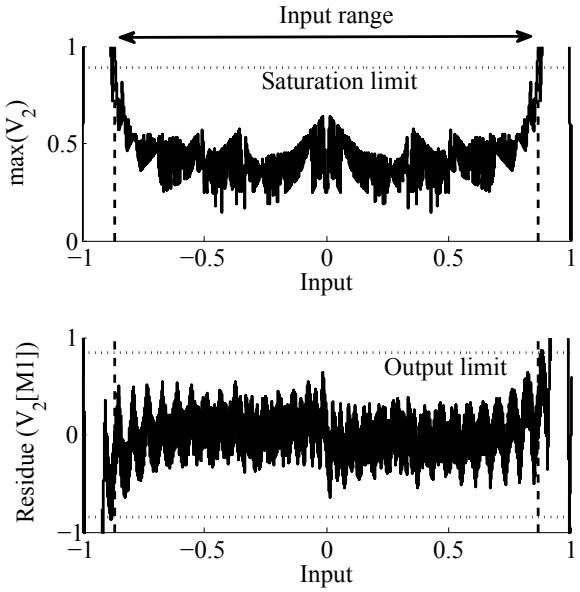


Fig. 2 Maximum of second integrator level (top) and residue values (bottom) with both axis scaled to $\Sigma\Delta$ reference level

the reference. The parameters a_1, a_2, a_3, a_4 were optimized by simulation and their values are respectively 0.5, 0.5, 0.75 and 0.5. With this set of parameters, the simulation of the maximum integrator value and the residue value are respectively shown in fig.2. In both results, values do not exceed the saturation or output limit for any input. The residue range is about 75% of the input range of the modulator. Since the saturation of the amplifier is avoided and the residue range fits the input range of this modulator, this architecture is suitable for a two-step ADC.

As one can see in the eq.(2), the value of the estimated signal depends on the true value of coefficients a_1 and a_2. In the next calculation, we do not consider the gain of the S/H, but the method remains the same. The circuit being implemented with a switched-capacitors (SC) circuit, the value of these coefficients depends of the technology. Using (2), one can find for the input signal X the exact equation of the input converter as

$$X = K_1 \sum_{K=1}^{M_1-1}\sum_{i=1}^{K-1} S_1[i] + \frac{K_1K_2}{a_1a_2}\sum_{K=1}^{M_2-1}\sum_{i=1}^{K-1} S_2[i] + \frac{K_1K_2}{(a_1a_2)^2}V_2[M_2] \quad (4)$$

where the last term, proportional to the residue of the second step, provides the accuracy of the ideal ADC. Now one can look at the difference between X and $\hat{X}$, E_{RR}, from the (2) and (4) and can be expressed as

$$E_{RR} = \left[K_1K_2\sum_{K=1}^{M_2-1}\sum_{i=1}^{K-1} S_2[i]\right]\left[\frac{1}{a_{1I}-a_{2I}} - \frac{1}{a_{1R}-a_{2R}}\right] - \frac{K_1K_2}{(a_1a_2)^2}V_2[M_2] \quad (5)$$

where a_{1I}, a_{2I}, a_{1R} and a_{2R} respectively represent the ideal and real coefficients. The error at the end of the conversion is due to neglecting the last residue $V_2[M_2]$ and the mismatch of the coefficients a_1 and a_2. These values in the switched capacitor must be known precisely, otherwise an extra calibration is needed to reach the full resolution. The variation of these coefficients can be reduced in its implementation with an suitable capacitance matching.

2.3 Digital Filter

As a reset occurs at each conversion, the digital filter of the IΣΔ is different from the classic ΣΔ. For a two-step IΣΔ with feed-forward in the modulator, in order to recover the input signal from the bitstream, the digital filter is similar to the discrete time filter. The digital filter used is shown in the fig.1(c). The ADC being a IΣΔ, a reset is also done on the digital filter at the beginning of each conversion. As for the analog modulator, each digital sample is integrated twice and a weighted summation of the estimated value is then performed. Multipliers must be added to perform the weighting operation on each bits of the bitstream

3 Circuit implementation

The T/H and the switched capacitor schematics of the modulator are shown in fig.3(a) and fig.4 respectfully. In both circuits, amplifiers have been designed with CMOS inverters to reduce area. For each ratio of cacitance, the capacitance value are multiple of an unitary capacitance. The value of 150 fF for C_S was chosen considering the technology (0.18um), the noise kT/C and the requirement for the Gain Bandwidth (GBW).

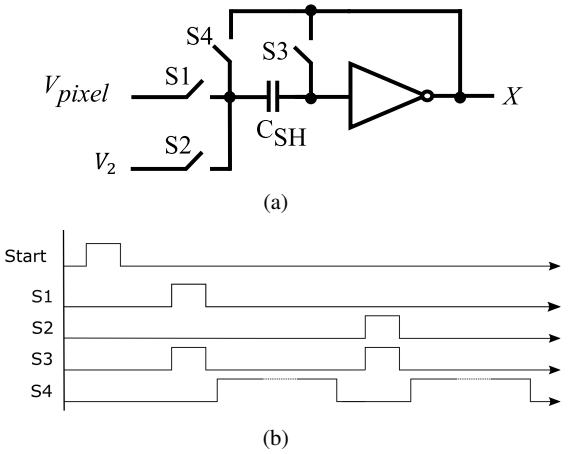


Fig. 3 (a) Schematic of the T/H stage and (b) Timing control of the S/H switches

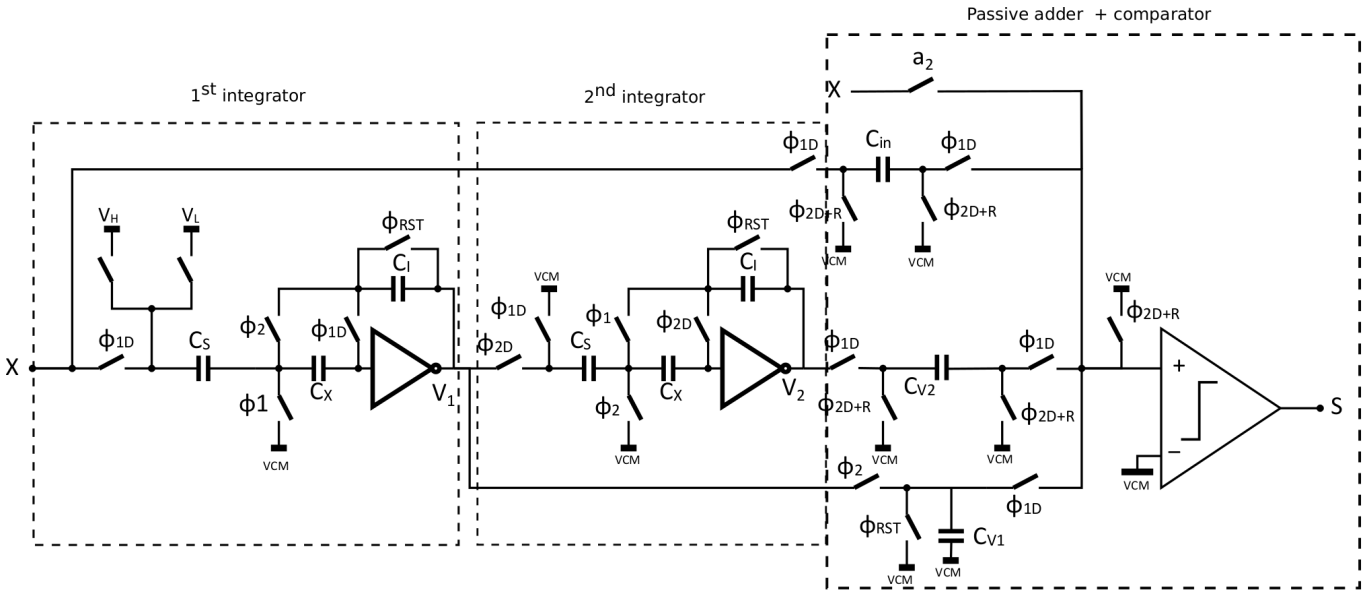


Fig. 4 Switched capacitor implementation of the 2^{nd} order modulator

Since inverter amplifiers have very large offset variation due to the process, we use an auto-zeroing scheme proposed in [2] for the $\Sigma\Delta$ modulator integration scheme.

A similar method is applied to the T/H and is shown in fig.3(b). Before the beginning of the coarse conversion, the pixel value is loaded into the capacitance C_{SH} (switches S1 and S3 closed, S2 and S4 opened). Then the value of the pixel is disconnected from the amplifier (S1 and S3 being open). Then S4 is closed and S3 opened, canceling the offset of the amplifier and storing the pixel value at the end of the operation. To load the residue $V_2[M_1]$ into the T/H at the end of the coarse conversion, the switch sequence is the same except that S2 is closed instead of S1 to select the right input. The SC implementation of the I$\Sigma\Delta$ modulator is reset between the first and the second step, and only the residue is held in the SC T/H stage.

3.1 Passive adder and comparator

The remaining circuit block required for the implementation of the modulator is passive adder filtered by a low-power, fast, clocked comparator [7]. The schematic of this comparator is shown in fig.5. In a I$\Sigma\Delta$ ADC, the comparator offset only impacts the input dynamic range of the modulator.*The input transistors (M1 and M2) are the most important to define comparator specifications as offset and decision time. To meet our requirements for these specifications, a good compromise is to set the input transistors size to (W/L)=(4µm/1µm).*

One can see in the fig.6 that the value of the offset goes from -12 to 8 mV with a mean value of -2 mV and a standard deviation of 4.5 mV. In order to be fast enough, the comparator must make its decision in less than 3 ns, considering the non-overlapping block. For two inputs values very close, which is the worst case possible in terms of speed, one can see in the fig.6 that the decision time of the comparator is up to 2.5 ns. This value is less than the required speed/offset, validating the comparator architecture.

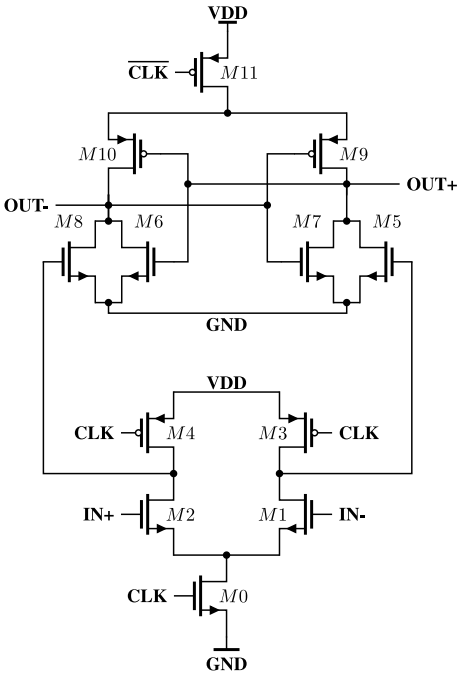


Fig. 5 Schematic of the double tail comparator

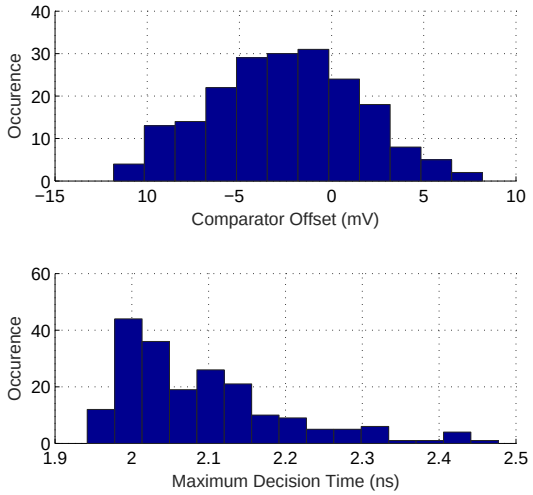


Fig. 6 MonteCarlo simulations of offset and decision time of the schematic comparator

Table 1 Inverter transistor size

Transistor	(W/L)
M1	20 μ / 0.36 μ
M2	5 μ / 0.36 μ
M3	30 μ / 0.36 μ
M4	7.5 μ / 0.36 μ
M5	8 μ / 0.36 μ
M6	2 μ / 0.36 μ

3.2 Inverter amplifier

It has been shown [1] that the amplifier gain needed to reach 14-bit resolution with this type of modulator is at least 80 dB. The small signal DC gain of an inverter is expressed as follows

$$A_v = (g_{m(N)} + g_{m(P)})(r_{o(N)} // r_{o(P)}) \quad (6)$$

where $g_{m(N)}$ and $g_{m(P)}$ represent the transconductance of NMOS and PMOS respectively, $r_{o(N)}$ and $r_{o(P)}$ their output resistance. From eq.(6) one can see that the gain can be increased with $r_{o(N,P)}$. Cascoding is a common way to raise the output resistance. However simple and cascoded inverters cannot reach a sufficiently high gain in this technology. Our solution is to add gain-boosting to the inverter[5]. The schematic of a gain-boosted inverter is shown in fig.7.

Thanks to the gain boosting amplifier circuit, the effective transconductance of the cascode transistor is increased, hence considerably increasing the output resistance of the inverter-based amplifier. A trade-off has to be found between the maximum DC gain and output linearity. To ensure good

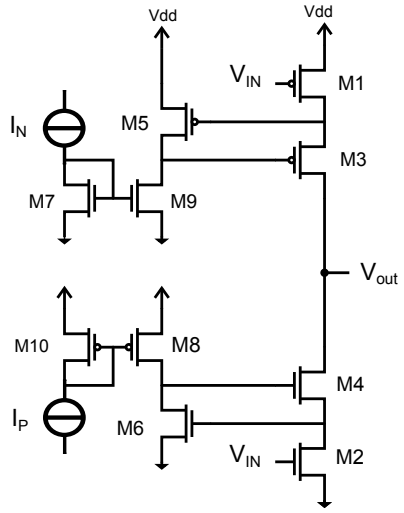


Fig. 7 Gain boosted inverter amplifier

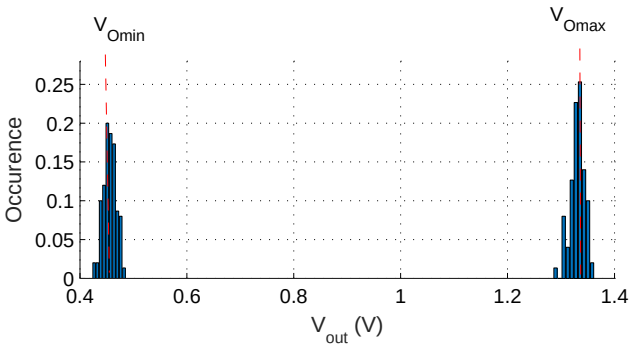


Fig. 8 Montecarlo simulation of the dynamic output range where a DC gain of 80 dB is ensured. V_{Omax} and V_{Omin} are normally distributed around the nominal values

output linearity swing, low-threshold transistor are used in the gain-boosting module (M5 and M6). *Moreover the PMOS transistor are sized larger than the NMOS to improve the symmetrical output range. The inverter transistor size are shown in the table 1.*

The inverter can be seen as a current source during the transient phase of the charge transfer, or as a voltage source in DC mode, when all the charges have been transferred. The second case is investigated in this section. The output linearity swing is the output range of the amplifier where a minimum DC gain of 80 dB is ensured[1]. A monte-carlo analysis of the inverter is realized and the output linearity is observed. The gain-boosted inverter amplifiers were sized to achieve a small signal gain of at least 80 dB with symetrical headroom of around 0.45 V from both supply rails. Monte carlo simulations were then ran to check how far the linear output range would change for the 10 μm pitch layout. The spread of the upper (V_{Omax}) and the lower (V_{Omin}) are given in the fig.8. The worst case value (0.5-1.3 V) are sufficient for our requirements.

Table 2 Inverter amplifier characteristics over different corner and the temperature

Case	V_{Omin} (V)	V_{Omax} (V)	ΔV_O (V)	GBW (MHz)
Typical	0.419	1.375	0.96	328
ws25	0.438	1.377	0.94	266
wp25	0.394	1.357	0.96	397
ws-20	0.458	1.361	0.90	228
wp-20	0.388	1.395	1.00	455
ws85	0.438	1.362	0.92	240
wp85	0.451	1.173	0.72	232

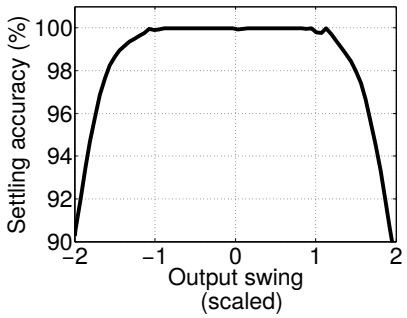


Fig. 9 Settling accuracy of an integration step

Considering the temperature dependencies of the amplifier over the different corners, the output linearity and the GBW were also obtained by simulations and the results are shown in Table.2. The different cases *ws* and *wp* represent respectively the worst speed and the worst power scenario for three different temperatures (25, -20 and 85 °C). One can see that all the cases are good with regard to the linearity and the GBW, except the case *"wp85"*, in which the gain-boosting circuit does not ensure enough feedback. The remaining issue in a low-voltage switched-capacitor circuit is the choice of switches, which influences the settling time of the voltages on the capacitors. With the designed switches, the settling accuracy of a transition from the voltage common mode to the extreme value is shown in fig.9. The X-axis, the output swing, is scaled to the $\Sigma\Delta$ reference. From this figure, one can observe that an accuracy of 99.9% is guaranteed for an output swing of 95% of the I$\Sigma\Delta$ reference.

4 Results

The proposed two-step inverted based ADC full transistor level was simulated in 0.18 μm technology. The supply voltage of the circuit is 1.8 V. The static current for a gain-boosting module is about 4 μW and 140 μW for an amplifier. With a main clock of 20 MHz and an overall OSR of 70,

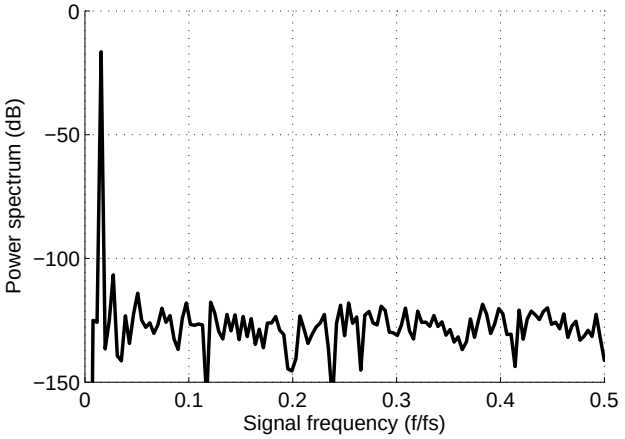


Fig. 10 Simulated output spectrum of I$\Sigma\Delta$ ADC with a 256 points FFT

the conversion is performed in less than 4 μs, so its sampling rate is up to 250 kS/s.

4.1 Schematic simulation results

Output spectrum is presented in fig.10 with an input signal frequency of 5 kHz and a 256 points FFT. This work achieves a SNR of 85.4 dB. The figure-of-merit (FoM) is written as follows,

$$FoM = \frac{P}{2^{ENOB}.Fs} \tag{7}$$

with P the power dissipation of the ADC, *ENOB* the effective number of bits calculated from the SNR, and F_s the sampling frequency of the ADC. This ADC achieves a FoM of 150 fJ/step. A comparison with similar works is shown in Table 3. This work consumes lower power and is very competitive compared to previous results. Its layout size is 25 μm $\times$ 240μm and is be suitable for a 12.5 μm pixel pitch when using double-sided ADC.

4.2 Post-layout simulation results

The post-layout simulation are used to determine the efficiency of a calibration on this ADC and the results are shown in fig.11. In this part, results are found by using a ramp at the input of the ADC. In fig.11.top, when applying a 140 points ramp within 75% of the input range, a resolution of 12-bit is achieved. Then a calibration is realized on every output bits with an offset using the least square method. Then a new conversion error is calculted with the calculated coefficients and the result is shown in fig.11.bottom. The green dots represents the points used for the calibration. The red points are random points, not used in the calibration, one can see that the resolution of the ADC almost reachs 14-bit.

Table 3 Performance comparison

	[9]	[11]	[4]	[8]	This work
Technology (μm)	0.18	0.35	0.18	0.15	0.18
ADC architecture	$\Sigma\Delta$+Cyclic	$\Sigma\Delta$+SAR	$\Sigma\Delta$+Cyclic	2 step $\Sigma\Delta$	2 step $\Sigma\Delta$
Sampling rate (kS/s)	30	150	50	-	**200**
Resolution	17	14.3	10.2	12	**14**
Power (μW)	345	300	13	363	460
DNL (LSB)	-0.88/1.38	-0.79/0.97	-	-0.7/1.8	-
INL (LSB)	-26.3/35	-1.7/2.79	-	-22/20	-
SNDR (dB)	85	-	63	-	85.4
FoM (fJ/step)	790	100	220	-	150

5 Conclusion

A two-step inverter-based I$\Sigma\Delta$ ADC is presented in this paper. The $\Sigma\Delta$ modulator is first analyzed. Then the circuit implementation of the T/H and the $\Sigma\Delta$ inverter-based modulator is analyzed. Finally simulations results are presented. This work had shown that hardware reuse can be realized for ADC in CMOS image Sensor. This point allow to decrease the overall size of the ADC and this architecture is a good trade-off for medium speed (250 kS/s) and high resolution (14-bit) ADC. We show that using a supply voltage of 1.8 V, a clock frequency of 20 MHz, a total OSR of 70, this schematic ADC achieves a SNR of 85.4 dB for a power consumption of 460 μW. The FoM of the ADC is 129 fJ/step. Future work is to send the chip to be made and also realize an embedded calibration for the ADC.

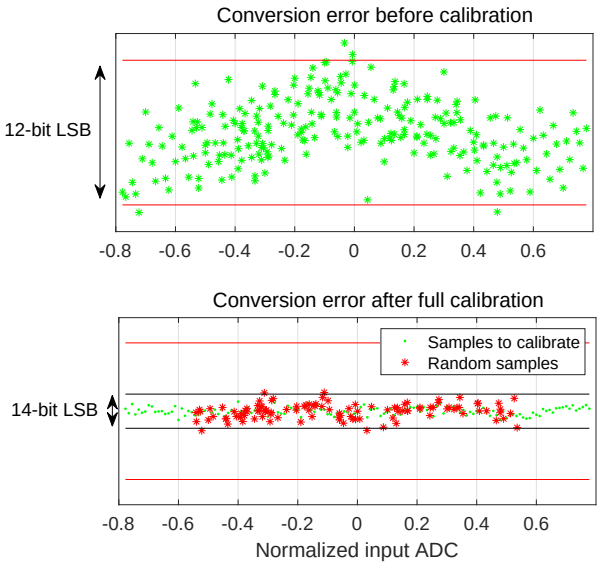


Fig. 11 Calibration of Post-layout simulations

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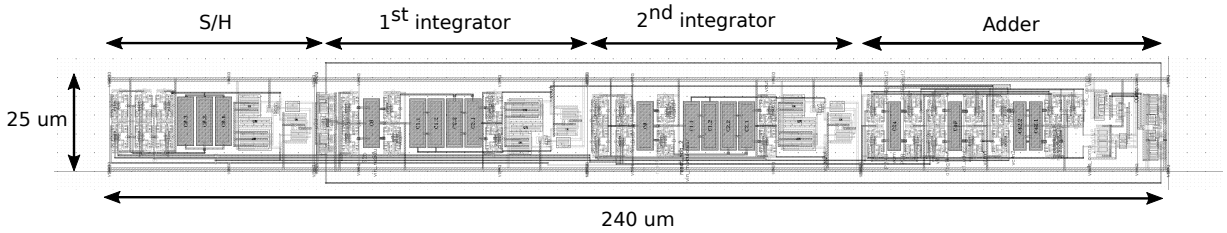


Fig. 12 Layout of the ADC

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