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Integrated waveguide PIN photodiodes exploiting lateral Si/Ge/Si heterojunction

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Abstract: Germanium photodetectors are considered to be mature components in the silicon photonics device library. They are critical for applications in sensing, communications, or optical interconnects. In this work, we report on design, fabrication, and experimental demonstration of an integrated waveguide PIN photodiode architecture that calls upon lateral double Silicon/Germanium/Silicon (Si/Ge/Si) heterojunctions. This photodiode configuration takes advantage of the compatibility with contact process steps of silicon modulators, yielding reduced fabrication complexity for transmitters and offering high-performance optical characteristics, viable for high-speed and efficient operation near 1.55 μm wavelengths. More specifically, we experimentally obtained at a reverse voltage of 1V a dark current lower than 10 nA, a responsivity higher than 1.1 A/W, and a 3 dB opto-electrical cut-off frequency over 50 GHz. The combined benefits of decreased process complexity and high-performance device operation pave the way towards attractive integration strategies to deploy cost-effective photonic transceivers on silicon-on-insulator substrates.

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1. Introduction

Group IV photonics is a promising on-chip technology, mostly relying on the silicon-on-insulator (SOI) platform, for broad ranges of optical applications such as optical communications, interconnects, and sensing [1–4]. Essential components in integrated photonic circuits are optical photodiodes to monitor light intensity variations or enabling high-speed detection of optical signals [5]. Photodiodes implemented directly on silicon (Si) substrates are desirable to leverage the benefits offered by the SOI technology. This includes compatibility with silicon (Si) microelectronics facilities, chip-scale device miniaturization and large-scale integration. However, an inherent shortcoming of the SOI platform is the inability of Si to absorb light at wavelengths beyond 1.1 μm, in general, for practically important O- to U- optical communication bands (1.26-1.68 μm), in particular [1–5].

From that point of view, germanium (Ge), with a cut-off wavelength near ~1.8 μm, is an ideal candidate for on-chip photo-detection. The last decades have seen tremendous developments in Ge-based waveguide photodetectors [5–19]. Despite the large lattice mismatch of Ge with Si (~4.2%), thin Ge films can be epitaxially grown on Si substrates. Ge photodetectors are nowadays considered as mature fundamental building blocks in the silicon photonic device library. They have attractive performance characteristics, readily comparable to those achieved by III-V semiconductors, commonly employed in optical telecommunication components.

Conventional Ge waveguide photodiodes, with vertical and lateral PIN junctions, call upon Ge doping and the deposition of metal contacts on Ge. However, the full Ge-based photodiode architectures suffer from significant losses, decreasing the device responsivity and requiring a specific technological process scheme for Ge [7–12]. A few research groups have reported on the fabrication of Ge waveguide photodetectors that avoid Ge doping and metal via-contact formation directly on Ge [13–15,18,19]. Improved photodiode performance characteristics were obtained, yielding enhanced bandwidth, high responsivity at telecom

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(1.55 μm) and at datacom (1.31 μm) wavelengths, and low dark currents [13–20]. Those performances are encouraging to handle demands in a variety of applications.

In this work, we report on the design, fabrication, and operation of a new Ge PIN waveguide photodiode that advantageously exploits lateral Silicon/Germanium/Silicon (Si/Ge/Si) heterojunctions. The use of this photodiode architecture benefits from (i) the improved optical confinement in the Ge layer, due to the larger refractive index difference between doped Si regions and the intrinsic Ge region, which in turn, yields a reduction of the optical loss in doped contacts, (ii) a better control of the photodiode geometry and (iii) an improvement of the photodiode responsivity. More specifically, we show that this Ge waveguide photodiode configuration yields enhanced performances in terms of speed and sensitivity. For experimentally characterized devices, we obtained low dark currents (well-below 10 nA at low voltage of −1 V), high photodiode responsivity (up to 1.16 A/W at 1550 nm at −1 V), and large −3 dB opto-electrical bandwidths (over 50 GHz). In addition, such a photodiode scheme offers substantial technological advantages such as a decrease in contact access resistance and improvements in opto-electronic device integration (providing substantial reduction in fabrication complexity and cost). Furthermore, the butt-coupling configuration used here allows the integration of hybrid photonic structures, as flat surfaces are still available after Ge photodetector fabrication.

2. Device design and fabrication

Figure 1(a) shows schematic of the Ge waveguide PIN photodiode that exploits the lateral double Si/Ge/Si heterojunction. In this work, the intrinsic region of Ge is sandwiched between P- and N-type doped Si regions, located at the end of a Si waveguide. Three-dimensional (3-D) Finite Difference Time Domain (FDTD) calculations were carried out using a commercially available simulation tool from Lumerical Solution, Inc. for a 1 μm wide and 10 μm long Ge cavity. As shown in Figs. 1(b) and 1(c), the optical power is efficiently coupled from the Si waveguide into the Ge area. In addition, the major portion of the optical power is sufficiently confined inside the Ge region, thereby avoiding the light absorption in doped contacts. The evolution of the fraction of optical powers inside the Ge region and P + + and N + + regions is shown in Fig. 1(d). More specifically, for a Ge width of 0.3 μm, the fraction of optical power inside this region is estimated to be 54.5%, while the fraction of optical power inside P + + and N + + regions is 31.8%. Conversely, with the increasing width of the Ge region, the optical field confinement of the proposed photodiode structure is enhanced, yielding a comparatively larger portion of optical power inside the Ge region, while the smaller portion of optical power belongs to side regions. In particular, for Ge width of 1 μm, this corresponds to the 86% of optical power, which stays inside the Ge region and only 8% of power is situated in the P + + and N + + regions. Furthermore, using the built-in Ge material properties, the 3-D FDTD calculations predict device responsivity of 0.63 A/W, for 10-μm-long devices. Hence, photodiodes with length of 5, 10, 20, and 40 μm were designed and processed. We used mature processes such as P + + and N + + ion implantation (used for the fabrication of optical modulators) or Ge selective epitaxial growth without any specific optimization to fabricate our devices.

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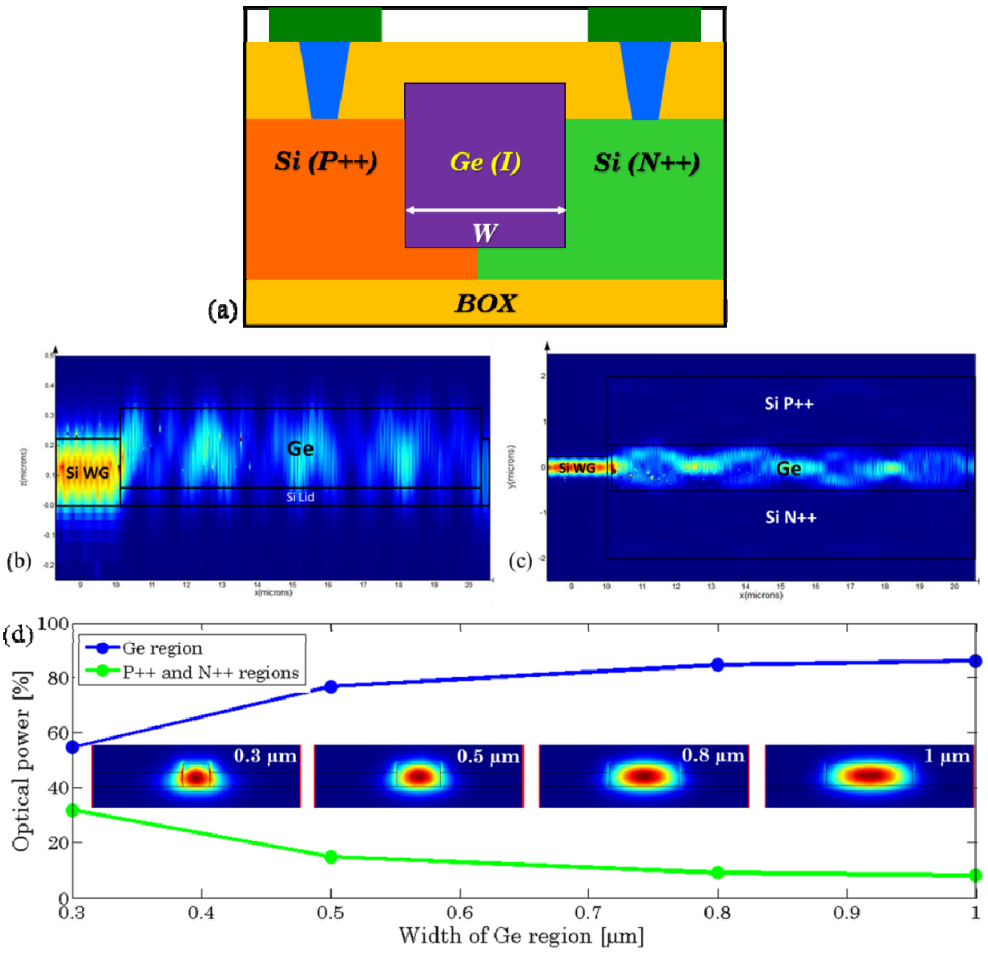


Fig. 1. (a) Schematic cross-section of the Ge waveguide PIN photodiode based on the lateral Si/Ge/Si heterojunction. (b) and (c) Vertical and top view color maps of the optical power in the Si waveguide and in the Si/Ge/Si photodetector obtained by 3-D FDTD simulations. (d) Evolution of optical powers inside the Ge region and P + +/N + + regions for different Ge widths. Inset: Mode profiles for different widths of Ge region.

The integrated Ge waveguide photodiodes were fabricated in LETI's cleanroom facilities, using 200 mm SOI wafers. The SOI substrates consisted in 220-nm-thick Si layers on top of 2-µm thick buried oxides (BOX). First, passive photonic components such as waveguides and surface grating couplers were fabricated using 193-nm deep-ultraviolet (deep-UV) optical lithography, followed by dry etching.

To facilitate the integration of Ge photodetectors into Si-based photonic circuits, we used a butt-coupling scheme with PIN junctions. In the butt-coupling scenario, the integration of Ge occurs at the end of Si waveguide, with a selective epitaxial growth of Ge in the etched Si cavity (surrounded by oxide and with a thin Si "seed" layer just above the BOX). The use of a butt-coupling approach and of PIN junction enables to contact the photodiode in single-etch step for P-type and N-type doped regions, and offers enhanced optical performances in terms of responsivity and spectral bandwidth, as discussed in Section 3. Using Si for photodiode contacts, we get rid, during the fabrication of optical interconnection of at least 7 fabrication steps, including photolithography steps, specific P-type and N-type ion implantation steps, stripping on Ge P-type and N-type doped regions, and an electrical activation annealing step. The same masking / ions implantation / stripping / annealing steps are indeed used for the

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fabrication of the Si-based optical modulators and the processing of the Si parts of our Si/Ge/Si photodetectors.

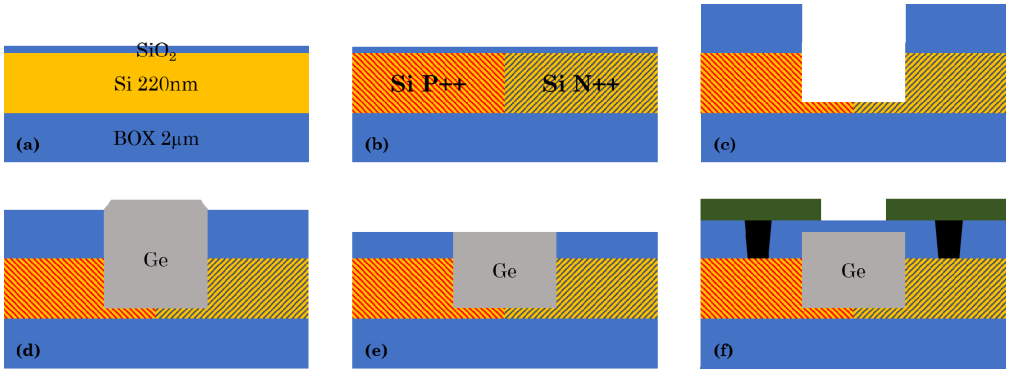


Fig. 2. Schematic illustration of the process flow used for the fabrication of our Ge waveguide photodiodes. (a) Starting wafer after passive device patterning and thermal oxidation. (b) Ion implantation in Si for photodiode contacts definition. (c) Etching of the cavity prior to the selective epitaxial growth of Ge. (d) Overflowing Ge after epitaxy and annealing. (d) Device after CMP. (f) Final device with W plug and AlCu electrodes.

The process flow used to fabricate this new flavor of waveguide Ge photodiodes is schematically shown in Figs. 2(a) - 2(f). After fabrication of passive devices, a thermal oxidation of about ~10 nm was used in order to have a cap layer prior to ion implantation [see Fig. 2(a)]. Si P-type and N-type regions were obtained by ion implantation of Boron (B) and Phosphorous (P), respectively [Fig. 2(b)]. Dopant concentrations in P- and N-regions were over 10^{19} at/cm^3, as for P + + and N + + contacts in Si modulators. A 800-nm-thick oxide layer was deposited prior to cavity patterning for the selective epitaxial growth of Ge. The upper oxide layer was fully etched down to the Si surface. The Si cavity is then etched, with around ~60 nm of Si remaining at the bottom of the cavity [Fig. 2(c)]. Then, a more than one micron thick Ge layer was selectively grown inside cavities, using a two-step Reduced Pressure - Chemical Vapor Deposition (RP-CVD) process, followed by 1 hour of annealing at 750°C to heal defects [Fig. 2(d)]. The process used has allowed the selective epitaxial growth of Ge in cavities as small as 300 nm x 5 µm. Then, Chemical Mechanical Polishing (CMP) was used to reduce the thickness of Ge layer down to ~260-nm and recover a flat surface prior to contact and metallization steps [Fig. 2(e)]. A top view image of a 1 µm wide Ge cavity is shown after CMP in Fig. 3(a). A thick oxide layer was then deposited for Ge passivation and insulation. 400 nm x 400 nm vias were subsequently patterned and etched down to the Si doped regions. In order to improve contact resistance, silicidation was performed. Ti/TiN/W stacks were used as metal plugs. The electrodes consisted in patterned AlCu layers. A schematic of the waveguide Ge photodiode is shown in Fig. 2(f) and a cross-sectional scanning electron microscopy (SEM) image of a 1 µm wide Ge cavity photodiode in Fig. 3(b).

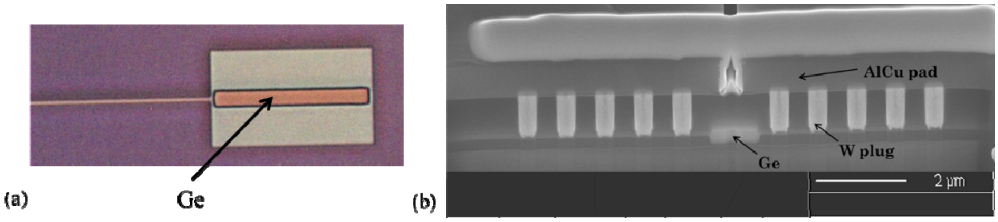


Fig. 3. (a) Top-view of a fabricated 1 µm wide Ge cavity after CMP. (b) Cross-sectional SEM image of a 1 µm wide Ge cavity photodiode.

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It is worth mentioning that, in comparison with previously reported conventional photodiodes [4, 7, 11], the intrinsic width of the Ge waveguide photodiode is solely defined by the width of the Ge cavity. Furthermore, the use of lateral Si/Ge/Si heterojunction yields a better optical confinement of the guided mode in the Ge layer compared to full Ge integration schemes. In other words, as doped regions are defined in Si, they have a refractive index close to that of Si (~3.47), which is lower than the refractive index of Ge. Indeed, due to the refractive index difference between Si and Ge, the incoming light coupled from the Si waveguide into the Ge region, stays confined in it and does not spread out in the doped regions, avoiding any deleterious absorption of photo-generated carriers in the later. This new integration scheme has important benefits: i.e. a reduction of the optical loss in doped contacts, a better control of the photodiode geometry (intrinsic width), and an improvement of the photodiode responsivity.

In addition, from a technological point of view, the lateral Si/Ge/Si heterojunction architecture also offers substantial advantages. In particular, it reduces the number of process steps used for device fabrication, making this Ge waveguide photodiode a promising candidate for cost-effective and large-volume deployment. Second, contact access resistances are reduced thanks to silicidation, which is used for other devices such as optical modulators.

3. Device characterization

We have carried out static optical measurements and radio-frequency measurements to quantify the benefits of using Si/Ge/Si waveguide photodetectors.

3.1 Current-voltage measurements

Typical current-voltage (I-V) characterizations were performed on Ge waveguide photodiodes. Under illumination, a photocurrent was generated by the device. Light coming from the tunable laser source was coupled via standard single-mode optical fiber (SMF-28) into the Si chip using surface grating couplers. The grating couplers were optimized for the in-plane transverse electrical (TE) polarization, at a wavelength of 1.55 µm.

Table 1. (a) Measured dark currents in nA for various widths and lengths of Si/Ge/Si PIN photodiodes under −1 V bias. (b) Measured mean dark current densities and standard deviations in A/cm^2 for various widths and lengths of Si/Ge/Si PIN photodiodes under −1 V bias.

(a) I_d **[nA] at −1 V**	W_{Ge} **= 0.3 µm**	W_{Ge} **= 0.5 µm**	W_{Ge} **= 0.8 µm**	W_{Ge} **= 1.0 µm**
L_{Ge} **= 5 µm**	8	-	8	6
L_{Ge} **= 10 µm**	13	6	16	18
L_{Ge} **= 20 µm**	56	27	24	74
L_{Ge} **= 40 µm**	-	63	55	207
(b)	W_{Ge} **= 0.3 µm**	W_{Ge} **= 0.5 µm**	W_{Ge} **= 0.8 µm**	W_{Ge} **= 1.0 µm**
Mean dark current density [A/cm^2]	0.731	0.452	0.555	1.142
Dark current density standard deviation [A/cm^2]	0.305	0.196	0.075	0.669

The measured dark current performances of all types of Ge photodiodes are summarized in Table 1(a), for a bias voltage of −1 V, while Table 1(b) provides measured mean dark current densities and the respective standard deviations. The dark current densities are obtained by normalizing the dark current by the cross section (width by height) of the photodiodes, thus eliminating the length of the photodiodes. Hence, we reported the mean dark current density obtained over a whole set of photodiodes with different lengths, but the same width, as well as the associated standard deviation.

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Conventional I-V curves of the dark current and photocurrent for Si/Ge/Si waveguide photodiodes are shown in Fig. 4(a), while Fig. 4(b) shows the evolution of the photodiode responsivity as a function of bias voltage for different lengths. The Ge width was 1 µm, while its length was equal to 5, 10, 20 and 40 µm.

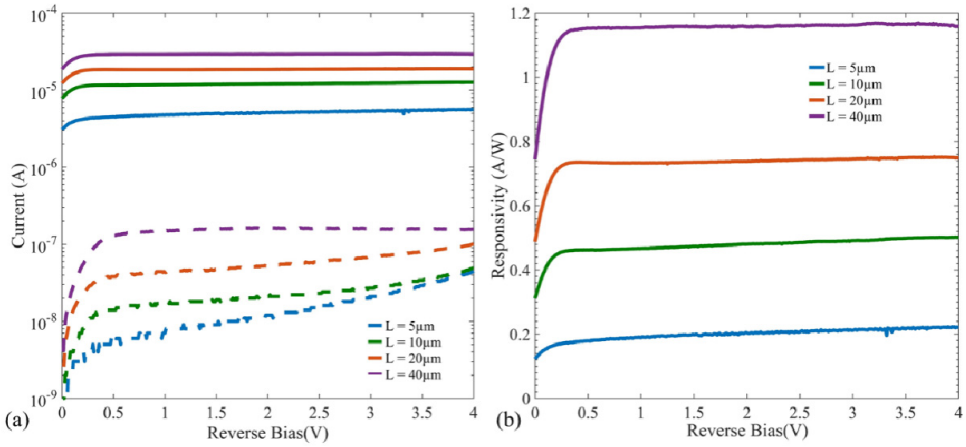


Fig. 4. (a) Measured current-voltage (I-V) characteristics under dark (dashed lines) and illuminated conditions (continuous line). (b) Evolution of the photodiode responsivity as a function of the bias voltage. The Ge waveguide photodiodes with lateral Si/Ge/Si heterojunctions have a Ge width of 1 µm and different device lengths (5, 10, 20, and 40 µm).

The measured devices exhibit very low dark currents, typically below 10 nA under −1 V for the shortest device configurations [see Table 1(a) and 1(b)]. The dark current increases monotonously with the length of the photodiode, while the evolution with the Ge width is less clear. The dominant contributions to the dark current are likely to be volumetric. The generated photocurrent was measured at a wavelength of 1550 nm, with an input received optical power of −16 dBm. The device showed a responsivity as high as 1.16 A/W at low bias voltage of −1 V for the widest and longest device arrangement (i.e. L_{Ge} = 40 µm and W_{Ge} = 1 µm). For L_{Ge} = 10 µm and W_{Ge} = 1 µm, the device responsivity was about 0.5 A/W. This value is lower than the expected one of 0.63A/W coming from 3D-FDTD simulation. We attribute the small discrepancy between measurements and FDTD predictions to the Ge absorption, which is probably smaller than that one considered for simulations.

From a practical point of view, this decrease may be a consequence of the 1 hour 750°C H_2 post-epitaxial annealing used to heal defects in the Ge layer. This might have induced a slight Si-Ge inter-diffusion, lowering the absorption of Ge. Nevertheless, the device responsivity reaches its maximum value at low bias voltage, (< 0.5 V), which is a prerequisite for low-power consumption operation. Since the maximum responsivity is achieved at low bias, this clearly indicates that all photo-generated carriers have been collected. From FDTD simulations, the expected values of responsivity in 0.3, 0.5, and 0.8 µm wide devices are about 0.35 A/W, 0.57 A/W and 0.66 A/W, respectively. In all cases, the device length was 10 µm. From simulations, it seemed that the 0.8 µm wide devices offered increased responsivity compared to wider devices (i.e. with 1 µm of Ge sandwiched between Si).

3.2 Cut-off frequency measurements

High speed measurements were performed using a classical RF experimental set-up. Light was coupled into the Si waveguides with grating couplers. The integrated Ge waveguide photodiodes were biased using 50 GHz probes. The generated photocurrent was measured using a Lightwave Component Analyzer (LCA), providing a frequency response in the 0.1 GHz to 50 GHz range.

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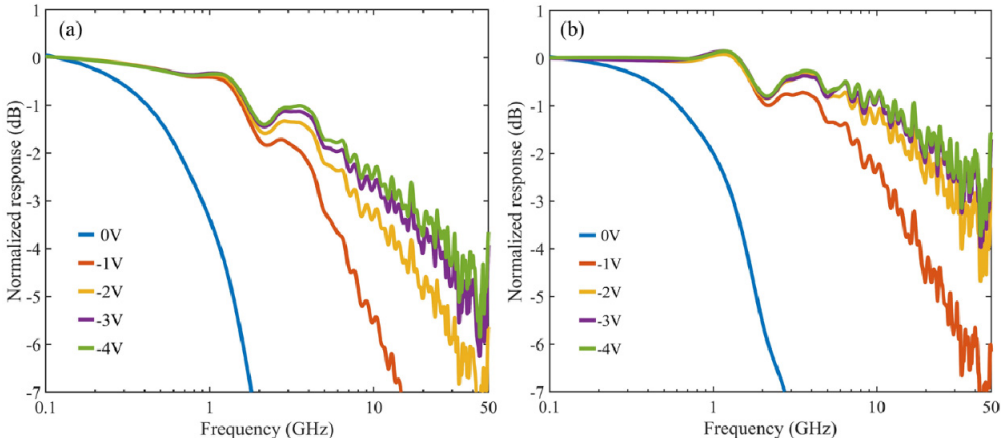


Fig. 5. Normalized frequency response obtained from LCA, for lateral Ge photodiode geometries (a) L_{Ge} = 40 µm; W_{Ge} = 1 µm and (b) L_{Ge} = 40 µm; W_{Ge} = 0.8 µm.

Figures 5(a) and 5(b) show frequency responses for the longest devices (i.e. L_{Ge} = 40 µm) under different reverse bias conditions (from 0 V to –4 V), for W_{Ge} = 1 µm and W_{Ge} = 0.8 µm, respectively. At 0 V, the –3 dB cut-off frequency are ~0.9 GHz and ~1.3 GHz, for W_{Ge} = 1 µm and W_{Ge} = 0.8 µm. Even for the smallest widths (i.e. W_{Ge} = 0.5 µm and W_{Ge} = 0.3 µm), the zero-bias bandwidth reached 3 GHz and 5 GHz, without any dependence on device length. These experimental behaviors are in good agreement with simulations.

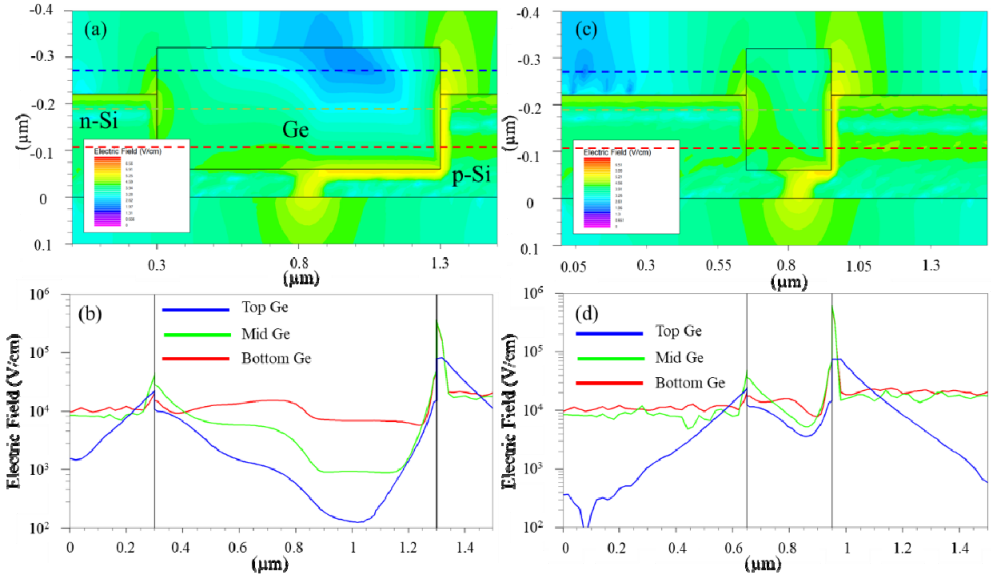


Fig. 6. Simulations of the built-in electric field under zero-bias (0 V) for devices with W_{Ge} = 1 µm [(a) and (b)] and W_{Ge} = 0.3 µm [(c) and (d)]. (b) and (d) correspond to the profile of the electric field along the cut-lines shown in (a) and (b), respectively.

Indeed, to better understand the device frequency response at 0 V, Technology Computer-Aided Design (TCAD) simulations (with inputs from a Silvaco ATHENA tool for ion implantation profiles) were performed together with ATLAS simulations to determine the electric field inside the diode. Simulations for the electric field are shown in Figs. 6(a) - 6(d).

Under zero bias, only the built-in electric field can extract photo-generated carriers. The wider the junction, the lower the electric field, and hence the lower the cut-off frequency.

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Previous works reported [11] that for Ge PIN homojunction photodiodes, zero-bias operation at high speed (~40 GHz) was possible. This was due to the single material configuration between the doped regions and intrinsic zone, and thus the absence of electric field and band gap energy discontinuities. However, in the Si/Ge/Si heterojunction case, as is the case here, there is a discontinuity of the electric field at the interface between the intrinsic Ge region and the Si doped regions. The built-in electric field is high at this interface (over 1.10^4 V/cm). It dropped by a factor equal to the permittivity ratio $\varepsilon_{Ge}/\varepsilon_{Si}$, ε_{Ge} and ε_{Si} being the relative permittivity of the Ge intrinsic region and doped Si regions, respectively [see Fig. 6]. Therefore, the zero-bias bandwidth remains low in every situation. Moreover, the top part of the Ge layer is not fully "sandwiched" between Si doped regions (the thickness of the Ge layer was ~260 nm, while the thickness of the Si doped regions was 220 nm). Whereas the electric field in the bottom part of the Ge layer is steady at around 1.10^4 V/cm [red curves in Figs. 6(b) and 6(d)], the electric field drops in the top part of the Ge layer [blue curves in Figs. 6(b) and 6(d)]. Photogenerated carriers are then unable to reach high drift velocity. This results in a significant degradation of the zero-bias frequency response of waveguide PIN photodiodes with a lateral Si/Ge/Si heterojunction.

Table 2. Summary of the –3 dB opto-electrical bandwidth in GHz extracted from frequency response measurements for the Ge layer lengths probed (L = 5, 10, 20, and 40 µm) under several reverse biases values in a range of 0 V to –4 V, and for different Ge widths (0.3, 0.5, 0.8, and 1 µm).

-3dB Bandwidth [GHz]		0 V	-1 V	-2 V	-3 V	-4 V
W_{Ge} = 0.3 µm	L_{Ge} = 5 µm	5.1	33	> 50	> 50	> 50
	L_{Ge} = 10 µm	5.1	34.7	> 50	> 50	> 50
	L_{Ge} = 20 µm	4.3	37.2	> 50	> 50	> 50
	L_{Ge} = 40 µm	-	-	-	-	-
W_{Ge} = 0.5 µm	L_{Ge} = 5 µm	2.3	18.4	36	> 50	> 50
	L_{Ge} = 10 µm	2	23.5	29.3	35.8	> 50
	L_{Ge} = 20 µm	3	35.6	42.8	> 50	> 50
	L_{Ge} = 40 µm	2.7	23.5	43	> 50	> 50
W_{Ge} = 0.8 µm	L_{Ge} = 5 µm	1.4	16	27	36	42
	L_{Ge} = 10 µm	1.2	6.3	15	19	24
	L_{Ge} = 20 µm	1.4	14.4	20.2	38.8	> 50
	L_{Ge} = 40 µm	1.3	13	32.8	38.1	> 50
W_{Ge} = 0.8 µm	L_{Ge} = 5 µm	1	2.1	4.5	5.2	-
	L_{Ge} = 10 µm	1	4.5	5.8	6.8	7.9
	L_{Ge} = 20 µm	0.9	5.6	9.3	12.5	15.1
	L_{Ge} = 40 µm	0.9	4.7	8	16.5	17.1

By contrast, under a reverse bias voltage of –1 V, a high electric field was present in the whole Ge layer and the cut-off frequency and responsivity definitely increased. A summary of the extracted –3 dB cut-off frequency is provided in Table 2. For Ge photodiodes with W_{Ge} = 1 µm, the bandwidth hardly reaches 18 GHz under a high voltage of –4 V, independently of the device length. This behavior is consistent with the device width, i.e. the frequency response of the device is limited by the carrier transit time.

A 50 GHz bandwidth was obtained by reducing the intrinsic Ge width. More specifically, this was achieved at low bias voltages of –2 V for W_{Ge} = 0.3 µm, –3 V for W_{Ge} = 0.5 µm and –4 V for W_{Ge} = 0.8 µm, respectively. Another interesting feature of the studied devices is that, even for long Ge layers, the frequency response does not seem to be limited by the RC delay. Indeed, devices with W_{Ge} = 0.5 µm had bandwidths above 50 GHz whatever the length was. However, our measurement set-up was limited to 50 GHz, thus restricting the device characterizations beyond this limit.

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4. Conclusion

In summary, we demonstrated the interest of using an improved Ge-based SOI waveguide PIN photodiode with a lateral Si/Ge/Si heterojunction, with doping and metal contacts in/on Si regions. This waveguide photodiode architecture takes full advantage of the implantation and contact process steps of Si modulators, which (i) results in a substantial simplification of the fabrication process of complex transceivers and (ii) yields high optical performances. In particular, via static optical and radio-frequency characterization, we obtained low dark currents (below 10 nA at −1 V), high device responsivities (over 1.1 A/W at 1550 nm and −1 V), and large −3 dB cut-off frequencies (over 50 GHz for the smallest Ge widths). This achievement opens the way towards advanced integration strategies for attractive and cost-effective photo-detection solutions in photonic transmitters and receivers on SOI substrates.

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