High-Performance Compact 3-D Solenoids for RF Applications

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***Abstract*—A cost-effective technology is proposed for the integration of very compact and high-performance 3-D solenoid inductors. Based on a two metal level process, it involves a 3-D copper electroplating step for simultaneous integration of vertical and upper sections of coils. Several solenoids fabricated on a glass substrate and ranging from 2.3 nH to 9.5 nH are presented. The best performance is experimentally achieved by a 3-turn 3 nH inductor showing a maximum Q-factor of 58 at 5.6 GHz and a self-resonant frequency of 19 GHz. The best inductance density of 63 $\mathrm{nH/mm^2}$ is reached by an 8-turn 9.5 nH solenoid.**

***Index Terms*—Integrated Passive Devices, Above-IC, solenoid, high-Q inductor, three-dimensional inductor, 3-D inductor.**

I. Introduction

THE integration of high-quality RF inductors remains a challenge, since the quite poor characteristics of these components are frequently limiting performance of integrated circuits (IC). Improvements can be achieved by implementing enhanced passive components on a specific chip beside the active die, by way of an integrated passive device (IPD) technology, or directly on the active die, from an above-IC integration. However, as IPD or above-IC current commercial technologies still propose only spiral inductors, the gain in performance is mainly based on the increased thickness of metal strips. The gain remains limited on Q-factor because of large inter-spire proximity effects, and the self-resonant frequency (SRF) is affected by the value of the substrate permittivity.

The solenoid topology can be an alternative to alleviate drawbacks of planar spiral structures. Because this three-dimensional (3-D) device is using the vertical dimension, its footprint on the substrate is lower. Such a topology improves Q-factor and *SRF* when the core of the coil is thick enough and turn-to-turn spacing is minimum [1]–[3]. Several solutions have been proposed for the fabrication of solenoids: deposition of thick insulating layers along with electroplated metallization [4], micromachining technologies to form air-core solenoids on top of a substrate [1]–[3], [5], [6] or in a cavity etched into the substrate [7]. Unfortunately, all these processes involve numerous and/or complex technological steps often constrained by equipment (masker resolution, UV source intensity and wavelength, etc.) and photoresist capabilities. As resulting core section and coil longitudinal compactness are usually too small, performance enhancement is not always in line with expectations.

The solution proposed in this paper addresses all the above-mentioned issues by using a new technology for the manufacturing of 3-D metal structures. After the description of the main steps of the process flow, experimental performances are presented for various 3-D solenoid inductors integrated on a glass substrate. The above-IC integration of solenoids over a silicon substrate is investigated and then compared to more usual planar approaches.

II. Fabrication Process

The fabrication process flow (Fig. 1) relies on two copper plating steps of thickness ranging from the standard of 15 µm up to 40 µm for compliance with high-power applications.

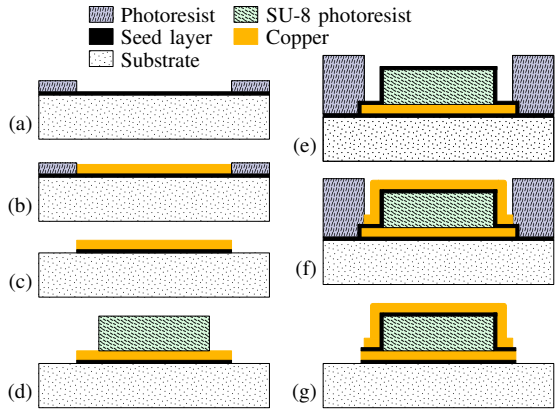

Fig. 1. 3-D integration steps (coil cross-sectional view).

First, a seed layer is sputtered over the substrate (a). The bottom metal layer is electroplated into openings of a patterned photoresist (b). The photoresist and the seed layer are removed (c). A 100 µm-thick SU-8 core ($\epsilon_r = 2.85$ and $tan\delta = 0.04$) is shaped (d), a new seed layer is sputtered and a sacrificial mold is patterned (e). This step is crucial since the thickness and aspect ratio of this mold determines the minimum lateral conductors width and spacing. Then, both side and top parts of the solenoid coil are formed in a single 3-D copper electroplating step (f), as reported in [8]. Finally, thick photoresist mold is removed and the second seed layer is etched (g). As described, when using the 3-D copper electroplating process, vertical and upper metal sections are fabricated simultaneously, so

This work was supported by the Région Midi-Pyrénées funded project Millitechno3D, under grant CLE-2012 no. 12050932 and by LAAS-CNRS micro and nano technologies platform member of the French RENATECH network.

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Manuscript received October 24, 2017; revised March 20, 2018; accepted April 20, 2018.

the numerous and critical steps for via hole implementation are avoided. For this process, three masks are needed for device fabrication and only standard equipment is used. After optimization, critical dimension tolerance is within $\pm 1.5\,\mu m$ and SU-8 resin thickness variation is within $\pm 3\,\mu m$. With a $100\,\mu m$-thick SU-8 layer, the minimum for metal width and spacing is $15\,\mu m$. When the low thermal budget, as well as the maximum temperature (bellow $150\,^{\circ}C$) are taken into consideration, it can be highlighted that this process is compatible with above-IC integration [8].

III. Results and Discussion

Four solenoid inductors have been designed and fabricated. Geometrical and measured electrical characteristics are summarized in Table I. Two of them are shown in Fig. 2. Devices L_1 and L_2 are both 3-turn and differ from conductor width w and spacing s. L_3 (6-turn) and L_4 (8-turn) are solenoids of large inductance values. They both share the same w and s as with L_2. The parameters l_s and w_s mentioned in Table I refer to solenoid total length and width, respectively.

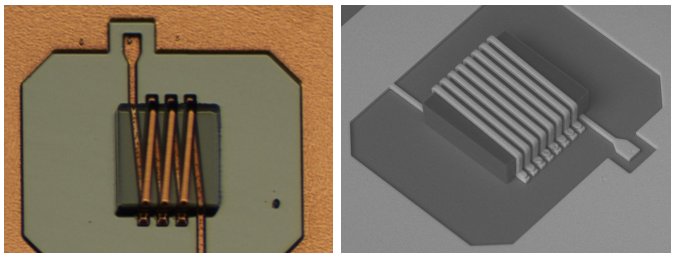

Fig. 2. Microphotographs of inductor L_1 (left) and SEM picture of L_4 (right).

TABLE I
Summarized Characteristics of the Inductors

Device	L_1	L_2	L_3	L_4
Number of turns n	3.4	3.4	6.4	8.4
w (µm) / s (µm)	30/30	20/20	20/20	20/20
Area w_s (µm) × l_s (µm)	350 × 240	350 × 160	350 × 280	420 × 360
L_{mes} @ 1 GHz /L_{calc}	2.3/2.5	3.0/3.4	5.8/6.1	9.5/10.2
L_{mes}/Area (nH/mm^2)	28	54	59	63
SRF (GHz)	19.1	16.8	11.4	8.1
Q_{max} @ f_{max} (GHz)	58 @ 5.6	55 @ 5.5	47 @ 4.6	40 @ 3.0

Inductors are embedded in a 1-port setup. On-wafer characterization of such high-Q inductive device is somewhat challenging. Vector Network Analyzer (VNA) measurement uncertainties on gamma (Γ) strongly affect the accuracy of the extracted Q factors for values beyond 50 [9]. An accuracy of 0.002 is verified on Γ magnitudes, all over the $40\,MHz - 20\,GHz$ frequency range. It translates into an uncertainty ΔQ of 7 for a Q value of 55 [9]. Parasitic interactions between the on-wafer setup and the inductor may have very visible effects when the Q-factor is high. These effects are minimized by tuning the internal dimensions and width of the metal ring surrounding the device under test (DUT) and connected to the ground tips of GSG probe [10]. Finally, inductance and Q-factor are derived from the measured Γ without de-embedding access wires and pads in order to keep the best measurement accuracy and to avoid additional errors. As a consequence, Q and *SRF* value are underestimated, up to $18\,\%$ and $5\,\%$ respectively, while inductance values are slightly overestimated ($+0.25\,nH$). However, the comparison with electromagnetic (EM) simulations carried out under the same conditions is more accurate [10].

Post-layout simulated and experimental L and Q values of L_1 to L_4 are plotted versus frequency in Fig. 3. EM simulations are performed by a 3-D EM simulator (ANSYS HFSS). As it can be noticed, results from measurements are in very good agreement with simulated data. The comparison of L_1 with L_2 shows that inductance density widely benefits from the reduction of s and w. A larger number of turns (from L_2 to L_3) increases the inductance and improves the inductance density thanks to a better magnetic flux confinement. The maximum density of $63\,nH/mm^2$ is reached by the 8-turn inductor L_4 because the number of turns and an increased core cross-section. Q_{max} is slightly decreased from L_1 to L_4, mainly because of increasing capacitive contribution of SU-8 core.

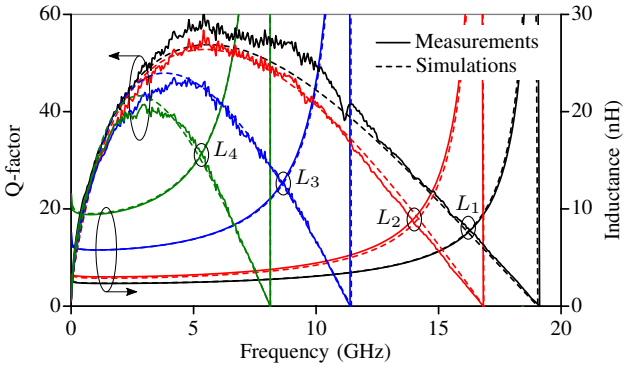

Fig. 3. Measured (——) and simulated (---) Q an L values versus frequency of devices L_1 to L_4.

The simple expression (1) can accurately predict the inductance value of a solenoid knowing its geometrical data. Table I reports calculated values (L_{calc}) for L_1 to L_4 using (1) added by access wires contribution ($\approx 0.25\,nH$).

$$L_c = \frac{\mu_0 n^2 A}{l_s} \tag{1}$$

In (1), A is the solenoid core cross-section. With an integer number of turns n, l_s and consequently L_c are proportional to n. The same proportionality is obtained for the resistance. Hence, unlike planar spiral inductors, adding turns to a solenoid does not degrade its Q-factor, as it is verified experimentally by Fig. 3, as long as dielectric contribution remains negligible (frequencies under $2\,GHz$).

EM simulations are used to evaluate the level of performance that can be expected from above-IC solenoids integrated using the proposed technology. The solenoids L_2 to L_4 are implemented above a $24\,\mu m$-thick layer of SU-8 resin, on top of a $10\,\Omega\,cm$ standard resistivity silicon substrate (Fig. 4(a)). As for CMOS and BiCMOS on-chip

planar inductors, a patterned ground shield is integrated under the solenoid using the first metal layer (a 0.6 µm-thick Al layer) of the back-end of line (BEOL). With this shielding, substrate induced dielectric losses are minimized. The stacking of all insulating layers of the BEOL is modeled by a single material with an ϵ_r of 4 and a thickness of 10 µm. Simulated data are presented in Fig. 4(b). As it can be expected, Q_{max} and *SRF* values are slightly lowered when compared with on-glass devices. Nevertheless, these values remain quite high, with Q_{max} ranging from 37 to 45 and the *SRF* from 5.5 GHz to 14 GHz. Inductance values remain almost unchanged.

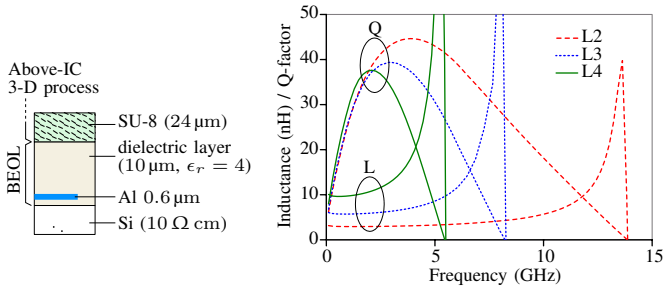

Fig. 4. (a) layers added under above-IC solenoids, (b) simulated data of above-IC solenoids L_2 (---), L_3 (····) and L_4 (——) versus frequency.

In Fig. 5, the new tradeoff between compactness and performance that can be achieved using the here-proposed solenoids is highlighted by the comparison with conventional planar technologies. The three main characteristics, i.e. surface area, Q_{max} and *SRF*, are reported versus inductor values in Fig. 5(a), (b) and (c), respectively. First, the comparison is made with on-chip silicon planar spiral inductors [11], [12]. If these inductors occupy the smallest area (Fig. 5(a)), as required for minimizing substrate-induced losses, they still present the lowest Q_{max} values (Fig. 5(b)), while *SRF* values remain close (Fig. 5(c)). Then, characteristics of some high-Q above-IC planar inductors [13] are reported in Fig. 5, as well. The process, as described in [13], is very close to best available IPD technologies: the inductor spiral is a 10 µm thick copper strip integrated on a 28 µm low ϵ_r thick insulating layer of benzocyclobutene (BCB), with a 10 µm thick copper underpass implemented 12 µm underneath. This time, it can be observed that the area of these inductors is about twice the area of 3-D solenoids (Fig. 5(a)), while the maximum Q-factor Q_{max} is twice for 3-D solenoids (Fig. 5(b)), and *SRF* remain quite close (Fig. 5(c)). These results again confirm the great interest of the proposed 3-D above-IC process. All other published solenoids are not reported in Fig. 5, either because their integration is not comparable, or because their performance is not in line with the expected level.

IV. Conclusion

A simple 3-D copper electroplating process involving two metallization steps has been successfully implemented for the fabrication of high performance highly integrated solenoid inductors. A maximum Q-factor Q_{max} of 58 and a self-resonant frequency *SRF* of 19 GHz are experimentally demonstrated

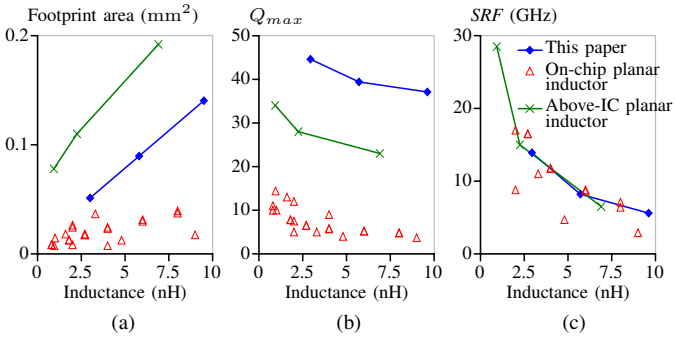

Fig. 5. Simulated characteristics of above-IC solenoids compared with on-chip [11], [12] and above-IC planar spiral inductors [13].

for a 2.3 nH solenoid. The best inductance-to-area ratio of 63 nH/mm² is reached by an inductor of 9.5 nH whereas all other characteristics remain very good, with a Q_{max} of 41 and a *SRF* of 8 GHz. When compared with planar inductors, these 3-D solenoids significantly improve the tradeoff between integration density and performance. Such a cost-effective 3-D technology then appears very promising for high-performance IPD or above-IC inductive device integration.

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