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Citation: Appl. Phys. Lett. **83**, 168 (2003); doi: 10.1063/1.1588378
View online: https://doi.org/10.1063/1.1588378
View Table of Contents: http://aip.scitation.org/toc/apl/83/1
Published by the American Institute of Physics

# Effect of annealing environment on the memory properties of thin oxides with embedded Si nanocrystals obtained by low-energy ion-beam synthesis

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(Received 17 October 2002; accepted 12 May 2003)

The effect of annealing in diluted oxygen versus inert environment on the structural and electrical characteristics of thin silicon dioxide layers with embedded Si nanocrystals fabricated by very low-energy silicon implantation (1 keV) is reported. Annealing in diluted oxygen increases the thickness of the control oxide, improves the integrity of the oxide and narrows the size distribution of the nanocrystals without affecting significantly their mean size ($\sim$2 nm). Strong charge storage effects at low gate voltages and enhanced charge retention times are observed through electrical measurements of metal-oxide-semiconductor capacitors. These results indicate that a combination of low-energy silicon implants and annealing in diluted oxygen allows for the fabrication of improved low-voltage nonvolatile memory devices. © *2003 American Institute of Physics.*
[DOI: 10.1063/1.1588378]

Memory cell structures using a metal-oxide-semiconductor field-effect transistor (MOSFET) with nanocrystals embedded within the gate $SiO_2$ have recently attracted much attention for high-density, low-voltage memory applications.[1] Among the different techniques aiming at the fabrication of silicon dioxide films with embedded nanocrystals, the very-low-energy ion-beam synthesis is of substantial interest as it allows for the formation of a two-dimensional array of Si nanocrystals in thin $SiO_2$ layers at relatively low doses and at a location tunable through the choice of implantation energy.[2,3] Recent work on nanocrystal memories obtained by using the latter technique gave attractive results,[4,5] suggesting that further elaboration on the fabrication routes may lead to structures of substantial impact to mainstream microelectronics. An important concern for the structures fabricated previously is related to the damage induced by implantation; such damage strongly affects the integrity of the oxide, and thus, the memory characteristics of the devices. In this work, we show conclusively that the latter problem can be significantly amended by performing the post-implantation annealing step in diluted oxygen. Here, the effect of the annealing atmosphere on the structural and electrical properties of low-energy Si-implanted $SiO_2$ films is examined through transmission electron microscopy (TEM) analysis and electrical measurements of MOS capacitors. Annealing in diluted oxygen environment has been applied earlier[6,7] only to thick oxides ($\sim$25 nm) implanted at high energies (20 to 25 keV) containing no nanocrystals; structures examined and most of the findings reported are not comparable to those considered herein.

Silicon dioxide layers 7 and 9 nm thick were thermally grown on 8-in., *p*-type, (100)-oriented Si wafers, and subsequently $^{28}Si$-implanted with an energy of 1 keV to a dose of $2\times10^{16}$ $Si^+$ $cm^{-2}$. Following the implantation step, all samples were furnace annealed under the following conditions: (a) 950 °C/30 min in inert ambient ($N_2$) or (b) 950 °C/15 min in $N_2$ ambient followed by 950 °C/15 min in $N_2$ diluted oxygen (1.5% $O_2$ per volume), or (c) 950 °C/30 min in $N_2$ diluted oxygen, hereafter referred as A1, A2, and A3 treatments, respectively. Fabrication of Al electrodes on both sides of the samples was followed for capacitance and current–voltage measurements of MOS capacitors. Cross-sectional high-contrast and high-resolution TEM (HRTEM) analysis as well as plane-view dark-field TEM inspection were performed on selected samples.

TEM examination of 7-nm-thick Si-implanted samples subsequently annealed following the A1 and A3 thermal treatments reveals the presence of a thin band of silicon nanocrystals ($\sim$2 nm in thickness) in the oxide layers (see Fig. 1). A significant oxide swelling (5.5 nm, including the nanocrystal band width) was observed for the A1 annealed samples. Effects of swelling for low-energy heavily Si-implanted oxides[2,3] and silicon substrate[8] have been previously reported. Overall change (swelling or shrinking) of oxide thickness can be caused by a host of factors. (A) Space taken by the implanted species. (B) Implantation of recoils

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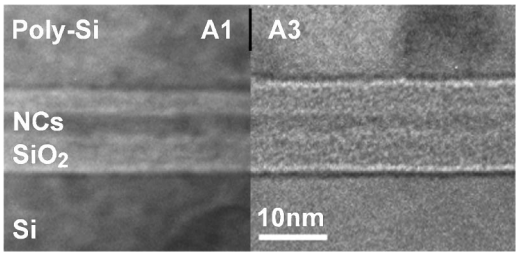


FIG. 1. Structure of 7-nm-thick $SiO_2$ samples implanted with $2\times10^{16}$ $Si^+$ $cm^{-2}$ at 1 keV and annealed following the A1 or A3 treatment. The mean thickness of the nanocrystalline layer thickness is about 2 nm in both cases. A3 thermal treatment leads to an increase of the control oxide by approximately 1 nm. A polysilicon film was deposited for TEM examination. Dimensions were evaluated from cross-sectional HRTEM and TEM under defocused bright-field conditions (see Refs. 3 and 11).

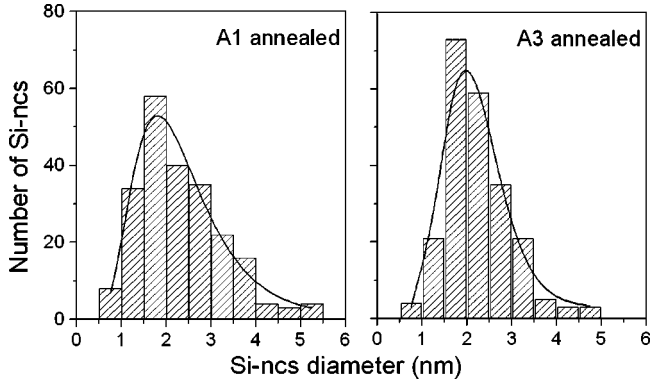


FIG. 2. Nanocrystal size distribution measured from plane-view TEM images of 7-nm-thick $SiO_2$ annealed according to the A1 or A3 treatment. The number-average size (mean size) is around of 2 nm for both samples.

that congest deeper in the matrix leaving vacancies behind[9] can also significantly contributed to volume changes. (C) Removal of near-surface atoms from the oxide (sputtering effect) during implantation that would ''reduce'' the A and B contributions to oxide swelling has to be taken into account but remains difficult to evaluate as the sputtering yield is very sensitive to surface roughness and any change in surface stoichiometry. (D) Possible change of density and also generation of strains as a result of crystallization. (E) Partial loss of implanted species upon substantial annealing. Other contributions are possible, as a result of incorporation of oxidizing species[10] from the air (F) or wet cleaning before annealing (G). Some pertinent contributions can be quantified while some others require further exploration. In addition, as there will be an interaction between some of the contributions it may not be possible for one to provide percentage contributions as there will be no additivity. It is of interest that additional TEM examination reveals that total swelling is slightly reduced (by ~0.5 nm) upon 950 °C annealing; this reduction may be due to a partial annealing of vacancies and/or to D and E contributions. We also find that the contribution from F is negligible as the same degree of swelling is observed whether the sample is wet-cleaned and then annealed or annealed without cleaning.

In addition, TEM examination reveals that the thickness of the oxide layer increases by about 6.5 nm after the A3 treatment. The differences in oxide thickness (~1 nm) observed between the A1 and A3 thermal treatments are mainly due to an increase of the thickness of the control oxide (the oxide layer between the top of the nanocrystal layer and the gate electrode). It is suggested that the observed oxide thickness enhancement is strongly related to a chemical reaction between excess silicon atoms and oxygen atoms. It is believed that during annealing in diluted oxygen of the Si-implanted oxides examined herein, the consumption of oxygen atoms by excess silicon atoms mainly takes place in the upper-half part of the Si-implanted distribution, thus leading to an increase of the control oxide thickness. TEM observations on 9-nm-thick oxides show that the structures obtained through A1 and A3 treatments follow the trends reported in Fig. 1 for 7-nm samples, with an additional thickness of about 2 nm of injection oxide (part of the oxide in between the $Si/SiO_2$ interface and the bottom of the nanocrystal layer). Furthermore, a combination of cross-sectional high-resolution and plane-view dark-field TEM analysis indicates that the nanocrystals are quasispherical in shape with a mean-diameter of about 2 nm (see Fig. 2). While no significant dependence of the nanocrystal mean-size on the annealing treatment was detected, TEM examination shows that a more uniform nanocrystal size distribution is obtained after the A3 treatment compared with the A1 treatment.

The effect of annealing ambient on the electrical properties of Si-implanted oxides has been examined through high-frequency (1 MHz) $C-V$ measurements under white light illumination conditions. The gate voltage was swept from inversion to accumulation and back to inversion at a rate of 0.5 V/s. The capacitor area was $100\times100$ $\mu m^2$. White light illumination was used to avoid deep depletion conditions that can occur at large positive gate voltages. The structural modifications induced by a post-implantation annealing in diluted oxygen are clearly reflected in the $C-V$ characteristics of 9-nm-thick Si-implanted samples reported in Fig. 3. In case of samples annealed following the A1 treatment [Fig. 3(a)], while no significant flat-band voltage shift ($\Delta V_{FB}$) is detected when the gate voltage is swept from $+2$ V to $-2$ V and back to $+2$ V, higher negative gate voltages lead to a positive voltage shift. This positive voltage shift is due to

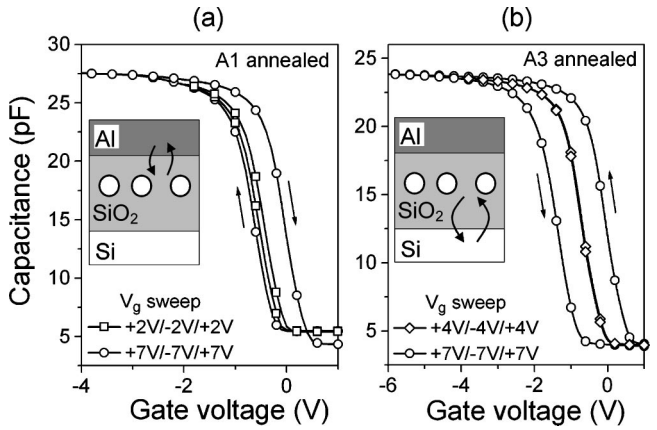


FIG. 3. High-frequency $C-V$ curves for a 9-nm-thick oxide layer implanted with $2\times10^{16}$ $Si/cm^2$ at 1 keV and subsequently annealed following (a) the A1 treatment or (b) the A3 treatment. (a) Negative gate voltage causes electron injection into the oxide from the gate (or hole extraction from the oxide, see inset) and a sweep of $V_g$ from accumulation ($-V_g$) to inversion ($+V_g$) traces the curve indicated by the arrow pointing to the right. (b) High positive and negative gate voltages cause, respectively, electron and hole injection into the oxide from the substrate (inset).

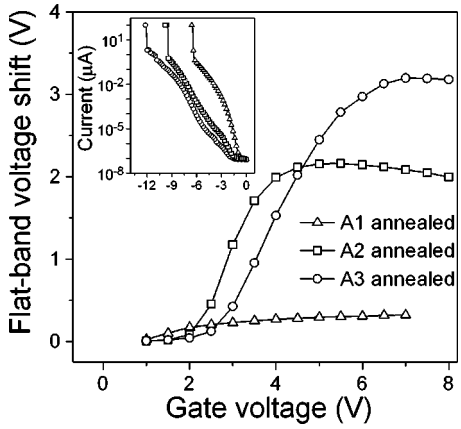


FIG. 4. Flat-band voltage shift ($\Delta V_{FB}$) as a function of the gate voltage round sweep for 7-nm-thick oxide layers implanted with $2\times10^{16}$ Si/cm$^2$ at 1 keV and subsequently annealed following the A1, A2, or A3 treatment. Inset: Magnitude of the dark gate current under accumulation conditions as a function of negative ramped gate voltage (1 V/s).

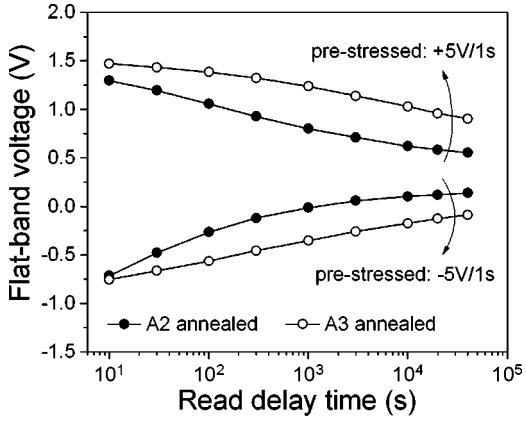


FIG. 5. Data retention characteristics of 7-nm-thick oxide layers implanted with $2\times10^{16}$ Si/cm$^2$ at 1 keV and subsequently A2 or A3 annealed. The magnitude of the applied gate voltage stress was $+5$ V or $-5$ V for 1 s.

negative charge trapped into the oxide following electron injection from the gate electrode. If the annealing sequence uses a thermal treatment in diluted oxygen (treatment A2 or A3), no hysteresis appears in the $C-V$ curves at positive or negative gate bias lower than 5 V [Fig. 3(b)]. Higher positive or negative gate voltages cause the $C-V$ characteristics to shift in the direction of stored negative or positive charges, respectively. In this case, charge trapping occurs through electron and hole injection from the substrate into the oxide. We suggest that as a result of implantation damage recovery and control oxide swelling during annealing in diluted oxygen, the integrity of the control oxide is significantly restored, charging from the gate is not detectable and effective charge injection from the substrate occurs.

The effect of the A1, A2, and A3 post-implantation thermal treatments on the memory window of 7-nm-thick oxide layers is shown in Fig. 4. In comparison with the A1 treatment, the magnitude of $\Delta V_{FB}$ as a function of the gate voltage sweep strongly increases after the A2 and A3 thermal treatments. It is believed that such an increase is due mainly to the improved quality of the overall oxide and enhanced thickness of the control oxide. This view is further supported by the observed gate current versus gate voltage characteristics under accumulation conditions of Si-implanted oxides subsequently annealed following the A1, A2, and A3 treatments (inset of Fig. 4). It is clear that annealing in diluted oxygen leads to oxides with a strongly reduced conductivity.

Finally, in view of the significant charging observed at small gate voltages (despite the large injection oxide thickness), it is inferred that the integrity of the injection oxide remains affected by the implantation process after annealing in $N_2/O_2$ ambient. It is suggested that remaining structural defects (e.g., excess of silicon atoms) enhance the conductivity of the injection oxide, through probably a trap-assisted direct tunneling current, thus leading to an effective charge injection into the nanocrystals at lower voltages than those required for a thermal tunnel oxide of equivalent thickness. A substantial contribution of these defects to the charge trapping reported herein is not excluded.

Measurements of the charge retention time at room temperature have been performed for 7-nm-thick A2 and A3 oxide layers through application of a $\pm5$ V gate voltage stress for 1 s. The flat-band voltage after electron (write) or hole (erase) injection as a function of waiting time is shown in Fig. 5. For the A2 sample, the flat-band voltage window significantly narrows within the first 15 min and subsequently decreases from 0.8 to 0.4 V through a waiting time of 11 h with a possible trend for stabilization. The A3 sample provides substantially larger windows for the range of times explored, with a window of about 1 V, corresponding to a waiting time of 11 h. Additional experiments performed on the same type of samples but with an additional 15-nm-thick deposited oxide reveal very similar window decay rates, thus indicating that charge loss occurs through the injection oxide and not through the control gate oxide.

Overall, appropriate midly-oxidative annealing of low-energy Si-implanted thin oxides was shown to lead to improved electrical characteristics pertinent to low-voltage nonvolatile memory cell applications.

This work was a part of the NEON project and was funded by the EC as GROWTH GRD1-2000-25619.

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