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Power Modeling for Fast Power Estimation on FPGA

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Abstract

Nowadays energy consumption is a major criterion in any electronic system, especially when it comes to systems working at high throughput with restricted energy consumption constraints like in the Internet of things (IoT), wireless sensor networks, etc.

In a near future, these devices will connect billions of services with different computing intensive applications including smart homes, wearable devices, health-care and smart cities. For these devices, the major source of power will be a either a battery or an energy harvesting system. In this context, new design constraints are going to appear and will definitely require to take power consumption into account during all the design process and especially in the first steps, at high-level where decisions have the greatest impact on the performances.

In our work, a power estimation methodology has been proposed to allow the designer to explore various hardware architectures in terms of power consumption and performances. After a simple high-level simulation, designers are able to compare several approaches and orient their choices toward an efficient solution. In our study, FPGAs devices have been first considered but we believe that this methodology could also be applied to circuits like ASICs.

This methodology consists in developing several power models for different operators or IPs like the arithmetic operators (adders, multipliers and memories), integrating them with high-level tools like Matlab and Labview for high-level power estimation.

The methodology aims to make design space exploration a lot easier, providing early and fast power and performance estimation at high-level. It also proposes an efficient way to efficiently compare several systems. The methodology is effective through an operator characterization step and the development of their models. Then, a high-level description of the entire system is realized from the models that have been previously developed. High-level simulations enable to check the functionality and evaluate the power and performance of the system.

These power models are based on neural networks that predict the power consumed by digital operators implemented on FPGA. These operators are interconnected and the statistical information of the data patterns are propagated among them. The obtained results make possible an overall power estimation of a specific design. A comparison is performed to evaluate the accuracy of the power models against the Xilinx Power Analyzer tool (XPA) for individual operators with an mean absolute percentage error that show an accuracy with less than 0.01%. Case studies are also presented as well as a focus on global power estimation for digital signal processing (DSP) function. Our approach shows a mean absolute percentage error of 12% versus the time consuming Xilinx classical flow of power estimation based on (XPA).

This new power estimation approach based on the decomposition of a digital system into basic operators. Each operator will be given its own model which estimates the switching activity of internal and output signals. By interconnecting several operators at high-level, switching activities and percentage of logic high are then propagated to enable a global power

estimation of a given system. This new approach provides flexibility for system designers, since it allows them to evaluate the power consumption of digital system at high-level of abstraction with a promising speed-up factor of the design process. It is not necessary to work at the RTL any more in order to obtain accurate results in terms of power consumption. As a consequence, there is no need to look at the register level and help them in avoiding of repeating the whole estimation process from scratch for each minor changes that can be appear after design evaluation of a complete system. This novel approach is suitable for digital systems with a significant level of complexity that can be decomposed into operators. However, most of the research community are interested in the power estimation at hight-level in the absence of hardware details.

The existing tools like Matlab and LabView are working at algorithmic level, then they are powerful enough to evaluate the functionality of a system then the performance. Making the gap narrower between the tools working at high-level of abstraction and the tools working at transistors level to evaluate the power consumption is a novel idea to make the design exploration easier for the system designers without the need to go deep into the hardware details which is a time consuming processes. As demonstrated the optimization at algorithmic level is the more efficient and practical way to achieve a maximum power efficient communication systems.

The effectiveness of the methodology has been demonstrated throughout several works like in [LPH16], [NPHL17]. To conclude, the main limitations of the proposed methodology have been investigated and addressed.

References

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[NPHL17] Y. Nasser, J. C. Prévotet, M. Hélard, and J. Lorandel. Dynamic power estimation based on switching activity propagation. In *2017 27th International Conference on Field Programmable Logic and Applications (FPL)*, pages 1–2, Sept 2017.