Degradation of hard MOS devices at low temperature

N.T. Fourches

DAPNIA/SEDI, CEA Saclay, 91191 Gif-sur-Yvette, France

Abstract : A study of n-channel MOS transistors stressed under Fowler Nordheim injection was made both at room temperature and low temperature (77 K) . Using alternatively positive and negative bias one can create interface states or bulk oxide charge at 300 K. This is comparable to ionising irradiation. At 77 K a slight reverse annealing occurs , due to the weak neutralization of interface states , under negative bias. Under positive bias no significant threshold voltage shift occurs at low temperature, almost all the interface charge being compensated by the oxide charge.

1. INTRODUCTION

There is a field where some work has been made in the last few years in cryogenic electronics: it is the ionising radiation effects on microelectronic Metal Oxide Semiconductor transistor devices . Quite recently some progress has been made in the CMOS technologies [1].Cryogenic radiation hard technologies have emerged based on the progress of submicronic integration of devices. However it is still interesting to investigate key issues in other degradation effects at cryogenic temperatures. This is the scope of our present work.

2. IRRADIATION AND CHARGE INJECTION : DEGRADATION

As the temperature lowers ,the Debye length reduces and operation of MOS devices is favourable due to leakage current reduction . At low temperature after ionising radiation exposure the threshold voltage shift is similar for either p-channel and n-channel devices due to the dominant contribution of self trapped holes in the gate oxide V_t shift at temperatures lower than 100 K [2] is significantly higher than at room temperature. Due to the annealing considerations , the radiation tolerance can only be kept for low dose rates [2] for micronic technologies. Deep submicronic technologies are more radiation tolerant due to tunnel annealing through the thin gate oxide [1] . There are great similarities between ionising irradiation effects on the gate oxide and degradation of the oxide by injected charges from both the gate and the bulk silicon. At room temperature these degradation effects have been thoroughly addressed by many authors for standard CMOS technologies [3-11]. In today's context of development of microelectronics for long lasting high energy physics experiments [12] , this is a crucial issue , therefore stress experiments on radiation hard devices from the development batches of a SOI (thick film) technology have been made.

3. MEASUREMENTS AND RESULTS

The devices under study were fabricated on a SOI substrate with an epitaxial film grown on the original substrate. The (Metal Oxide Semiconductor) MOS transistors used for this study had a designed gate length is of the order of 0.6 micrometers and the gate width 25

micrometers. In order to meet the radiation hardness specifications, the 21 nm gate oxide was grown on (110) silicon at relatively low temperature (below 1000 °C) under wet and dry conditions alternatively. Post oxidization anneals were kept to a minimum. The gate is made of doped polysilicon. For the measurements and stresses a parameter analyzer (HP 4145) is used. The threshold voltage is determined from the $I_d = F(V_g)$ characteristic in the linear mode together with the subthreshold slope (weak inversion regime). The determination of the midgap voltage is possible using the MacWhorter and Winokur method allowing the respective contributions of the trapped oxide charge and the c:Si/SiO₂ interface states to be calculated. During stress at an optimum stressing point, the drain and source of the transistor are connected to the bulk which is held at 0 volts while the gate is biased.

3.1 Room temperature results

The n-channel transistors were chosen because they are preferable for the search of the effect of interface states under irradiation. The interface states are generated under normal gate bias conditions and have the effects of compensating the bulk trapped oxide charge. Fowler Nordheim stress regime at room temperature is used to generate bulk oxide charge and interface charge. The current through the structure follows a $J \sim V^2 \exp(-b/V)$ law which is characteristic of tunnel emission (Physics of Semiconductor Device S.M. Sze p 403). This proves that a Fowler Nordheim tunneling regime is established through the structure at 300K. On figure 1(a) it can be seen that the creation of interface states during positive biased stress greatly offsets the creation of bulk charged centers located in the a:SiO₂. The threshold voltage shift increases of nearly 1 V after 3000 seconds + 15.5 Volts stress.. The mechanisms for interface state creation can be hole or a positively charged specie moving towards the interface, reacting with the electrons from the silicon and not trapped by the oxide centers located close to the interface. This means that the precursors of the charged centers have a sufficiently low concentration to become inactive or the trapped carriers can escape by tunneling given the high field during stress, contrary to irradiation where the interface and oxide charges compensate [2]. This could mean that hole injection to the oxide from the gate does not create stable defects.

Figure 1 : (a) plot of the threshold voltage shift, with its contributions from the trapped oxide charge, the interface charge, versus stress time. All the measurements were made at 300 K on a n-channel structure biased positively (gate bias + 15.4 V). (b) same plot with measurements made at 300 K on a n-channel structure already stressed positively. The gate bias during stress was negative (- 15.4 V).

The difference between hard and soft oxides could then be the fact that the concentration of precursors in the oxide is lower for a hard oxide than for a soft one. If the E' centers are the dominant traps for holes gamma irradiation creates E' centers (trivalent defect associated

with an oxygen vacancy). Precursors can exist in the silicon rich area , near the c:Si /a:SiO₂ interface.

When the device is subsequently stressed with opposite bias (-15.5 Volts on the gate (figure 1(b)) the threshold voltage shift is due to positive oxide charge creation with a very low interface state creation . This could be due to hot hole injection from the substrate into the oxide, that could create E' centers in a two step process , first precursors (oxygen vacancies) are created , then the holes are trapped by the defects to form positively charged E' centers. A relatively low number of holes generate Pb interface centers . A quantitative approach may be introduced , to determine a capture cross section for carriers (holes) of the E' precursors.

If J is the current density (carrier/cm²s) , σ the capture cross section (cm²) , and n_{ot} the number of centers in the oxide under study , one obtains : $J \sigma = dn_{ot}/dt$ by integration , this leads to : $\sigma J.t = n_{ot}$ where t is the total injection time . n_{ot} can be deduced from the relation $C_{ox} \Delta V_{ot} = q n_{ot}$ where C_{ox} is the oxide capacitance and ΔV_{ot} the threshold voltage shift due to the oxide trapped charge. With the values used for this study ($t = 2500$ s, $n_{ot} = 15000$) we obtain : $\sigma = 6 \cdot 10^{-18}$ cm² , which is a relatively weak value for a capture cross section , this suggest that the centers are originally neutral and are not coulombic defects. That interpretation is in agreement with the E' center generation model. A conclusion can be drawn : electrical stressing with positive gate biasing followed by negative gate biasing is apparently equivalent to ionizing irradiation for a n channel device; in the sense that the charge in the oxide is compensated at the end of biasing process by the interface charge (see figure 2). A quantitative approach is more difficult since the energy deposited in the oxide during electrical stressing is a necessary parameter.

3.2 Low temperature results

At low temperature the picture is different (Figure 2) . For positive bias , the threshold voltage shift remains stable during stress , both the oxide charge and interface charge increase on a fresh sample . The oxide trapped charge does not increase greatly during stressing under negative bias , holes do not seem to be injected easily from the substrate to the silicon dioxide , this proves that this injection mechanism is temperature dependent , or that the traps are not effective at this temperature. E' generation could also be low in these conditions , the remaining holes being trapped in shallow polaron states at this temperature in the same way as the during irradiation [2].

Figure 2 : (a) plot of the threshold voltage shift , with its contributions from the trapped oxide charge , the interface charge , versus stress time. The measurements were made at 77 K , with a positive bias on the gate (+15.4 V) on a fresh and already 300 K stressed structure. (b) Same as (a) with a negative gate bias (-15.4 V) on a 300 K stressed structure.

It has been shown in a previous work that the annealing of polaron states (or self trapped holes) is greatly enhanced by electric fields above 5 MV/cm, this explain the apparent low positive charge introduction rate. One stringent feature of these results is that the low temperature stressing at negative bias results in a negative shift of the interface state threshold voltage shift. The most plausible interpretation is that an anneal of Pb centers occurs due to holes neutralizing negatively charged Pb centers :

Hole (from the bulk silicon) + Pb (negatively charged) $\rightarrow$ Pb anneal (neutral)

There is no evidence for oxide charge annealing, demonstrating that neutralization of E' centers is less important than the neutralization of interface states.

4. CONCLUSIONS

Fowler Nordheim injections were made on MOS devices at low temperature. Positive bias injection does not create many E' centers in the bulk oxide (at 300K or at 77K). Tunneling electrons do not create bulk defects close enough to the interface and that they have not enough energy to create neutral defects through a electronic process [13]. Holes migrate through polaronic hopping in the opposite direction and could contribute to the weak generation of stable E' centers (11) at room temperature but it seems that the fast transport of holes (electric field enhanced) generates more interface states (Pb like) than bulk defects. With positive bias most of the current is formed of electrons, the holes being minority carriers, in a sufficient number to generate Pb centers. Under negative bias only oxide traps precursors can be generated by, possibly, incoming electrons from the gate. The macroscopic effects were understood by the combination of microscopic mechanisms close to the ones acting during ionizing irradiation. The presence of a weak reverse annealing process was established at low temperature.

References

- [1] Jenkins W.C., Liu S.T., IEEE Transactions on Nuclear Science, Vol 47, No 6 (3), (2000) 2204-2207
- [2] Fourches Nicolas T., Phys. Rev. B Vol 55, No 12, (1997) 7641
- [3] Chen T.P., Li Stella, Fung S., and. Lo K.F., IEEE Transactions on Electron Devices, Vol 45, No 9, 1920-1926 (1998)
- [4] Pananakakis G. and Ghibaudo G., Papadas C. and Vincent E., Kies R., J. Appl. Phys. 82 (5), 2548 (1997)
- [5] Dimaria D.J., Appl. Phys. Lett., Vol 75, No 16, 2427 (1999)
- [6] Candelori A., Paccagnella A., Cammarata M., Ghidini G., and Fuochi P.G., IEEE Transactions on Nuclear Science, Vol 45, No 6, 2383-2386 (1998)
- [7] Lee K.Y., Fang Y.K., Chen C.W., Huang K.C., Liang M.S., and. Wu S.G., IEEE Electron Device Letters, Vol 18, No 8, 382-384 (1997)
- [8] Ang D.S. and. Ling C.H., IEEE Electron Device Letters, Vol 20, No 3, 135-137 (1999)
- [9] Rodriguez R., Nafria M., Miranda E., Suné J., Aymerich X., IEEE Electron Device Letters, Vol 20, No 7, 317-319 (1999)
- [10] Spinelli Alessandro S., Lacaita Andrea L., Rigamonti Matteo, and Ghidini Gabriella, IEEE Electron Device Letters, Vol 20, No 3, 106-108 (1999)
- [11] Eriguchi J Koji and Niwa Masaaki, IEEE Electron Device Letters, Vol 18, No 12, 577-579 (1997)
- [12] ATLAS, Technical Proposal, CERN/LHCC/94-43/LHCC/P2 (1994) p44,83
- [13] Revesz A. G., IEEE Transactions on Nuclear Science, NS18, No 6, 113 (1971)