Bromine/methanol wet chemical etching of via holes for InP microwave devices

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We report on the realization of via holes on InP material (for the first time to our knowledge) using bromine/methanol wet chemical etching. Typical dimension of the via holes is about 80 μm in diameter. A specific layout has been accomplished to obtain the via hole equivalent circuit. Measurements have been performed from 50 MHz to 30 GHz. They exhibit losses of 0.1 dB at 30 GHz. The via hole equivalent circuit is found to be a resistance and an inductance in serial configuration with typical values of 0.4 Ω and 26 pH, respectively. © 1998 American Vacuum Society. [S0734-211X(98)00702-1]

I. INTRODUCTION

At microwave frequencies, microstrip lines are one of the most common transmission structures to perform monolithic microwave integrated circuits (MMICs). In fact, via hole technology allows good thermal dissipation and small size circuits owing to the grounding back side. InP devices demonstrate good electrical properties and the realization of a good via hole etching on this material is essential.

Only few papers are reported on this subject. Dry etching using electron cyclotron resonance (ECR) Cl_2/Ar plasma has been demonstrated with vertical profile and relatively fast etch rate (2.7 $\mu\text{m}/\text{min}$).¹ Other plasma etchings with ECR^{2,3} or with a reactive ion etching (RIE) chamber⁴ have also been demonstrated. Good results have also been shown with laser-assisted photoelectrochemical etching.⁵ Via hole technology would be simplified using wet chemical etching, but to our knowledge it has not yet been reported on InP wafers. The main reasons are the difficulty in obtaining a good uniformity and the strong isotropy of the wet chemical etching. In this article we report on the realization of via holes on InP material using bromine/methanol wet chemical etching to perform field effect transistors (FETs) in microstrip technology.

To validate our technology, a specific layout has been realized to measure only the via hole without the other elements. It allows one to obtain an equivalent circuit up to 30 GHz.

II. MICROSTRIP TECHNOLOGY

The realization of this technology requires five main steps:

- (i) Etching of blind holes on the front side. They will be used for the via hole step.
- (ii) Processing of the transistors.
- (iii) Thinning of the wafer to obtain the good characteristic impedance value of the transmission line.

(iv) Etching of the via holes from the back to the front of the wafer side to reach the front side source electrodes. The via hole optical mask alignment is performed with the blind holes.

(v) Electroplating of the wafer back side to realize the electrical grounding.

The process sequence is represented in Fig. 1 with a cross-sectional view.

For the wet chemical etching of InP material, it is important to avoid too much undercut to permit a high via hole density. The chosen etchant is bromine/methanol which gives desired profiles. The etching rate can be controlled by varying the bromine concentration in the methanol but it can become dangerous to have more than 10% of bromine due to its instability.⁶ Hence, a volume percent of 3 has been chosen, which is a good compromise between the etch rate (about 8 $\mu\text{m}/\text{min}$) and the mixture instability. This concentration falls down during the etching process due to the bromine evaporation. Nevertheless, it is not an obstacle for our technology.

(i) The first step of our microstrip technology consists of making blind holes on the front side. Obtaining a good and reliable uniformity etching is necessary because they will be used for the via hole back side alignment. Because the bromine/methanol mixture etches photoresists, a dielectric masklike silicon nitride (Si_3N_4) or silicon oxide (SiO_2) is required. Hence, a 1000 Å Si_3N_4 film is deposited by plasma enhanced chemical vapor deposition (PECVD) at 300 °C with a Plasma Lab 80 Plus of Oxford Plasma Technology on a 2 in. (001) oriented InP wafer. A Shipley 1400-27 photoresist is then patterned to obtain 80×80 μm^2 squares. The Si_3N_4 is etched at a pressure of 30 mTorr with a CF_4 , CHF_3 , and O_2 gas ratio of 40/25/4 sccm, respectively, in a RIE chamber. The rf power used is 100 W and the dc bias is -430 V. Then, the wet chemical etching using 3% bromine in methanol was done at room temperature for 10 min. The rinsing liquid is methanol. But to avoid the back side of the wafer is etched, the substrate is adhered with wax on a silicon wafer which does not react with the mixture. The

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FIG. 1. Cross-sectional view of the process sequence: (a) blind hole etching, (b) blind hole blocking up and metallization layer protection, (c) via hole etching, and (d) back side gold electroplating.

(110) cleavage plane exhibits a reverse mesa-shaped structure and the (110) cleavage plane a V-shaped structure.⁷ Since there is no undercut due to strong Si_3N_4 adherence, the etching will be stopped owing to the V-shaped profile [Fig. 1(a)]. Figure 2 shows depth cartography of blind holes for two quarters of 2 in. InP wafer after 10 min etching. The measurements were performed with a Tencor P-10 surface profiler. For the two samples, the average depth is about $45 \pm 2 \mu\text{m}$, which demonstrates very good uniformity. This is the key point which will allow proper alignment of the via holes and therefore superior reliability.

Prior to removing the mask, another 1000 Å Si_3N_4 layer is deposited to block up the blind holes. A Shipley 1400-27 photoresist is then patterned and the 2000 Å Si_3N_4 film is then etched by plasma (under the same conditions as mentioned earlier) everywhere on the wafer except for 160×160

FIG. 2. Blind hole depth cartography after 10 min etching using 3% bromine/methanol on two quarters of 2 in. (001) oriented InP wafer.

μm^2 squares on the blind holes and where the via holes will arrive on the front side source electrodes [Fig. 1(b)]. This dielectric film avoids the liquid etchants passing from the back to front side through the blind holes during thinning and the via hole steps. It also protects the metallization layers at the end of the etching of the via holes.

(ii) The next step is the processing of the FETs. The InP substrate is removed from the silicon wafer with trichloroethylene which dissolves the wax. The ohmic contacts, the mesa etching and the gate deposition are performed successively. We can observe in Fig. 1(b) that a part of the metallization layers is deposited on the Si_3N_4 film.

(iii) At this moment, the wafer must be thinned. Prior to this step, a 10 μm thick Hoechst 4562 photoresist is deposited on the wafer's front side to protect the transistors. Next, the same side is adhered on a silicon wafer with a wax. The substrate is chemically thinned at room temperature with a $\text{HCl}/\text{H}_2\text{O}$ (5:1) solution which produces superior uniformity and fast etch rate (10 $\mu\text{m}/\text{min}$). The thickness is controlled during the process with a Mitutoyo micrometer until $\sim 40 \mu\text{m}$. The check is made too by observing the blind holes on the back side. They have an oblong form due to the reverse mesa-shaped structure on the (110) plane. When they become visible on the whole wafer, it is certain that the thickness is under $45 \mu\text{m}$. Therefore, this is essential information to control the thickness and show how much the uniformity of the blind hole etching is primordial.

(iv) For the via hole procedure, a dielectric mask deposited at a temperature below the wax melting point (70°C) is required. Si_3N_4 deposited by PECVD at 60°C has bad adherence. In fact, after the photoresist annealing at 60°C , the dielectric moves away from the wafer. The solution found is to sputter a 500 Å SiO_2 film at room temperature. Then, a Shipley 1400-27 photoresist is spun on the back side and annealed at 60°C for 30 min in an oven. The via hole alignment is performed owing to the blind holes to pattern $80 \times 80 \mu\text{m}^2$ squares. The SiO_2 film is etched by plasma in the same manner as that of Si_3N_4 , as described previously. The hole dimensions are small enough to obtain a relatively high via hole density. The etching of the via holes is then accomplished from back to front side using a 3% bromine/methanol solution and is stopped on the Si_3N_4 layer, which was deposited to protect the metallization layers [Fig. 1(c)]. A plasma etching of the Si_3N_4 film of the front side and the SiO_2 film of the back side is realized in a RIE chamber under the same

FIG. 3. Cross-sectional SEM photograph of a via hole.

conditions as mentioned earlier. This plasma etching does not etch the front side metallization layers.

(v) The next step is the back side metallization for the ground. To increase the adherence of the gold which will be electroplated, a gold film must be first deposited on the back side. The vacuum evaporation technique does not deposit metallization on the hidden parts of the wafer (the reverse mesa-shaped structure). Nevertheless, the gold film is deposited on the V-shaped walls which represent the greater majority of the via hole walls. In addition, the cathodic sputtering technique allows one to deposit the gold film on all the walls of the via hole. So this sputtering technique is preferred to obtain the best metallization of the via hole.

To prevent the substrate from becoming curved due to the gold strains after electroplating and removing from the silicon wafer, a 5.5 μm thick Hoechst 4562 photoresist is patterned with a chessboard-shaped mask. This photoresist is post-baked for 1 h at 60 °C in an oven to improve its adherence. To electroplate gold, the wafer is connected to the cathode owing to the sputtered gold film. A Pt wire is used as the anode. The electrodes are immersed in a Sel-Rex Pure Gold 402 electrolytic solution, with KAu(CN)₂. A dc bias is applied between the electrodes to obtain a current density of 2.5 mA/cm², allowing one to achieve a thickness of 3 μm in 15 min. Gold is electroplated on the via holes and on the whole wafer [Fig. 1(d)], except for some horizontal and vertical lines. These lines are about 150 μm in width and are spaced by the field dimension (7 mm in our case). At last, the wafer is removed from the silicon wafer with trichloroethylene. Figure 3 shows a scanning electron microscope (SEM) photograph of a via hole V-shaped cross section. It represents the right part of Fig. 1(d). The gold is heavily electroplated on the back side and on the walls of the via hole. It is connected with a source electrode on the front side wafer. Around the source, the Si₃N₄ film, which was deposited to protect the metallization layer, is also visible. In the photograph's background we can see two source electrodes with a microstrip line in the middle of them. It is possible to per-

FIG. 4. Specific layout to measure via hole elements in the dotted line plane.

form smaller via holes, but the wafer would be thinner due to the V-shaped profile.

III. ELECTRICAL MEASUREMENTS

dc and microwave measurements up to 30 GHz have been done to validate our microstrip technology. A specific layout has been performed to characterize and to deduce the equivalent circuit of a via hole, without other elements, up to 30

FIG. 5. Evolution of the S11 (a) and S11 magnitude (b) of a via hole from 500 MHz to 30 GHz.

FIG. 6. Evolution of the real (a) and imaginary (b) Z11 parts of a via hole from 500 MHz to 30 GHz.

GHz. The measurements are calibrated in the plane represented in Fig. 4 by the dotted line with a specific calibration kit (TRL).

Figure 5 shows on the Smith chart the S11 and also the S11 magnitude evolutions from 500 MHz to 30 GHz measured with this specific layout. Figure 5(a) demonstrates that the via hole fits in a short-circuit up to 30 GHz. Figure 5(b) exhibits losses of only 0.2 dB at 30 GHz for the S11 magnitude. So the via hole losses are only 0.1 dB since S11 represents the reflection of a via hole that is two times its losses.

The equivalent circuit of a via hole is a resistance and an inductance in serial configuration. Figure 6(a) demonstrates a

very low resistance up to 30 GHz from the Z11 real part. dc measurements exhibit a typical value of about 0.4Ω . Figure 6(b) shows the Z11 imaginary part of a via hole measured with the specific layout. The linear behavior demonstrates that it is an inductance and a calculation determined from the line slope gives 26 pH.

IV. CONCLUSION

In conclusion, via holes have been successfully realized for the first time to our knowledge on InP substrates by wet chemical etching using bromine/methanol. The blind holes depth uniformity allows one to have a reliable technology. The substrate thickness is $40 \mu\text{m}$ and is back side electroplated with a chessboard-shaped $3 \mu\text{m}$ thick gold film. Measurements allow one to obtain the elements of the via hole equivalent circuit, which are an inductance of 26 pH and a resistance of 0.4Ω in serial configuration. The electrical losses due to a via hole are only 0.1 dB at 30 GHz.

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