Impact of aging on the soft error rate of 6T SRAM for planar and bulk technologies

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A B S T R A C T

This paper evaluates the impact of aging on the radiation sensitivity of 6T SRAM for two planar bulk technologies. This study is motivated by the growing impact of aging and radiation effects on the reliability of CMOS technology. A modelling methodology dedicated to this new phenomenon is proposed. This modelling uses the radiation modelling device MUSCA SEP3 and an electrical aging modelling. First, the impact of aging on SEE sensitivity is studied through a parametric modeling of the threshold voltages of the transistors composing the 6T SRAM. Then, an operative avionics environment is modelled in order to evaluate the consequences on reliability.

Keywords:
Aging
NBTI
6T SRAM
SEE
Modelling
Soft error rate

1. Introduction

By following and exceeding Moore's law [1], the CMOS technology has seen its performances strongly increase over the last decades. The main areas of improvement have been the increase in clock pulses frequency and the decrease in power consumption. This aggressive scaling had to be done at the expense of other parameters. Radiation sensitivity and degradation mechanisms were two reliability issues that were impacted by this scaling.

The CMOS inverter is sensible by design to cosmic particles that can ionize its composing silicon and create a parasite short-circuit. The increase of radiation sensitivity is a direct result of the decrease of operative voltages and the large-scale integration. The decrease of the voltage threshold (V_{th}) has lowered the minimal charge needed to open a conduction path between the source and the drain of a transistor. The ongoing decrease of the voltage threshold has made CMOS technology sensitive to more and more particles over the course of its integration. The first single event effects (SEE) observed had been caused by neutrons and heavy ions, SEE caused by protons and muons have been observed respectively in 2007 [2] and 2010 [3]. The large-scale integration has also increased the density of transistors in a given volume, enabling a single charged particle to deposit a significant amount of energy to flip several logical cells. This type of error is called multiple-cell upset (MCU), MCUs can easily occur in static random access memory (SRAM) [4] as similar logical cells are condensed in a restrained volume. The 6T SRAM cell is the most popular design for memory cell due to its good balance between stability and performance. It is widely used in modern processors and ASICS. Mitigation features such as Error correction code (ECC) or hardened layout can be employed, especially for registers containing critical data such as L1 caches. However, these methods both have limits to their effectiveness ECC so MCUs should still be monitored to assure that they don't exceed a definite limit. Moreover, performance or cost will be a trade-off of the implementation of these features.

The transistors composing a 6T SRAM cell are also sensitive to several front-end of line (FEOL) reliability mechanisms. FEOL mechanisms such as negative bias temperature instability (NBTI), hot carrier mechanisms and oxide degradations all have an impact on the threshold voltage of transistors. These degradations affects the stability of the cell, in particular the static noise margin. The static noise margin has been shown to be correlated with radiation sensitivity [5]. V_{th} being a key parameter for the SEE sensitivity of the 6T SRAM cell justify this study.

From a safety standpoint, ensuring the radiation sensitivity of CMOS electronic systems over their lifetime is a requirement for industries using embedded electronics in life-critical systems. This paper presents a modelling approach at circuit level in order to estimate the impact of this potential phenomenon on two planar bulk technologies, the 45 and 32 nm nodes.

2. Modelling methodology

A modelling platform has been developed in order to study the combined effects of aging degradation and radiation susceptibility [6]. This

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http://dx.doi.org/10.1016/j.microrel.2017.07.078

platform consists of a combination of modelling devices including multiple physical models and scales. Those modelling devices include radiation field modelling, MUSCA SEP3 (Multi-Scales Single Event Phenomena Predictive Platform, [7,8,9]) for the simulation of the interactions between the radiative environment [10] and the materials composing the electronic devices, aging mechanisms modelling and electronic technology modelling.

The modelling of radiation effects in nanoscale devices requires taking into account high level physical description. Thus, realistic secondary ion track 3D structures issued from GEANT4 simulations were considered [11,12,13]. Carriers and charges evolve according to mechanisms such as drift (electric field), diffusion (carrier concentration gradient), collection and recombination processes [14]. SEE assessment consists in coupling MUSCA SEP3 with electrical simulations (CADENCE tool) [15].

The Fig. 1 provides an overview of the different modelling devices involved in this study and their interoperability.

Aging mechanisms are modelled through their impact on the threshold voltage of pMOSFET and nMOSFET composing a 6T SRAM. Numerous degradation mechanisms activated in a 6T SRAM have an impact on the threshold voltage, but only simplified models of threshold voltage shift are considered. These models are based on three points: time dependency, temperature dependency, and saturation value.

NBTI has always been identified as the main degradation mechanisms activated by a CMOS inverter structure, but has only started to be a reliability concern below the 130 nm node [16,17]. NBTI is activated through an electrochemical reaction, leading it to be process dependent. The introduction of high-κ materials as dielectric layers is one the reason of the recent growth of NBTI [18]. The threshold voltage shift of pMOS induced by a NBT stress is dependant of temperature and time. Gate voltage dependency is not considered here as it is assumed to be constant. Temperature dependency is modelled with Arrhenius law and time with a power law [19,20,21]. Empirical models are used to match the saturation effect observed in NTBI.

Hot carrier injection is the degradation mechanisms that impact nMOS transistors. Positive BTI impact on nMOSFETs has grown with the latest technological nodes, and may even outmatch the effect of hot carrier injections in future technologies, but will not be considered in this study.

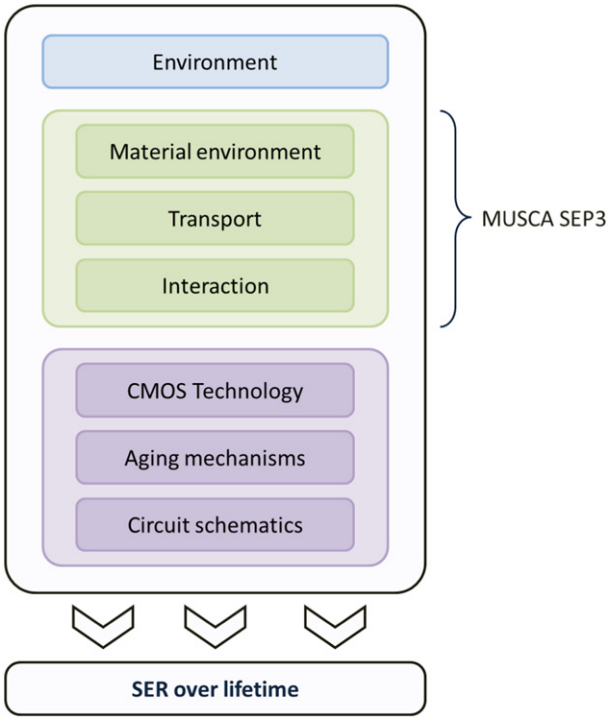

Fig. 1. Methodology of the different modelling devices and their interactions.

Table 1
Modelling parameters of studied technologies.

Node (nm)	Vdd (V)	Type	Vth (V)	Max ΔVth (V)	Cell area (μm²)
45 nm	1.1	nMOS	0.64	0.05	0.345
		pMOS	−0.58	0.1	
32 nm	1	nMOS	0.63	0.05	0.171
		pMOS	−0.59	0.1	

V_{th} shift in nMOS channel due to HCI is assumed to be proportional to the number of interface and oxide traps ΔN generated in a sensitive volume of the conduction channel [22]. Time-dependency of ΔN can be described with the lucky-electron model [20,23] as a power law. Temperature dependency has been changing with the lowering of gate length. In short channel devices, hot carrier degradation in nMOSFETs increases consistently with temperature [24]. This is aggravating for CMOS reliability as pMOSFETs and nMOSFETS degradation are both increased with temperature.

Reliable CMOS transistors models describing their electrical behaviour have been used in this study. These models have been developed through the predictive technology model program [25,26]. These models have been updated with data provided by integrated device manufacturers [27,28].

The main technological parameters used for modelling are summed up in Table 1.

In the first part of this study, a parametric study on the threshold voltage is presented. This parametric study is done in order to first evaluate the impact of V_{th} on SEE sensitivity.

In a second part, an aging profile representing the evolution of V_{th} over time is proposed. Then, a specific avionic environment is modelled to evaluate the SEE sensitivity over the lifetime of a SRAM 6T.

3. Impact of the threshold voltage on SEE sensitivity

A parametric study on the threshold voltages of the transistors that composed the 6T SRAM has been made in order to gain a better understanding of its impact on SEE sensitivity. The radiation sensitivity is characterized by the cross section, representing the probability for a given particle to cause a SEU or a MCU; it is expressed in cm^2/bit which represents the theoretical sensible area if all incident particles were to have a probability of interaction of 1.

The combined effects are a theoretical symmetrical shift of pMOS and nMOS transistors, this is unlikely to occur for all values covered and a more realistic combined effect will be used in a second part.

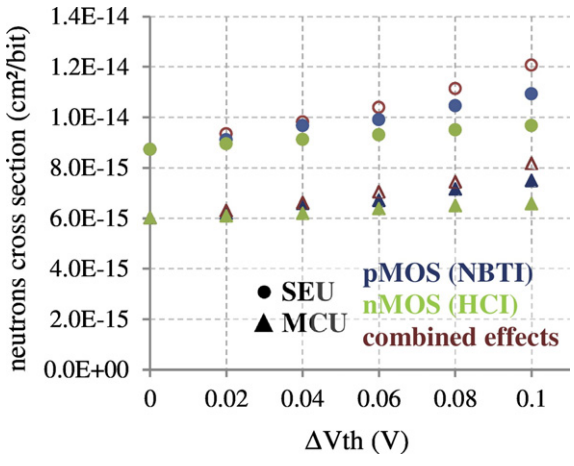

Fig. 2. Impact of the threshold voltage of the transistors composing a 6T SRAM planar bulk 32 nm on its neutrons cross section.

Fig. 3. Probability of number of bit upset per bit flip induced by a neutron particle in a planar bulk 32 nm 6T SRAM cell.

3.1. Threshold voltage dependency

The pMOS threshold voltage has the most impact on the SEE sensitivity of 32 nm SRAM (see Fig. 2), the nMOS threshold voltage only has a slight effect on the SEE sensitivity. The correlation between ΔV_{th} and the cross section is linear. The combined effect of nMOS and pMOS voltage threshold are the worst case degradations, it can be noted that the cross section with combined effects is higher than the sum of cross sections of nMOS and pMOS.

A given particle has more probability to flip at least two bits than only one (see Fig. 3). It can also be noted that a consequent number of MCU are more than two-bit upsets. The prevalence of a pair number of event is attributed to the symmetrical design of the SRAM cell. The threshold voltage shift does not affect the occurrence rate of MCUs.

The proton cross section can also be obtained in order to simulate a realistic radiative environment. The proton cross section of a planar bulk 32 nm, although being 100 times lower than the neutron cross section, still contributes to soft errors in an atmospheric environment. V_{th} shift impacts the proton cross section in a similar manner than the neutron cross section.

The 45 nm cell presents a similar trend than the 32 nm related to the pMOS V_{th} dependency (see Fig. 4). The nMOS V_{th} shift is slightly beneficial to SEE sensitivity. The fact that the 45 nm cell has a higher cross section than the 32 nm cell can be counterintuitive, as the 32 nm cell requires less energy to be flipped. It is explained by the difference in cell area (see Table 1), meaning that less particles will impact a 32 nm cell. However, the more packed design of the 32 nm cell show a higher rate of MCU than the 45 nm cell.

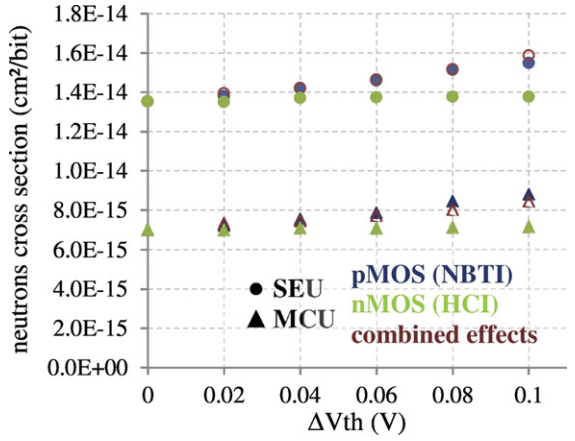

Fig. 4. Impact of the threshold voltage of the transistors composing a 6T SRAM planar bulk 45 nm on its neutrons cross section.

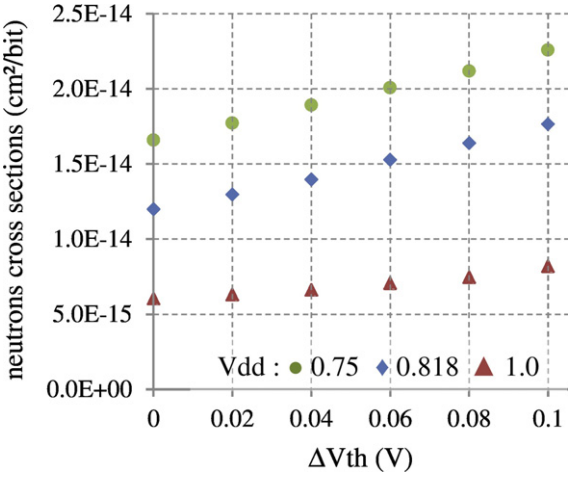

Fig. 5. Impact of the threshold voltage of the transistors composing a 6T SRAM planar bulk 32 nm on its neutrons cross section for three supply voltages.

3.2. Supply voltage dependency

The value of supply voltage is often lowered to reduce the consumption. It has a direct impact on the radiation sensitivity, as the electrical charge needed to flip a bit is lowered. Fig. 5 show the influence of the threshold voltage for 32 nm 6T SRAM. In addition to the increase of the cross section at low voltage, the impact of aging is amplified.

4. Impact in an operational environment

As an example of the practical impact that this underlined phenomenon could have, an avionics environment is modelled. Avionics component are prone to aging due to their intensive use and are more exposed to radiations at high altitude and high latitude. In previous works [29], *Hubert* et al. presented a new atmospheric radiation model named ATMORAD based on simulations of extensive Air Showers according to primary spectra which only depend on the solar modulation potential (Force-Field Approximation). Thanks to this approach, the solar modulation potential can be deduced from cascade neutron measured in neutron spectrometer network operating simultaneously instruments in French Pyrenees and Antarctica [30,31] (Pic-du-Midi observatory and Concordia station, respectively). Thus, it is possible to extrapolate the spectral fluency rate of secondary particles [31,32] considering any geographical location by data assimilation process (using physical models of primaries and atmospheric showers). In this study, a realistic Paris - New-York flight is considered, using data issued from the Eurocontrol

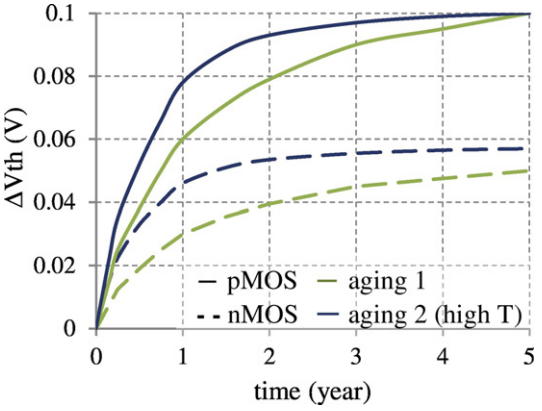

Fig. 6. V_{th} shift over time in a 6T SRAM used in this modelling.

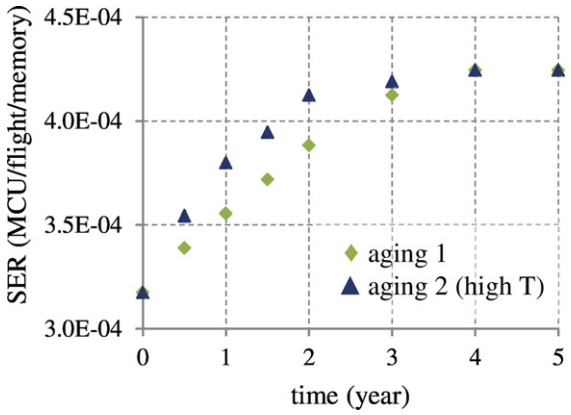

Fig. 7. Evolution of the SER over the lifetime of a 2 MB 6T SRAM bulk 32 nm for a Paris – New York flight.

Demand Data Repository [33] database. This flight of 8 h30 approaches high latitudes and is submitted to higher radiations than most flights.

These results are presented for two hypothesis of degradation of threshold voltage over time. Fig. 6 presents two aging profiles, profile 1 is made for an average temperature of 25 °C, and profile 2 is representative of a higher temperature of 75 °C. The values of ΔV_{th} have been chosen to be consistent in terms of growth rate and saturation value [21,24]. A linear degradation is proposed in the early stage of aging to take into account the recovery phenomenon of NBTI.

The reliability of a 6T SRAM cell of 2 MB is considered. The soft error rate (SER) is expressed for the number of MCU per flight per memory. Fig. 7 shows the evolution of the reliability of a 32 nm cell over the lifetime for the two aging profiles. The cell reaches a maximum degradation SER_{max} of 33% of its original SER. This maximum is not dependent on the aging profile due to the saturation effect of NBTI. However, the aging profile could matter in term of maintainability: in this example, a component accepting a degradation of its SER of 25% would have to be changed over a year of use with the high temperature aging profile, but with last 8 months more with the aging profile 1. In order to overcome the consideration of aging profile, the SER_{max} needs to be considered.

Fig. 8 compares the 45 and 32 nm cells. Although the planar bulk 45 nm cell presents a higher SEE sensitivity at nominal threshold voltages than the 32 nm node, their sensitivity become similar considering a worst case degradation. Threshold voltage has more impact on 32 nm SRAM SEE sensitivity than for the 45 nm SRAM. In a similar way than before, taking into account the SER_{max} would allow the reliability assessment to be refined.

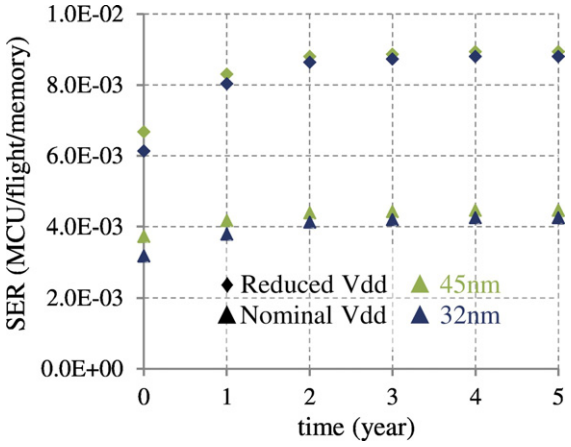

Fig. 8. Comparison of the SER in 6T SRAM of two planar bulk technologies at two supply voltages for a Paris - New York flight, the aging profile 2 (high T) was used.

5. Conclusion

An example of the impact of aging on the SEE sensitivity of the 6T SRAM has been given for two planar bulk technologies. The pMOS threshold voltage has been identified as the main parameter involved in SEE sensitivity.

Modelling of an operational avionics environment highlighted the significance of the soft error rate corresponding to the maximum threshold voltage degradation. Shorter lives devices could be operated under a lower SER requirement but would require a more refined modelling of their aging profile.

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