AIRBUS GROUP

INTRODUCING ICIM-CPI TO MODEL THE IC IMMUNITY TO CONDUCTED PULSES

PRISCILA FERNANDEZ-LOPEZ (VALEO)

CHRISTIAN MAROT (AIRBUS)

OUTLINE

- Context
- ICIM-CPI model structure
- PIML format
- Application case
- Conclusions and Perspectives

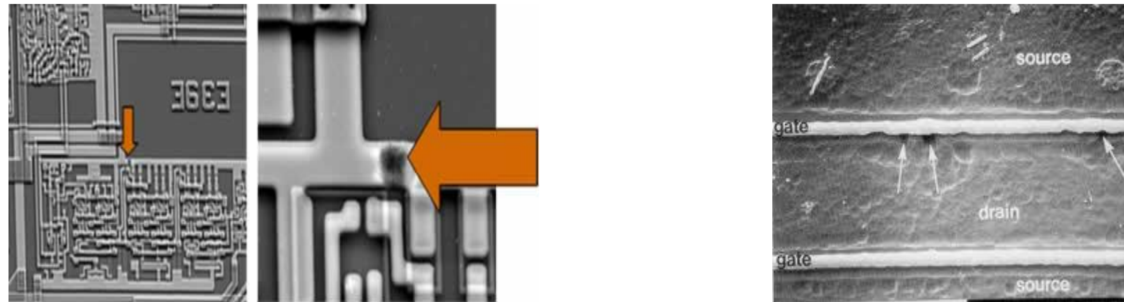
Valeo

AIRBUS GROUP

CONTEXT

CONTEXT

○ **ESD (ElectroStatic Discharge) and EFT (Electric Fast Transient) may be the origin of ICs susceptibility.**



○ **They can be caused by component handling during assembly or from user's body, and by switch contact closure or switched-mode power supply.**

○ **To prevent IC failure to these transient stresses, various tests have been designed:**

- TLP (Transmission Line Pulse) described in IEC 62615.
- Human Body Model (HBM)
- IEC 61000-4-2 and IEC 61000-4-4 (Testing and measurement techniques).

CONTEXT – IMMUNITY TO TRANSIENTS MODELLING

- **No model is available to predict failure/destruction of an IC due to transients by simulation.**

- **Such a model may help to design internal or external protections to comply with requirements.**

- **State of the art of the IC models for EMC simulation in IEC 62433 (*“EMC IC modelling”*):**

		Conducted	Radiated
Emission		ICEM-CE (62433-2)	ICEM-RE (62433-3)
Immunity	**CW**	ICIM-CI (62433-4)	ICIM-RI
	Transient	ICIM-CPI (62433-6)	ICIM-RPI

Published
Ongoing
No Standard

- Part 6: Models of ICs for Pulse immunity behavioural simulation – Conducted Pulse Immunity (ICIM-CPI)

Valeo

CURRENT DOCUMENT FOR ICIM-CPI

- Document submitted by the French National Committee
- Discussed in TC 47 / SC 47A / WG2
  - Partners: US, DE, FR, IE,NL, UK, JP, KR

- Next meeting: September 2017 in Regensburg (Germany)

EMC IC modelling –

Part 6: Models of Integrated Circuits for Pulses Immunity behavioural simulation – Conducted Pulse Immunity modelling (ICIM-CPI)

1 Scope

The objective of this part of IEC 62433 standard is to provide a flow for deriving a macro-model to allow the simulation of the conducted transient immunity of an Integrated Circuit (IC) to pulses such as Electrostatic Discharge (ESD) and Electric Fast Transient (EFT). It is intended to be used for predicting the immunity levels to conducted pulses disturbances applied on IC pins. This model is commonly called Integrated Circuit Immunity Model Conducted Pulse Immunity, ICIM-CPI. It is intended to be used for predicting the immunity levels, both damage and function failure, to conducted pulses disturbances applied on IC pins.

ICIM-CPI can be extracted for analogue, digital and mixed-signal ICs. An ICIM-CPI models one IC, with its several terminals (e.g. input, output and supply pins). To correctly describe the immunity to pulses, an ICIM-CPI describes the nonlinear behaviour of the IC terminals.

An ICIM-CPI can be inserted into a time-domain electric circuit simulation. That way, failure can be predicted at IC, board and equipment level, when submitted to conducted pulses.

This document has two main parts:

- the first is the electrical description of ICIM-CPI macro-model elements
- the second part proposes a universal data exchange format called PIML based on XML. This format allows encoding the ICIM-CPI in a more useable and generic form for immunity simulation.

INTERNATIONAL ELECTROTECHNICAL COMMISSION

____

EMC IC modelling

Part 6: Models of integrated circuits for Pulse immunity behavioural simulation - Conducted Pulse Immunity (ICIM-CPI)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62433-6 has been prepared by subcommittee 47A: Integrated Circuit, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
XX/XX/FDIS	XX/XX/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,

AIRBUS
GROUP

ICIM-CPI MODEL STRUCTURE

ICIM-CPI MODEL STRUCTURE

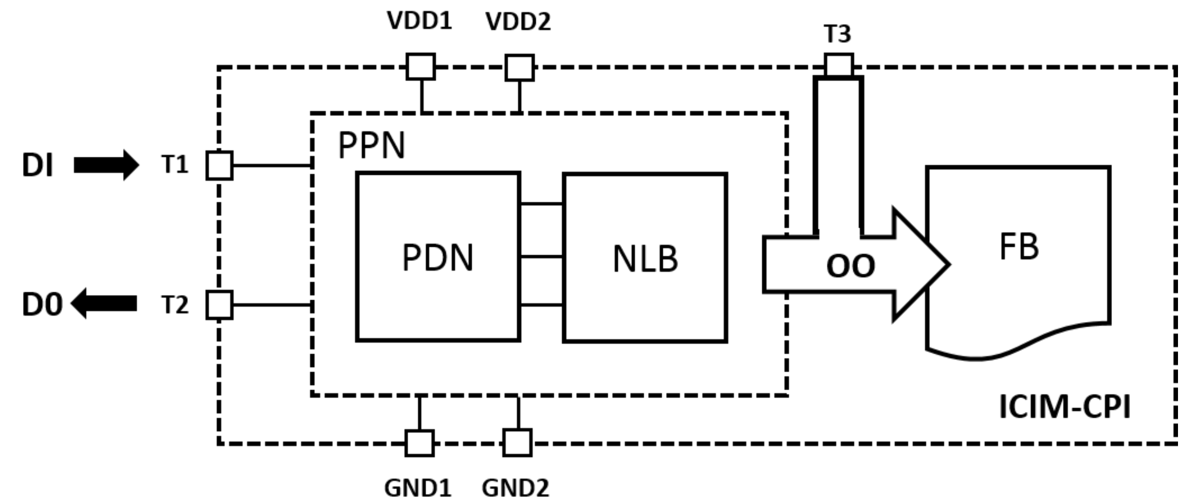
○ **PPN (Pulse Propagation Network): describes the pulse propagation path**

- PDN (Passive Distribution Network): *linear* characteristics
- NLB (Non-Linear Block): *non-linear* characteristics

○ **FB (Failure Behaviour): describes how the IC reacts to the applied pulse disturbance according to a failure criterion**

○ **Terminals:**

- DI (Disturbance Input): terminal for injection
- DO (Disturbance Output): terminal whose Z influences the PPN transfer characteristics
- OO (Observable Output): terminal where signal is monitored
- VDD: power supply
- GND: ground reference

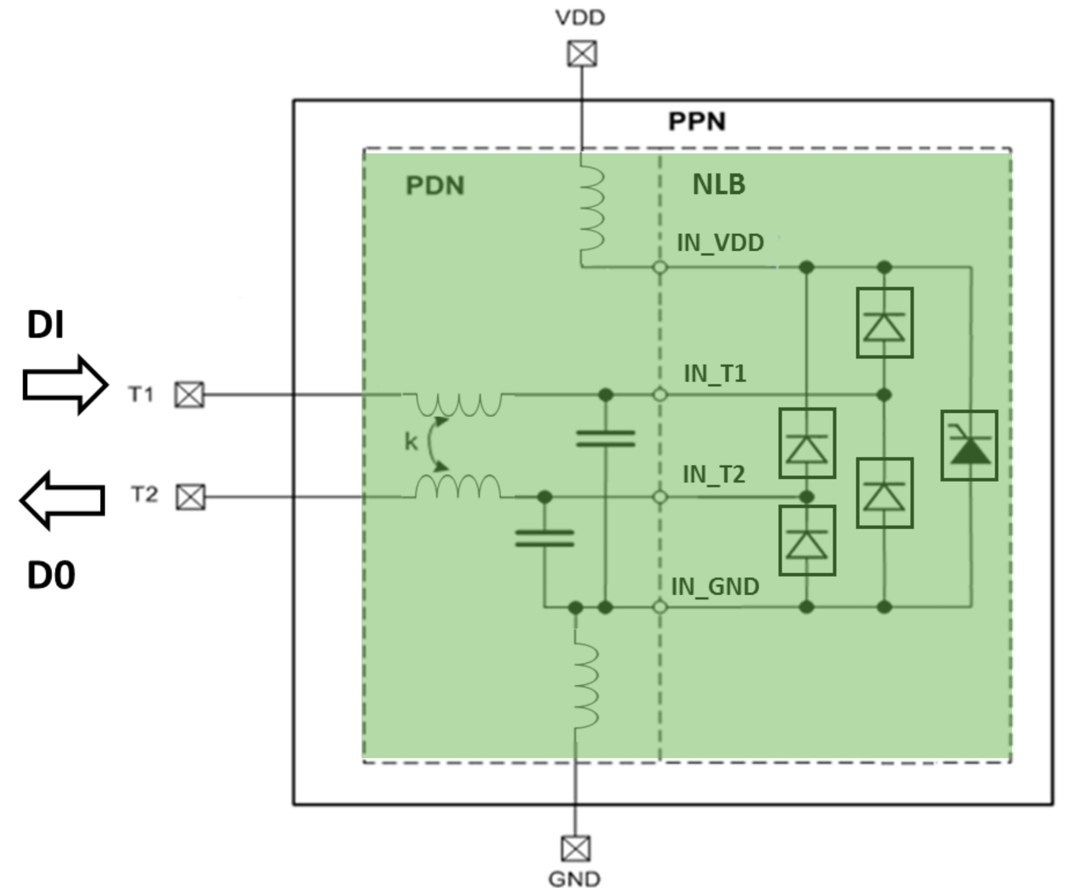


Valeo

PPN – PULSE PROPAGATION NETWORK

- **The PPN consists in two parts:**
  - PDN: linear network modelling the IC connections (package interconnections, bonding wires…)
  - NLB: non-linear block modelling the ESD protection devices (diodes and other components)

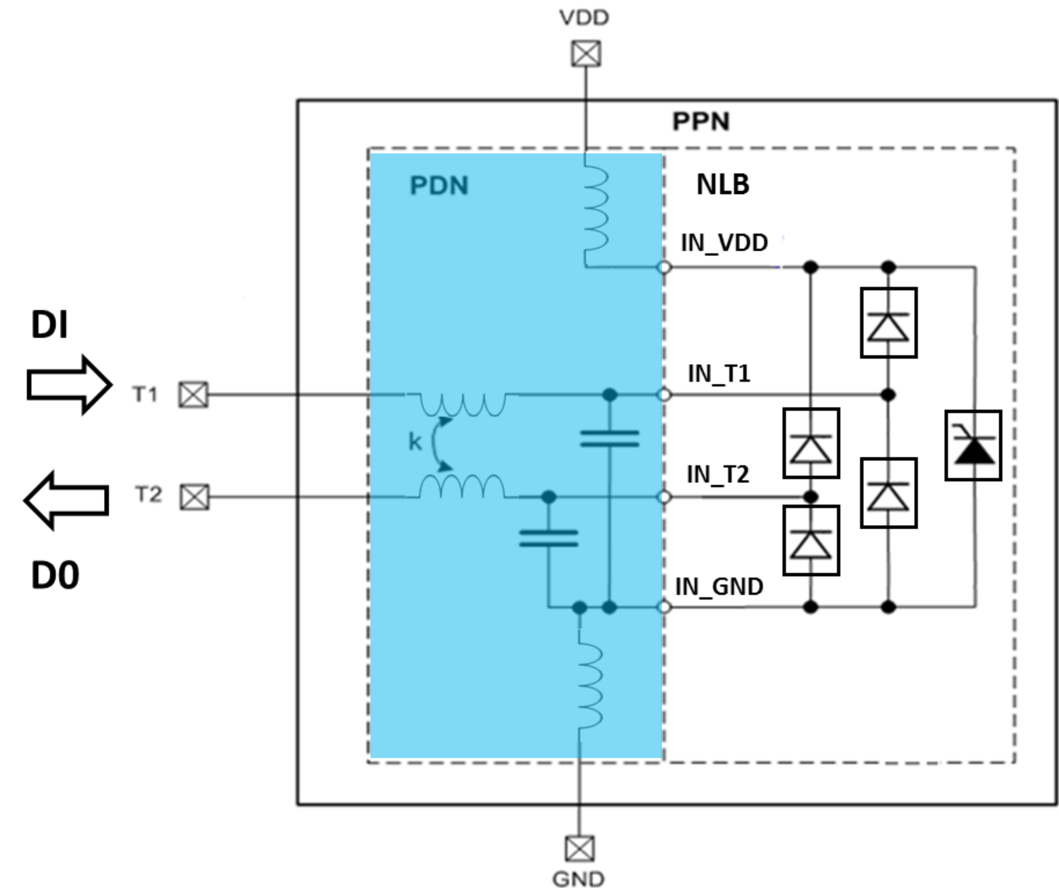
- **Internal Terminals (IN_x): connect PDN and NLB**



Valeo

PDN – PASSIVE DISTRIBUTION NETWORK

- **Passive elements for the package, bonding wires and on-chip interconnection.**
- **Linear elements: R, L, C, k.**
- **Z network including all the propagation paths taken by the pulse injected to DI:**
  - Z between DI and GND
  - Z between DI and DOs (as couplings exist between them)
  - Z between DO and GND

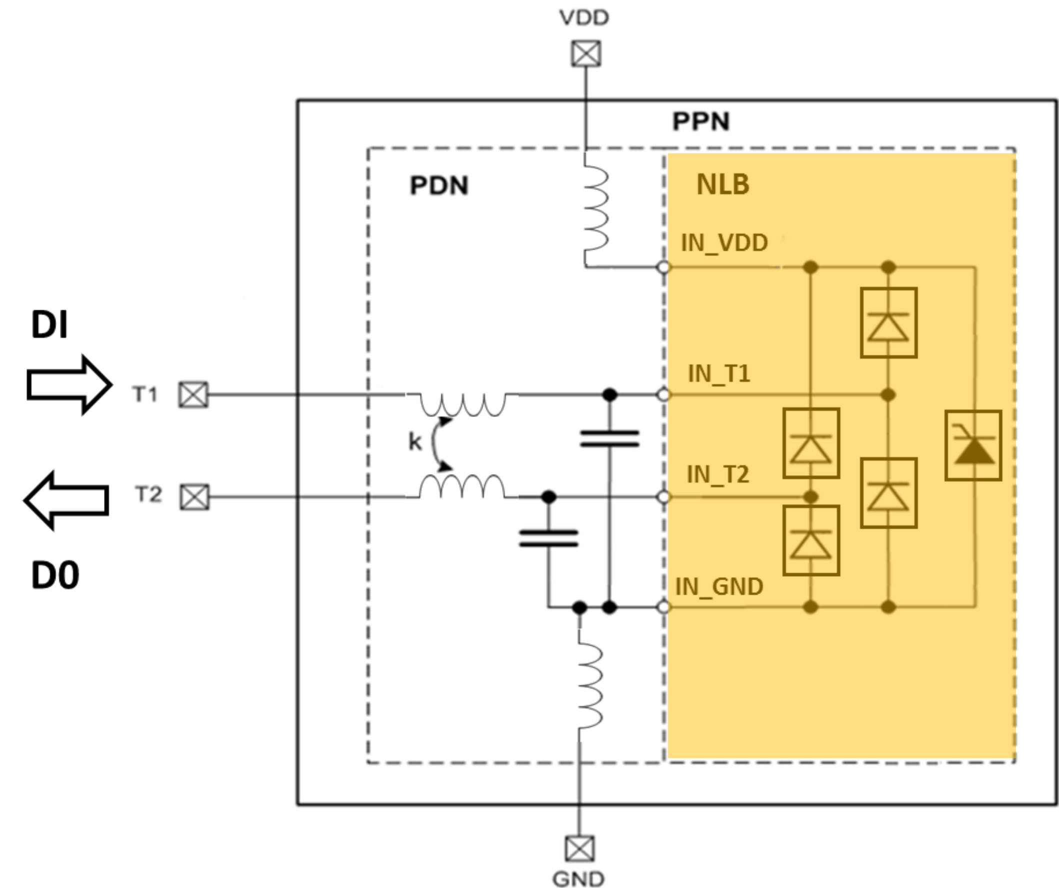


- **PDN can be extracted from:**
  - S-parameters
  - IBIS file

NLB – NON-LINEAR BLOCK

- **Non-linear behaviour of the IC input network (protection devices as diodes, gate-grounded NMOS structures, …)**

- **NLB extracted from:**
  - IBIS file
  - By simulation with a circuit simulator according to the end-user's knowledge of the IC.
  - I/V measurements performed with a TLP generator (IEC 62615 standard).



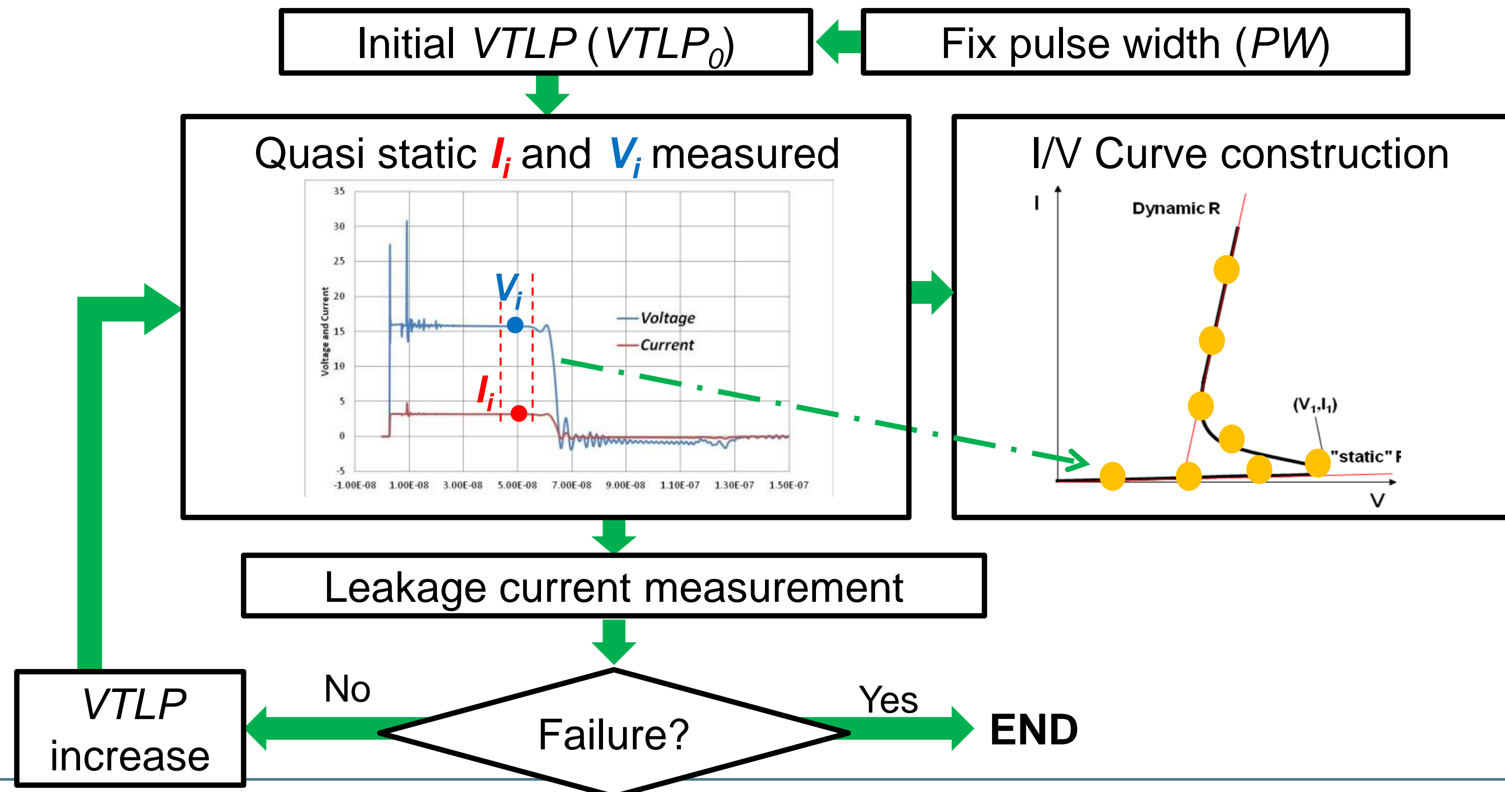
NLB – I/V MEASUREMENT WITH TLP GENERATOR

○ TLP (Transmission Line Pulse) Generator:

- Polarity: « + » or « - »
- Pulse width (*PW*): from 50ns to 1µs
- Magnitude (*VTLP*): from 10V to 4kV

○ I/V measurement steps:

- Between DI and its GND



Valeo

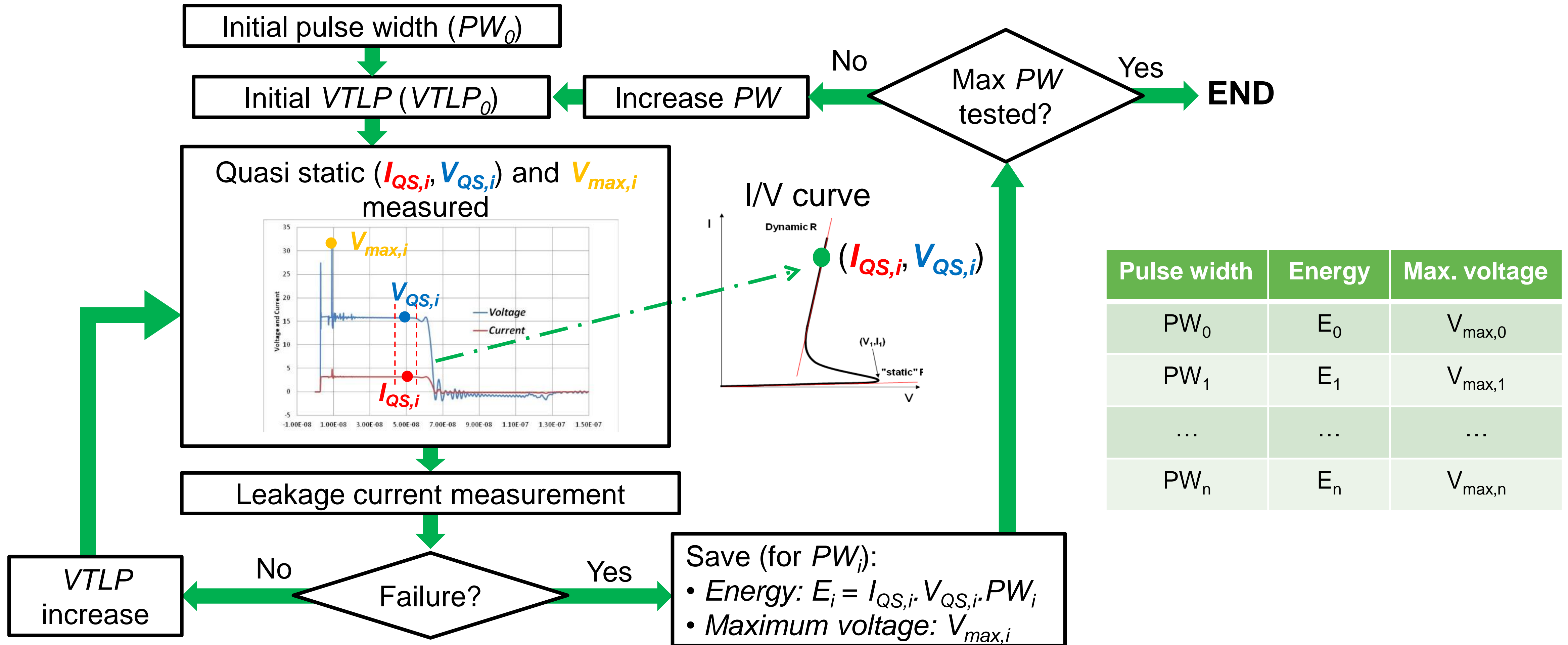
FB – FAILURE BEHAVIOUR

○ **FB contains the thresholds for different failure criteria associated to the performance classes (IEC 62215-3):**

- Class A_{IC}: All monitored functions of the IC perform within the defined tolerances during and after exposure to disturbance.
- Class B_{IC}: Short time degradation of one or more monitored signals during exposure to disturbance.
- Class C_{IC}: At least one of the monitored functions of the IC is out of the defined tolerances during exposure to the disturbance but it returns automatically to the defined tolerances after exposure to disturbance.
- Class D_{IC}: At least one monitored function of the IC does not perform within the defined tolerances during exposure to the disturbance and it does not return to normal operation by itself.
  - Class $D1_{IC}$: The IC returns to normal operation by manual intervention (e.g. reset)
  - Class $D2_{IC}$: The IC returns to normal operation by power cycling the device.
- Class E_{IC}: At least one monitored function of the IC does not perform within the defined tolerances after exposure and it can not be returned to proper operation.

FB – EXTRACTION

- **Steps for failure threshold extraction for class E_{IC} (destruction) → using TLP generator**



Pulse width	Energy	Max. voltage
PW_0	E_0	$V_{max,0}$
PW_1	E_1	$V_{max,1}$
…	…	…
PW_n	E_n	$V_{max,n}$

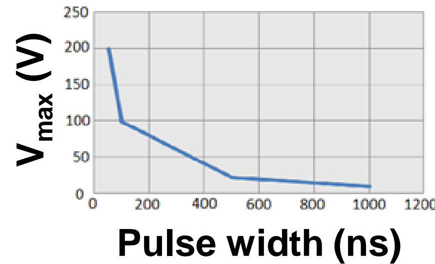
Valeo

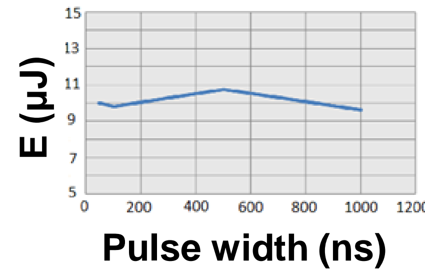
FB – DESTRUCTION CRITERION IDENTIFICATION

Pulse width	Energy	Max. voltage
PW_0	E_0	$V_{max,0}$
PW_1	E_1	$V_{max,1}$
…	…	…
PW_n	E_n	$V_{max,n}$

○ **E(PW) and V_{max}(PW) curves from characterization:**

Case 1

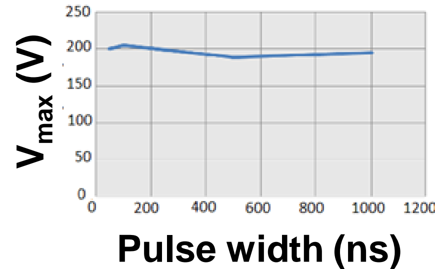


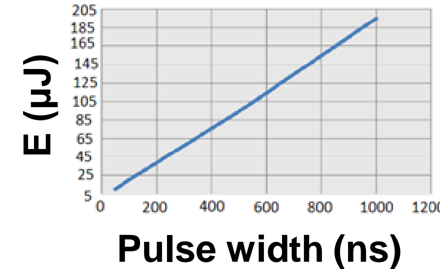


E(PW) is constant → **Energy (thermal) breakdown**

ex. Failure threshold: $E = 10\mu J$

Case 2

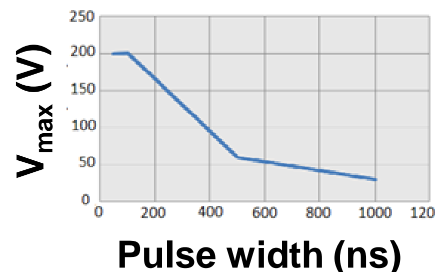


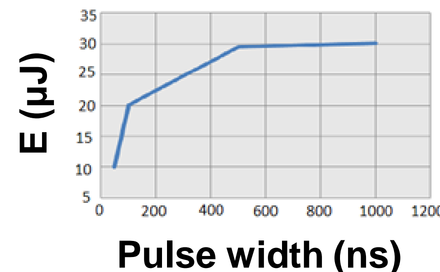


V_{max}(PW) is constant → **Overvoltage breakdown**

ex. Failure threshold: $V_{max} = 200V$

Case 3





V_{max}(PW) is constant for short *PW*

E(PW) is constant for large *PW*

Mix of overvoltage and energy breakdown

ex. Failure thresholds: $V_{max} = 200V$ and $E = 30\mu J$

FB – ALL PERFORMANCE CLASSES

- FB table for different performance classes

pulse characteristics at DI terminal				Pulse characteristics at OO terminal				
V_{MAX} (V)	V_{GS} (V)	I_{GS} (A)	Pulse width PW (ns)	Destruction Class E	Freeze Class D	Reset Class C	OUTPUT x	
							Glitch width (ns)	Voltage @state_0 (V)
< 30	< 5	< 5	< 20	No	No	No	< 20	>4
30	8	6	30	No	No	No	20	2.3
30	8	6	50	No	No	Yes	-	-
50	10	10	50	No	Yes	No	-	-
62	10	20	50	Yes	-	-	-	-
20	4	3	100	No	No	No	80	1
25	5	6	100	No	No	Yes	-	-
30	5	10	100	No	Yes	No	-	-
30	7	14	100	Yes	-	-	-	-

ICIM-CPI VALIDITY

- **Time domain**

- **An ICIM-CPI model has limited validity around the conditions in which it has been extracted:**
  - Power supply voltage range
  - Temperature range
  - Load conditions on the IC terminals

Valeo

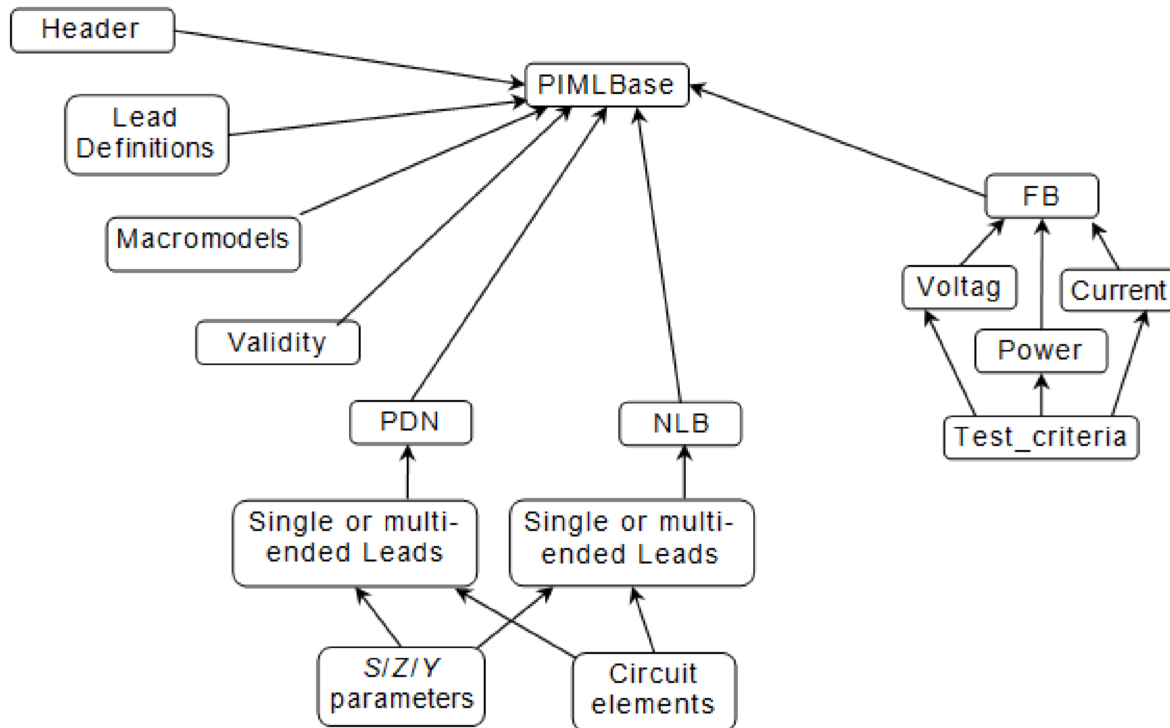
AIRBUS
GROUP

PIML FORMAT

PIML FORMAT - GENERAL

○ Pulse Immunity Markup Language: data exchange format for ICIM-CPI macro-model

- Based on XML format
- Uses IC_EMCML defined in IEC 62433-1.




```
<?xml version="1.0" encoding="UTF-8"?>
<PImodel>
<!-- HEADER -->
      <Header>
            ...
      </Header>

      <!-- DUT LEAD DEFINITIONS-->
      <Lead_definitions>
            ...
      </Lead_definitions>

      <!-- SPICE MACRO-MODEL DEFINITIONS -->
      <Macromodels>
            ...
      </Macromodels>

      <!-- MODEL VALIDITY CONDITIONS -->
      <Validity>
            ...
      </Validity>

      <!-- MODEL PDN DATA -->
      <Pdn>
            ...
      </Pdn>

      <!-- MODEL NLB DATA -->
      <Nlb>
            ...
      </Nlb>

      <!-- MODEL FB DATA -->
      <Fb>
            ...
      </Fb>
</PImodel>
```


Valeo

AIRBUS
GROUP

APPLICATION CASE

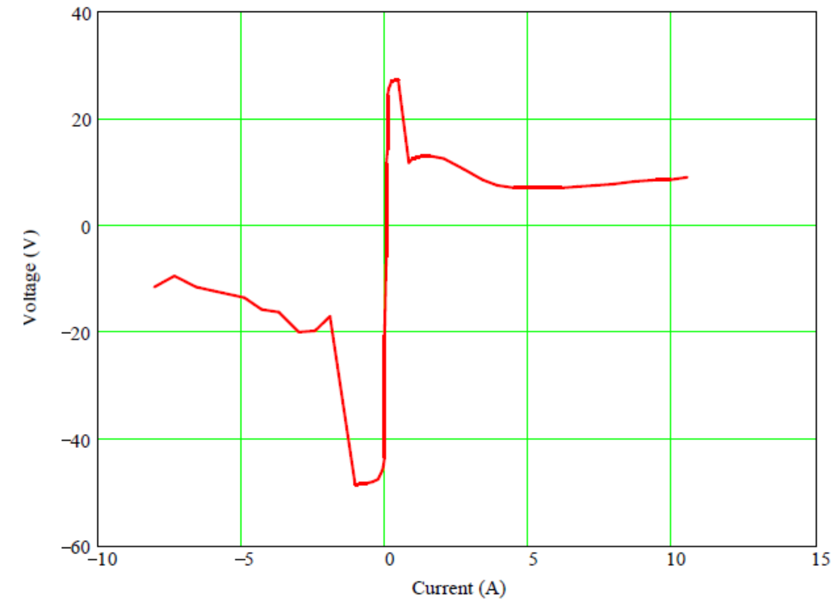
APPLICATION CASE

- The ICIM-CPI model can be used at equipment level in SPICE-like simulators considering external components such as protection capacitors, filter components, PCB trace parasitics, etc.

- For IC's destruction prediction, the user must monitor the simulated (V_{Max}, V_{QS}, I_{QS}) and compared them to the thresholds (FB).

- ICIM-CPI model of a Smart MOS
  - DI: OUT pin
  - NLB: I/V curve
  - FB: voltage breakdown (V_{max} = 225V)

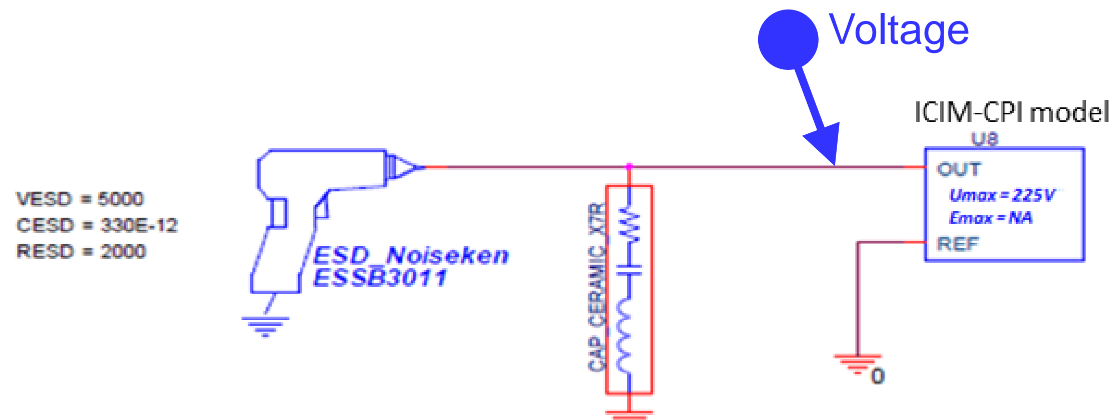
Test #	Pulse width (ns)	Quasi static current (A)	Quasi static voltage (V)	Peak voltage (V)	Energy (µJ)
1	100	12.7	11.3	225	14
2	500	11.7	12	220	70
3	1000	12.2	808	230	107

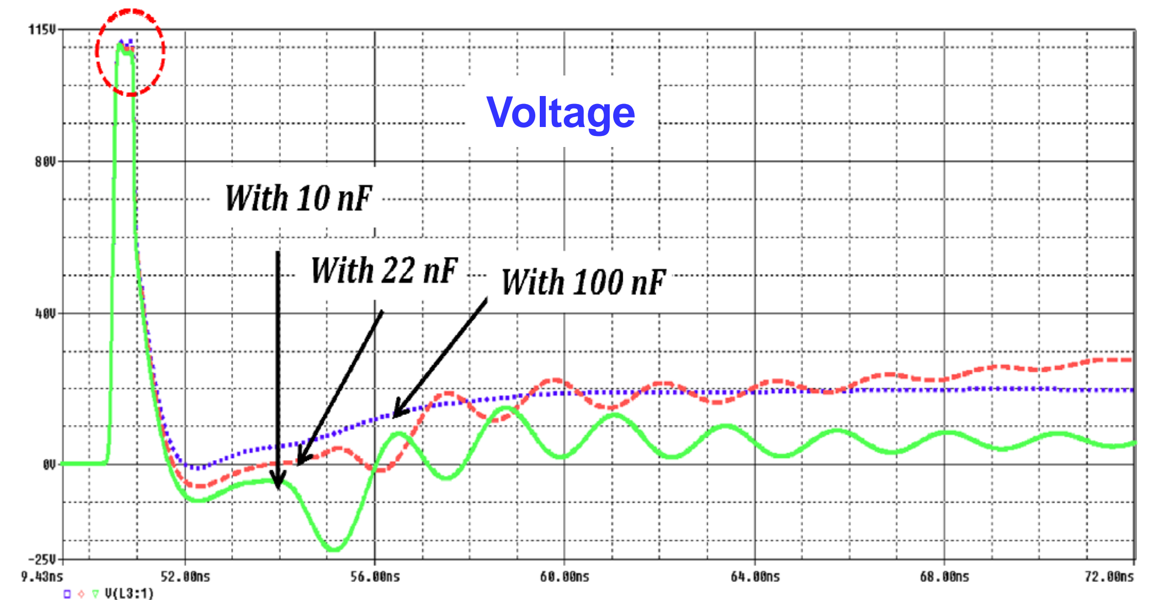


F. Lafon, A. Ramanujan, P. Fernandez-Lopez, "Black box model of integrated circuits for ESD behavioral simulation and industrial application case", Advanced Electromagnetics, vol. 4, no. 2, pp 26-37, November 2015.

APPLICATION CASE

- Two SmartMos are used to drive both car's fog lamps
  - Same schematic for right and left sides
- Differences in ESD robustness observed on both sides
- Simulation is used to understand the phenomenon



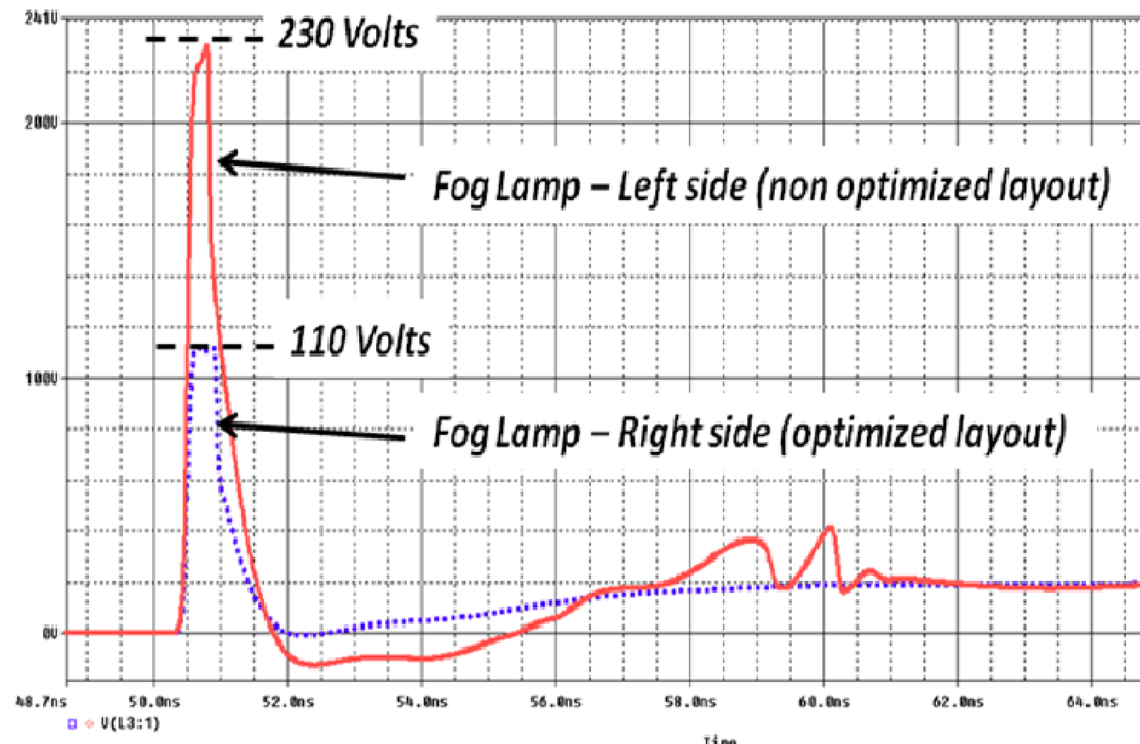


F. Lafon, A. Ramanujan, P. Fernandez-Lopez, "Black box model of integrated circuits for ESD behavioral simulation and industrial application case", Advanced Electromagnetics, vol. 4, no. 2, pp 26-37, November 2015.

APPLICATION CASE

○ **In order to explain the robustness difference between left and right sides → focus on the layout.**

- Capacitors on left side are not laid out on the direct trace → dedicated trace in series which induces ~4nH.



Vmax = 230V > 225V (FB)
Destruction risk on left side

Vmax = 110V < 225V (FB)
No destruction risk on right side

F. Lafon, A. Ramanujan, P. Fernandez-Lopez, "Black box model of integrated circuits for ESD behavioral simulation and industrial application case", Advanced Electromagnetics, vol. 4, no. 2, pp 26-37, November 2015.

AIRBUS
GROUP

CONCLUSIONS AND PERSPECTIVES

CONCLUSIONS AND PERSPECTIVES

- **A document describing the ICIM-CPI model is currently ongoing within IEC SC47A (Integrated Circuits) → IEC 62433-6.**

- **It consists in two parts:**
  - PPN which describes the pulse propagation network both linear (PDN) and non-linear (NLB) parts.
  - FB which contains the failure or destruction thresholds (PW, V_{QS}, I_{QS}, V_{Max}).

- **The PIML exchange format is also described.**

- **ICIM-CPI is currently at CD stage and it should go to CDV stage by the end of 2017.**

- **Target: to be published as an IEC standard in 2 years.**

Valeo

SMART TECHNOLOGY
FOR SMARTER CARS