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# Analysis and Comparison of Charge-Pump Conditioning Circuits for Capacitive Electromechanical Energy Conversion

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**Abstract**—This work presents a rigorous electrical analysis of charge-pump conditioning circuits for capacitive energy converters (CEG) with built-in bias voltage. The subsequent implications on the selection of the optimal conditioning circuit are also presented. In particular, the determining role of the application context and constraints on the optimal conditioning circuit choice is discussed. This context is defined by the transducer’s capacitance variation amplitude, by the value of the built-in bias of the transducer, and by limitations on the operating voltages across the circuit elements and the transducer.

## I. INTRODUCTION

Kinetic energy harvesting is a promising technology to convert mechanical energy from a system’s surrounding vibrations, to electrical energy for its autonomous operation. It can be achieved using capacitive energy converters (CEG). Such a converter can be seen in the electrical domain as a variable capacitor connected to a conditioning circuit. This variable capacitor is called the capacitive transducer. In capacitive energy conversion applications, this transducer can be charged by a built-in voltage, by the deposition of an electret layer [1]. The energy conversion occurs when the electrostatic force between the transducer’s plates opposes the movement induced by an external mechanical force on them. The conditioning circuit determines the evolution of the transducer’s biasing throughout the variation of its capacitance. Eventually, an interface circuit extracts the converted energy from the conditioning circuit and delivers it in a suitable form to the load.

Previous works [2] on conditioning circuits have shown that the family of charge-pump conditioning circuits (CPCC) is the most practical for use in CEG. This is because these circuits are inductor-less, and do not require synchronization with the mechanical input. However, most CPCC still lack analysis, particularly when combined to capacitive transducers with built-in bias. Notably, it is still unclear how the choice of a particular conditioning circuit among this family affects the rate of energy conversion for a given CEG.

This paper first reports the results of the analysis of four CPCCs joined to a built-in charged transducer, when its capacitance variation is considered as an input of the system.

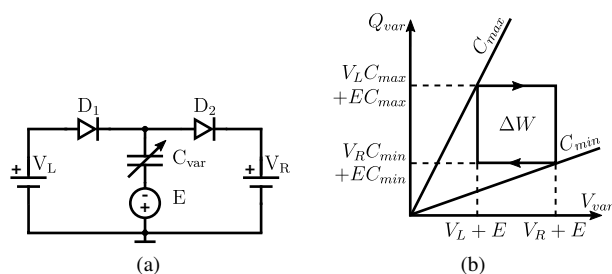


Fig. 1. (a) Generic charge-pump conditioning circuit for biasing a CEG with built-in bias (b) Corresponding charge-voltage diagram.

Based on these results, the maximum energy conversion rate of the different circuits are compared, for different application contexts and constraints. In Section II, the CPCC are presented. The circuit comparison is detailed in Section III.

## II. CHARGE-PUMP CONDITIONING CIRCUITS (CPCC)

Charge pump conditioning circuits (CPCC) are networks of capacitors and diodes driven by a time-varying capacitor. The transducer biasing schemes implemented by circuits of this family are qualitatively similar [3]. This biasing scheme is conceptually described by the circuit depicted in Fig. 1a. The capacitive transducer is modeled in the electrical domain as a variable capacitor  $C_{var}$ . The voltage source  $E$  represents the built-in potential of the transducer. This biasing scheme of the transducer can be summarized in the charge-voltage diagram depicted in Fig. 1b. The converted energy during a given cycle of  $C_{var}$ ’s variation is equal to the area of the rectangle in the QV diagram of that cycle. In the following, it will be referred to as the “converted power” for the sake of shortness.

The rectangular shape of the QV diagram is common to all CPCCs. At every cycle of the transducer’s capacitance variation,  $V_L$  and  $V_R$  depend on the internal energy of the circuit, i.e., the voltage across the CPCC’s fixed capacitors. The evolutions of  $V_L$  and  $V_R$  throughout  $C_{var}$ ’s variation cycles depend on the circuit’s internal energy. This dependence is different for each CPCC. It is fundamental to note that for each CPCC, the converted power is fully determined by

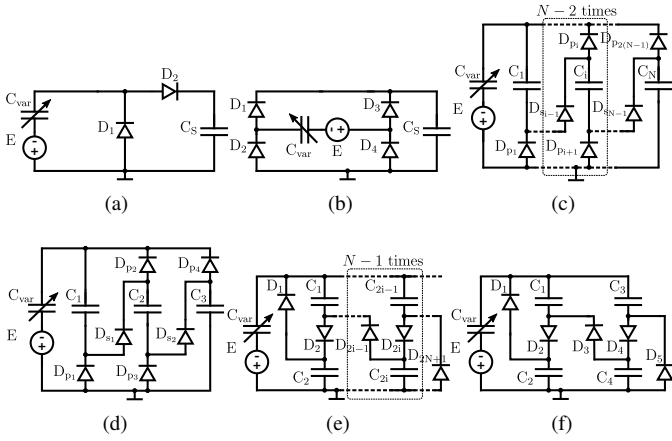


Fig. 2. (a) Half-wave CPCC (b) full-wave CPCC (c) Generic topology of the cycle-widening CPCC (d) Cycle-widening CPCC with  $N = 2$  (e) Generic topology of the cycle-offsetting CPCC (f) Cycle-offsetting CPCC with  $N = 3$

the voltages across its fixed capacitors. Hence, the converted power also evolves throughout  $C_{var}$ 's variation cycles.

In the subsections II-A to II-C, we present four different circuits of the CPCC family. For each circuit, expressions for the converted power are given. All the results are given for the circuits working in their steady-state mode of operation, with the transducer cyclically varying between maximum and minimum values  $C_{max}$  and  $C_{min}$ . For simplicity, the circuit elements are considered ideal. Let us also define  $\eta := C_{max}/C_{min}$ . The analysis is made in the electrical domain, that is,  $C_{var}$  is considered as an input of the system. Hence,  $\eta$  is supposed to be constant throughout each circuit's operation. Also, in all the following, it is supposed that  $C_{max}$  is much smaller than any of the CPCC's fixed capacitor. This is a fair assumption given the typical capacitance values of the transducers used in capacitive energy converters. The subsection II-D introduces a simple energy-extracting interface circuit for CPCCs.

#### A. Rectifier charge-pumps (HW and FW)

We first consider the CPCCs depicted in Fig. 2a and Fig. 2b. These CPCC are only used in the case of transducers with a built-in bias ( $E \neq 0$ ). Their topologies are close to traditional half-wave and full-wave rectifiers. Hence, in the following, these circuits will be referred to as the HW and FW conditioning circuits. The FW CPCC has been used for example in the CEG reported in [4].

The HW circuit implements, at each cycle of  $C_{var}$ 's variation, the generic QV diagram depicted in Fig. 1b. The characteristic voltages are  $(V_L, V_R) = (0, V_{S_n})$  where  $V_{S_n}$  is the voltage across  $C_S$  at cycle  $n$ . The QV cycle implemented by the FW circuit has characteristic voltages  $(V_L, V_R) = (-V_{S_n}, V_{S_n})$ . The HW and FW circuits exhibit saturation of their fixed capacitors voltages under  $C_{var}$ 's cyclical variation between  $C_{max}$  and  $C_{min}$ . Hence, a cycle with maximum converted power exists. This is illustrated on the simulation example depicted in Fig. 3a.

The maximum energy conversion cycles are obtained for

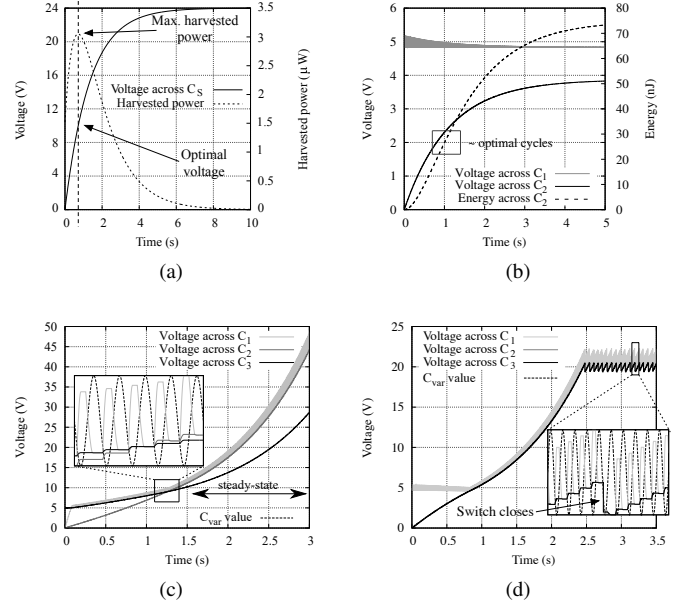


Fig. 3. Examples of simulations of CPCCs connected to an harmonically time-varying capacitance. (a) HW conditioning circuit (b) CW conditioning circuit showing saturation ( $N = 2$ ) (c) CW circuit with exponential converted power increase ( $N = 3$ ) (d) CW circuit with an energy-extracting interface

the following voltages on the capacitor  $C_S$  of HW and FW:

$$V_{opt}^{HW} = \frac{1}{2}E(\eta - 1), \quad \text{and} \quad V_{opt}^{FW} = \frac{1}{2}E\frac{\eta - 1}{\eta + 1}, \quad (1)$$

respectively. The corresponding maximum converted power, normalized by  $C_{min}$ , reads:

$$\frac{\Delta W_{opt}^{HW}}{C_{min}} = \frac{E^2(\eta - 1)^2}{4}, \quad \text{and} \quad \frac{\Delta W_{opt}^{FW}}{C_{min}} = \frac{E^2(\eta - 1)^2}{2(\eta + 1)}. \quad (2)$$

The HW and FW circuits are examples of saturating CPCCs, and both are used in the case. Note that there are saturating CPCCs that can work with transducers without pre-bias (such as the circuit reported in [5]).

#### B. Cycle-widening charge-pumps (CW)

A subset of CPCCs is based on the generic topology depicted in Fig. 2c. In the following, we shall refer to these circuits as the cycle-widening (CW) CPCCs. Unlike HW and FW circuits, these circuits can be used with transducers that have no built-in bias ( $E = 0$ ), as long as there is an initial energy in the circuit's capacitors.

Our analysis, fully-reported in [6], shows that these circuits implement the generic CPCC QV diagram depicted in Fig. 1b, with a constant ratio  $(V_R/V_L)_{CW}$  throughout the circuit's operation. Its value can be set to any rational number equal or greater than 2 by the choice of the circuit's elements and the number of branches:

$$\left(\frac{V_R}{V_L}\right)_{CW} = \Pi + \frac{1}{\Pi - 1} \sum_{i=1}^{\Pi} C_i \sum_{i=\Pi+1}^N C_i^{-1}, \quad \text{where} \quad (3)$$

$$\Pi := \min(\{p \in \mathbb{N} \mid 1; N \setminus \{ \text{such that } \Gamma(p+1) \} \cup \{N\} \}), \quad \text{and}$$

$$\Gamma(p) := \left\{ \sum_{i=1}^p C_i - (p-1)C_p > 0 \right\},$$

and where the fixed capacitors of the circuit are labeled such that  $C_1 \leq \dots \leq C_N$ . At any cycle  $n$  of  $C_{\text{var}}$ 's variation,  $V_{Ln} = \max_{1 \leq i \leq N}(V_{Cin})$ , where  $V_{Ln}$  is the circuit's characteristic voltage  $V_L$  at cycle  $n$  and  $V_{Cin}$  denotes the voltage across the capacitor  $C_i$  at cycle  $n$  of the transducer's capacitance variation.

The ratio is fixed if and only if  $(V_R/V_L)_{CW} < \eta$ . If this condition is fulfilled, the constant ratio implies that the energy accumulation process shows no saturation and grows exponentially with operation time, as depicted in the simulation example in Fig. 3c. Hence, in the absence of further voltage limitations, no maximum of converted power exists. Otherwise, if  $(V_R/V_L)_{CW} \geq \eta$  a saturating energy conversion scheme is implemented (as depicted in Fig. 3b).

The converted power for a given cycle  $n$  reads:

$$\frac{\Delta W_n^{CW}}{C_{min}} = V_{Ln} \left( \left( \frac{V_R}{V_L} \right)_{CW} - 1 \right) \times \left( V_{Ln} \left( \eta - \left( \frac{V_R}{V_L} \right)_{CW} \right) + E(\eta - 1) \right). \quad (4)$$

### C. Cycle-offsetting charge-pumps (CO)

Another subset of CPCCs is based on the generic topology depicted in Fig. 2e, notably reported in [7]. As for CW circuits, these circuits can be used with an unbiased transducer ( $E = 0$ ). In the following, these circuits will be referred to as the cycle-offsetting (CO) CPCCs.

These circuits implement the CPCC generic QV diagram depicted in Fig. 1b, with the constant ratio

$$\left( \frac{V_R}{V_L} \right)_{CO} = \frac{N + 1}{N} \quad (5)$$

throughout the circuit's operation, where  $N$  is set by the number of branches in the circuit. The fixed capacitors values have to be chosen as reported in [7]. As a result, the voltages  $V_R$  and  $V_L$  increase exponentially throughout the cycles of  $C_{\text{var}}$ 's variation. The subsequent energy conversion process is exponential, as for the CW CPCC. Hence, no maximum of converted power exists in the absence of further voltage limitations. This exponential mode holds as long as  $(V_R/V_L)_{CO} < \eta$ . Otherwise, a saturating energy conversion scheme is implemented. At any cycle  $n$  of  $C_{\text{var}}$ 's variation,  $V_{Ln} = \max_{1 \leq i \leq N}(V_{Cin})$ , where  $V_{Ln}$  is the circuit's characteristic voltage  $V_L$  at cycle  $n$  and  $V_{Cin}$  denotes the voltage across the capacitor  $C_i$  at cycle  $n$ .

The converted power is expressed as:

$$\frac{\Delta W_n^{CO}}{C_{min}} = NV_{Ln} \left( V_{Ln} \left( \eta - \left( \frac{V_R}{V_L} \right)_{CO} \right) + \frac{E}{N}(\eta - 1) \right). \quad (6)$$

Finally, note that a different generic topology implementing the same biasing scheme is reported in [8].

### D. Energy-extracting and load interface circuit

In applications, an energy-extracting interface is needed in conjunction with the CPCC. Its role is to extract energy from the conditioning circuit whilst sustaining a maximum

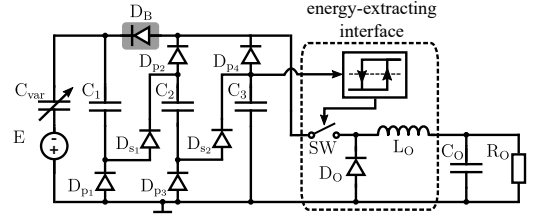


Fig. 4. Energy-extracting interface connected to a cycle-widening circuit.

energy conversion point. This is done by controlling one of the characteristic voltages  $V_R$  and  $V_L$  of the CPCC. For example, this can be limiting one of the characteristic voltages  $V_R$  and  $V_L$  to  $V_{max}^T$  or  $V_{max}^S$ , defined and discussed in Section III.

To fulfill this task, a simple implementation of such an interface is depicted in Fig. 4, in conjunction with the CW circuit with  $N = 3$  as an example. This interface implements a voltage comparison with hysteresis. The voltage across the capacitor  $C_3$  is compared with a fixed voltage  $V_{comp}$ , closing and opening the switch accordingly. In this way, the converted energy is transferred from the conditioning circuit to the output or storage capacitor  $C_O$ . An illustrating example is given in the simulations results depicted in Fig. 3d.

Note that in Fig. 4, the CW circuit is slightly modified (see Section III-B). The diode  $D_B$  is added to reduce the voltage across the switch of energy-extracting interface.

## III. COMPARISON OF THE CHARGE-PUMP CONDITIONING CIRCUITS

In the following, the studied conditioning circuits are compared in terms of maximum converted power, as a function of the application context defined by  $(\eta, E, V_{max})$ , where  $V_{max}$  represents one of two different limitations. The first possible limitation is on the maximum allowed voltage across the transducer. The second is a limitation on the maximum allowed voltage across the CPCC's interface switch. Note that in practice, the two constraints always exist (e.g., for technological reasons). For simplicity, the two cases are investigated separately in subsections III-A and III-B.

If none of the aforementioned limitations existed, the circuits with exponential converted power increase (CO and CW) could lead to arbitrarily high converted power values after a sufficiently long operation time. In particular, using the CO circuit with  $N$  sufficiently large such that  $(N + 1)/N < \eta$  would guarantee that an exponential steady-state mode of energy conversion will be reached.

### A. Voltage limitation across the transducer

Suppose that there exists a limitation  $V_{max}^T$  on the voltage across the transducer. This corresponds to the maximum allowable voltage across the dipole  $\{C_{\text{var}} + E\}$ .

Let us first compare the HW and FW circuits. The following is derived from the expressions of maximum converted power in (2), and from the converted power at  $V_S = V_{max}^T$ . This latter quantity is the QV diagram area at  $V_S = V_{max}^T$  for both circuits. If  $V_{opt}^{HW}, V_{opt}^{FW} > V_{max}^T$ , then the FW circuit yields

a higher converted power when  $V_{max}^T/E > (\eta - 1)/(2\eta + 1)$ . In every other configuration of  $V_{opt}^{HW}$ ,  $V_{opt}^{FW}$  and  $V_{max}$ , the HW circuit yields a higher converted power.

Let us now geometrically derive the optimal cycle for energy conversion under the  $V_{max}^T$  limitation, for constant  $V_R/V_L$  ratio CPCCs. Consider a rectangle that has two sides parallel to the V-axis, and whose right side is located in an interval  $]0; L]$  on the V-axis. Consider that, as for the QV diagram represented in Fig. 1b, the bottom right and upper left edges of the rectangle are located on the lines  $Q = C_{max}V$  and  $Q = C_{min}V$ , respectively. It can be shown that the rectangle with largest area having these properties is the one whose right side is at  $V = L$  and left side at  $V = (\eta + 1)/2\eta \cdot L$ .

From these results, setting  $L = V_{max}^T + E$ , it comes that a CPCC implementing a fixed  $V_R/V_L$  ratio can maximize the converted power when:

$$\frac{V_{max}^T + E}{((V_R/V_L)_{opt})^{-1}V_{max} + E} = \frac{2\eta}{\eta + 1}, \text{ and } V_R = V_{max}^T$$

$$\Rightarrow \begin{cases} \left(\frac{V_R}{V_L}\right)_{opt} &= \frac{2V_{max}^T\eta}{V_{max}^T(\eta+1) - E(\eta-1)}, \\ V_R &= V_{max}^T. \end{cases} \quad (7)$$

The second condition can always be fulfilled by a circuit operating in an exponential mode, because of the non-saturating voltages across their fixed capacitors. This holds as long as  $E \neq 0$ , or if there is an initial energy in the CPCCs capacitors. If  $(V_R/V_L)_{opt} \geq 2$ , then a CW circuit (including the Bennet's doubler) has to be used to implement the optimal cycle, using (3) to choose the capacitors so as to implement the desired ratio. Otherwise, if  $(V_R/V_L)_{opt} < 2$ , then a CO circuit has to be used. In this case, it is hard to accurately tune the value of  $(V_R/V_L)_{CO}$  to its optimal value, because only ratios of the form  $(N + 1)/N$  for integer  $N$  can be implemented. In both cases, it has to be checked whether the condition  $(V_R/V_L)_{opt} < \eta$  is fulfilled. Also, remark that if  $V_{max}/E \leq (\eta - 1)/(\eta + 1)$ , then  $V_{max}^S$  is too restrictive to implement the optimal cycle obtained from the geometrical argument above, and the cycle has to be adjusted. Finally, it should be noted that increasing the number of branches in the CO and CW circuits increases the losses in the circuit's elements in a non-idealized system, because of the multiplication of circuit branches. This can affect the optimal converted power of the circuit.

### B. Voltage limitation on the interface

Suppose that there exists a limitation  $V_{max}^S$  on the voltage across the switch SW of the energy-extracting circuit. For simplicity, we will suppose that the node of the switch connected to the inductor is at zero potential. This is a fair assumption as the voltage at the load side is supposedly much lower than the voltages across the conditioning circuit.

It can be seen immediately that an energy extracting interface for HW and FW circuits will be biased at most by their respective characteristic voltage  $V_R$ , as  $C_S$  is the sole energy reservoir for these circuits. For the CO conditioning circuit, it can be shown that the switch has to be connected to

the non-ground transducer node in order to extract energy at the rate it is converted. Hence, it will also be biased at most by the circuit's characteristic voltage  $V_R$  during its operation. Therefore, for these circuits, the comparison is the same as what is done in Section III-A, with  $V_{max}^T = V_{max}^S$ .

For the CW circuit, when the diode  $D_B$  is added as depicted in Fig. 4, the interface circuit can extract energy from all the capacitors, except  $C_1$ . This does not have an impact on the amount of extracted energy if  $C_1$  is chosen small enough. The presence of  $D_B$  ensures that the switch is biased at most by  $V_L$ . Hence, if the condition  $(V_L/V_R)_{CW} < \eta$  is verified, it gives a larger converted power than the other circuits. From a geometrical argument similar to the one in Section III-A, the optimal  $V_R/V_L$  ratio can be derived:

$$\begin{cases} \left(\frac{V_R}{V_L}\right)_{opt} &= \frac{V_{max}^S(\eta+1)+E(\eta-1)}{2V_{max}^S}, \\ V_L &= V_{max}^S. \end{cases} \quad (8)$$

The second condition can always be fulfilled when the circuit operates in its exponential mode, i.e., if  $(V_R/V_L)_{CW} < \eta$ . Note that it can be shown that even operating in its saturation mode, the CW circuit is still advantageous over the three other circuits for a wide range of  $(\eta, E, V_{max})$  parameters.

## IV. CONCLUSION

The paper reported results from the analysis of various charge-pump conditioning circuits for capacitive energy conversion using pre-charged transducers. These results were used to compare the different circuits under different application constraints. Further work will have to include the impact of the electromechanical coupling in this comparison, as it can have a large impact on the system's dynamics [9].

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