Embedding Crypto in SoCs: Threats and Protections

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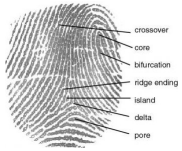
GDR SoC'17, Bordeaux

Summary

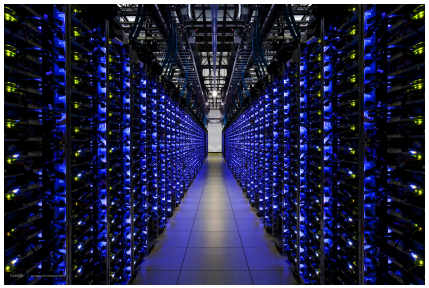
- Introduction & Cryptographic Background
- Side Channel Attacks
- Fault Injection Attacks
- Protections Examples
- Conclusion and References

Applications with Security Needs













Applications: smart cards, computers, Internet, telecommunications, set-top boxes, data storage, RFID tags, WSN, smart grids...

Cryptographic Features

Objectives:

- Confidentiality
- Integrity
- Authenticity
- Non-repudiation
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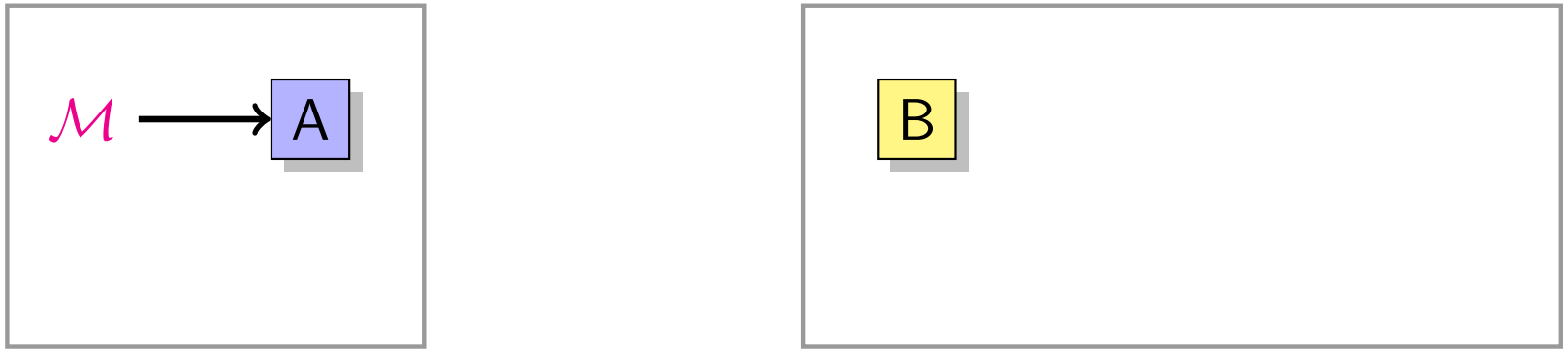
Implementation issues:

- Performances: speed, delay, throughput, latency
- Cost: device (memory, size, weight), low power/energy consumption, design
- Security: protection against attacks

Symmetric / Private-Key Cryptography



- A : Alice, B : Bob
- $\mathcal{M}$: plain text/message

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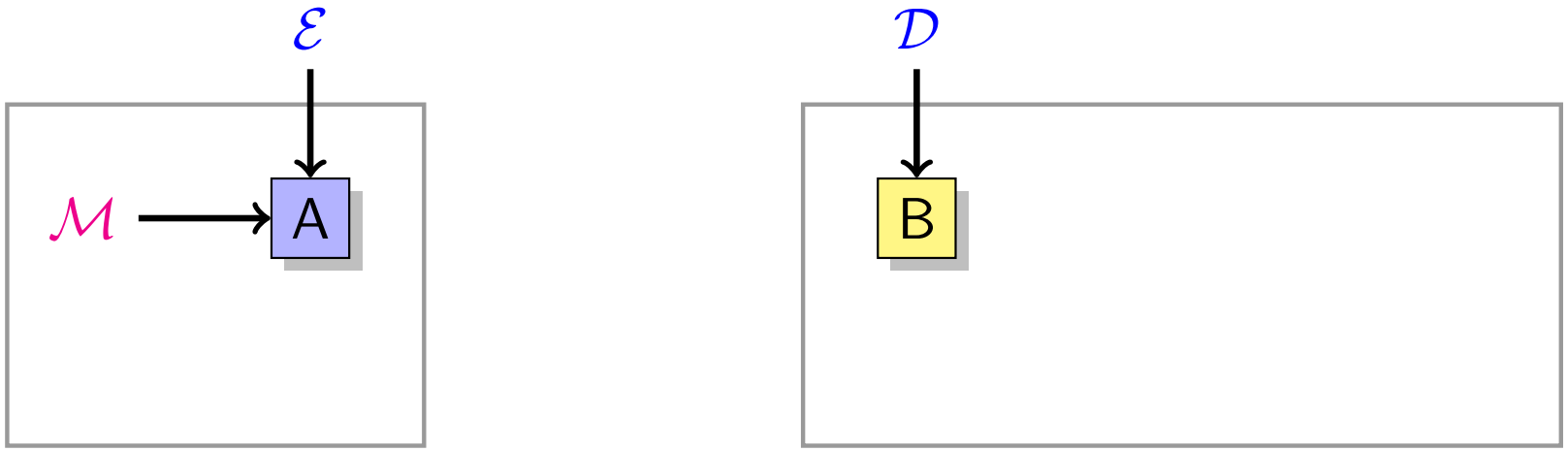

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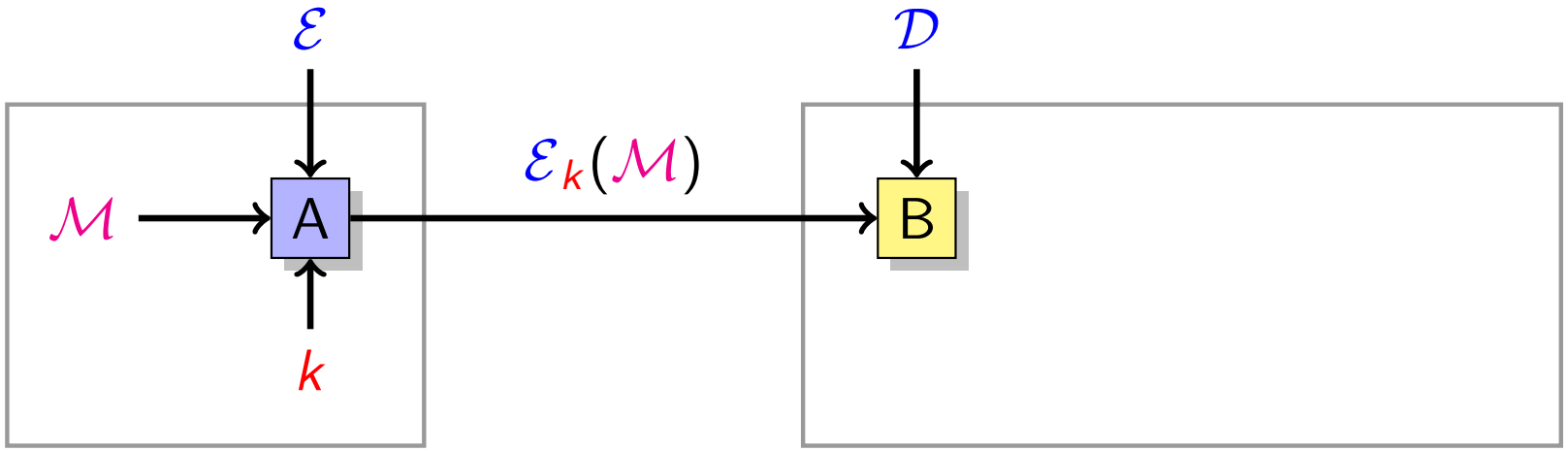

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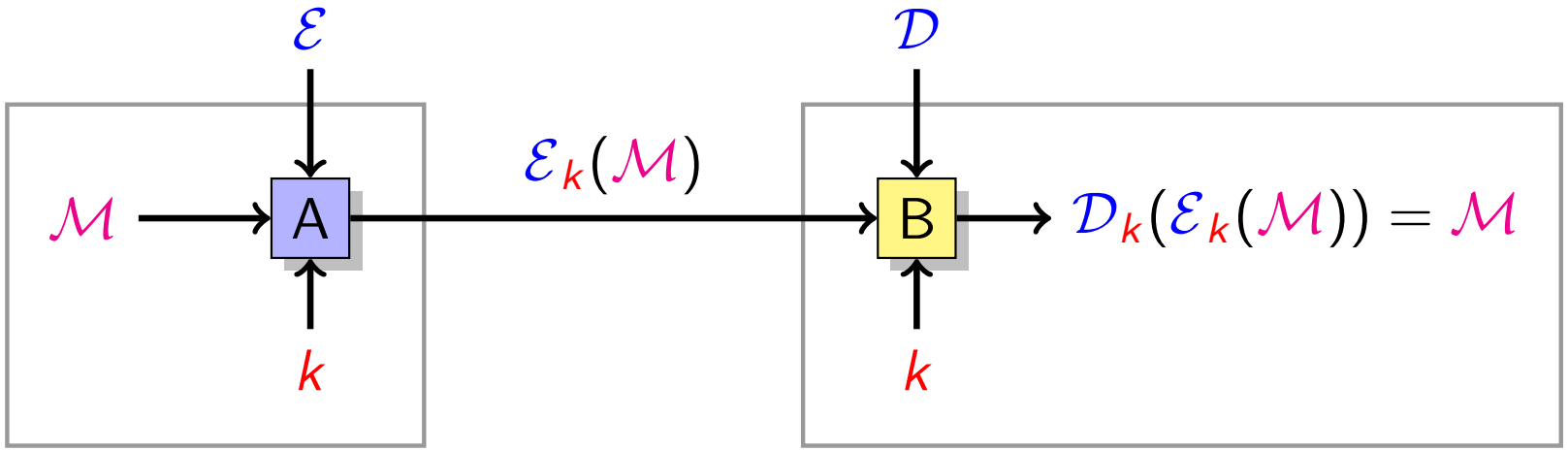

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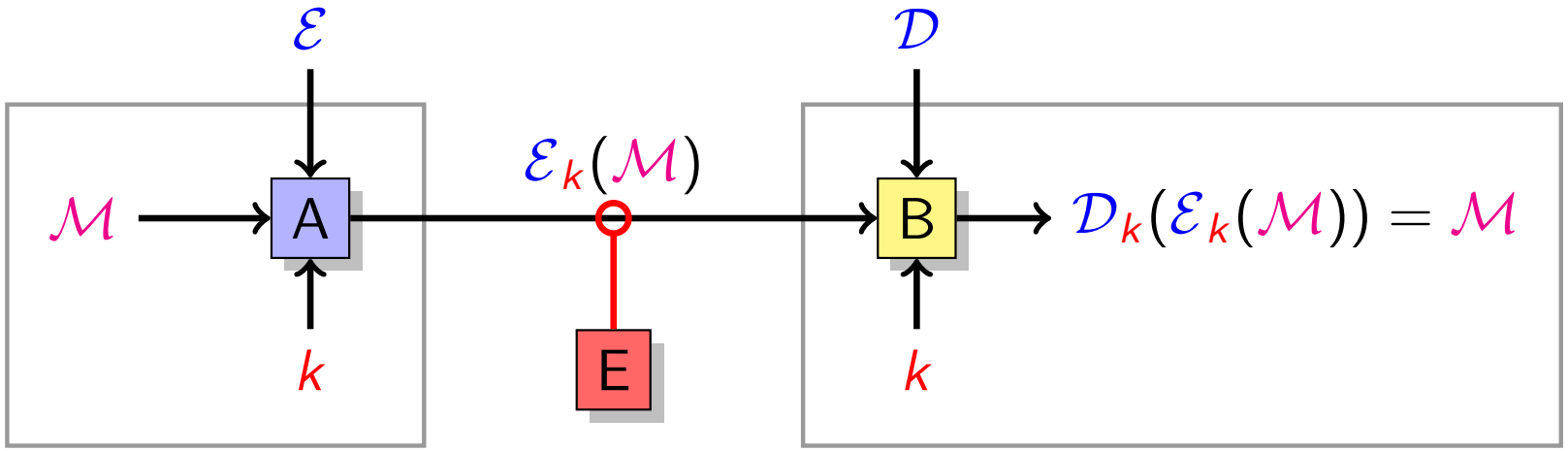

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- E : eavesdropper/spy

Advanced Encryption Standard (AES)

Established by NIST in 2001

Symmetric encryption

Block size: 128 bits

key length	#round
128	10
192	12
256	14

Based on substitution-permutation network

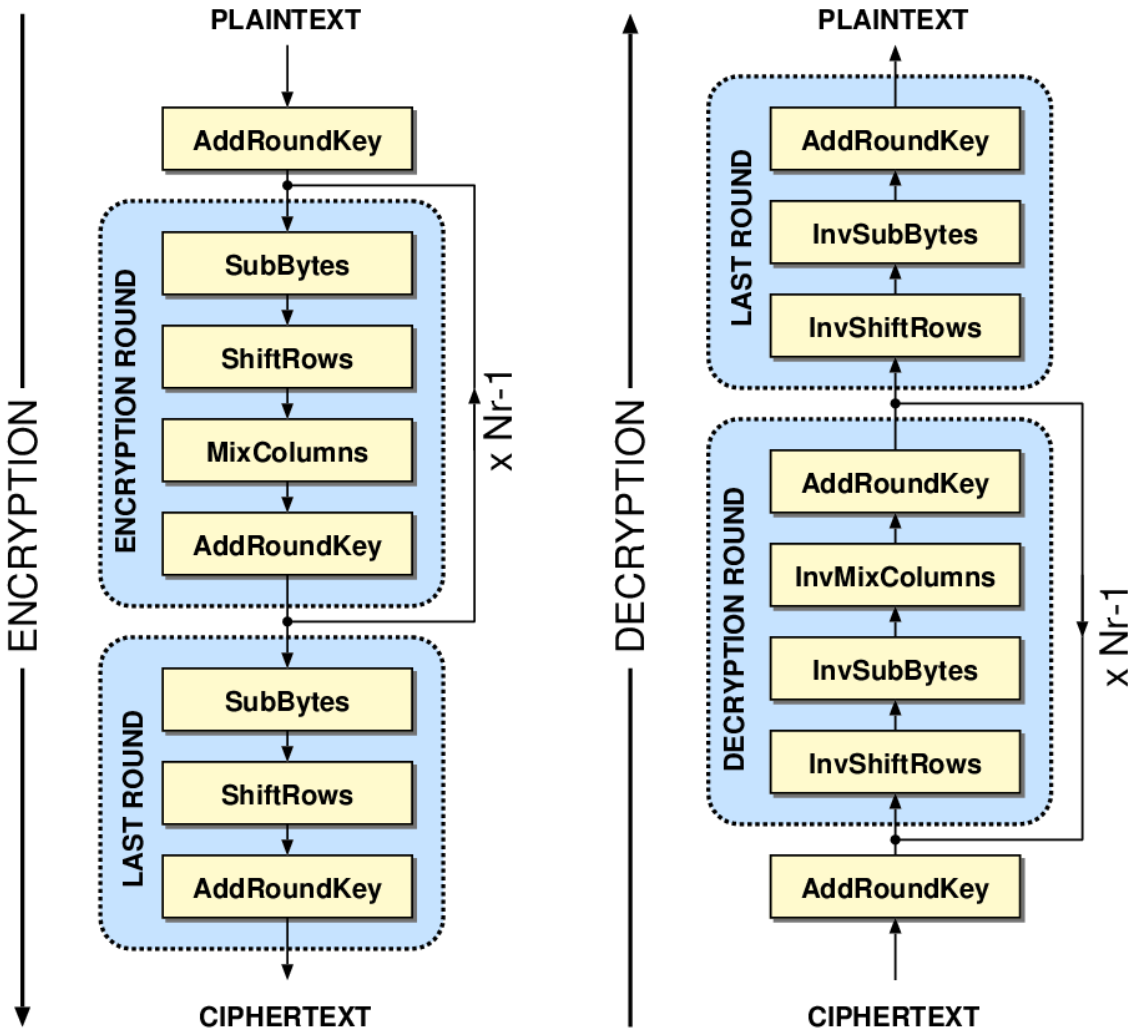
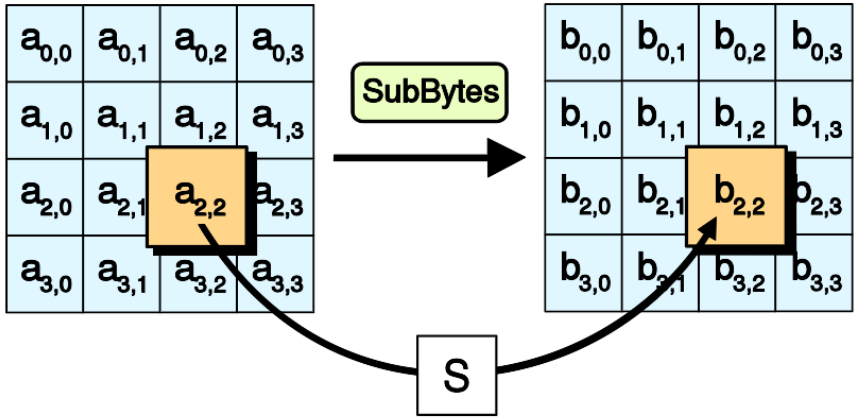
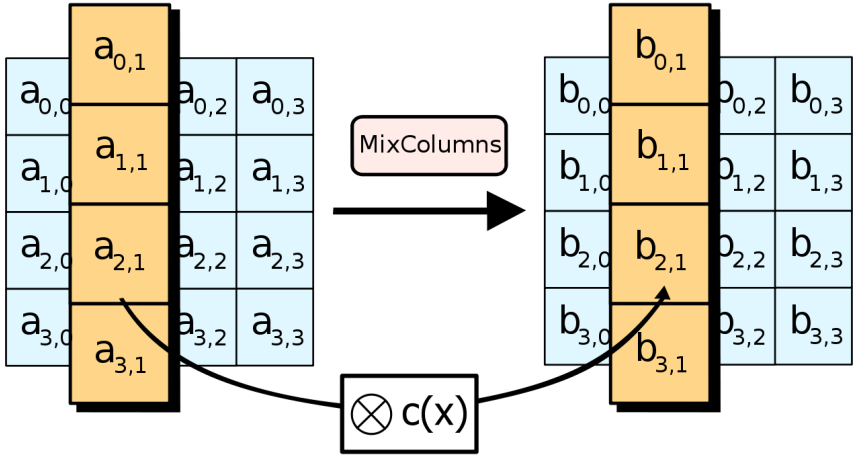


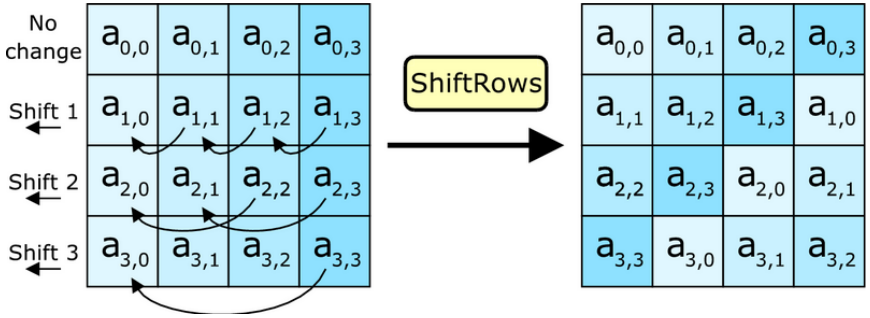
Image source: `http://fr.wikipedia.org/`

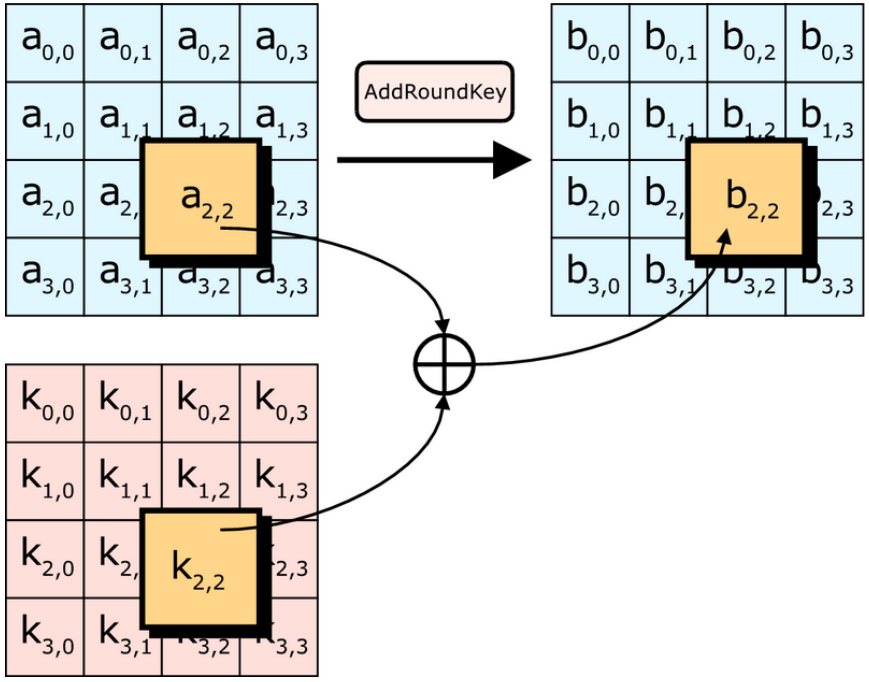
NIST: National Institute of Standards and Technology

AES Round Operations









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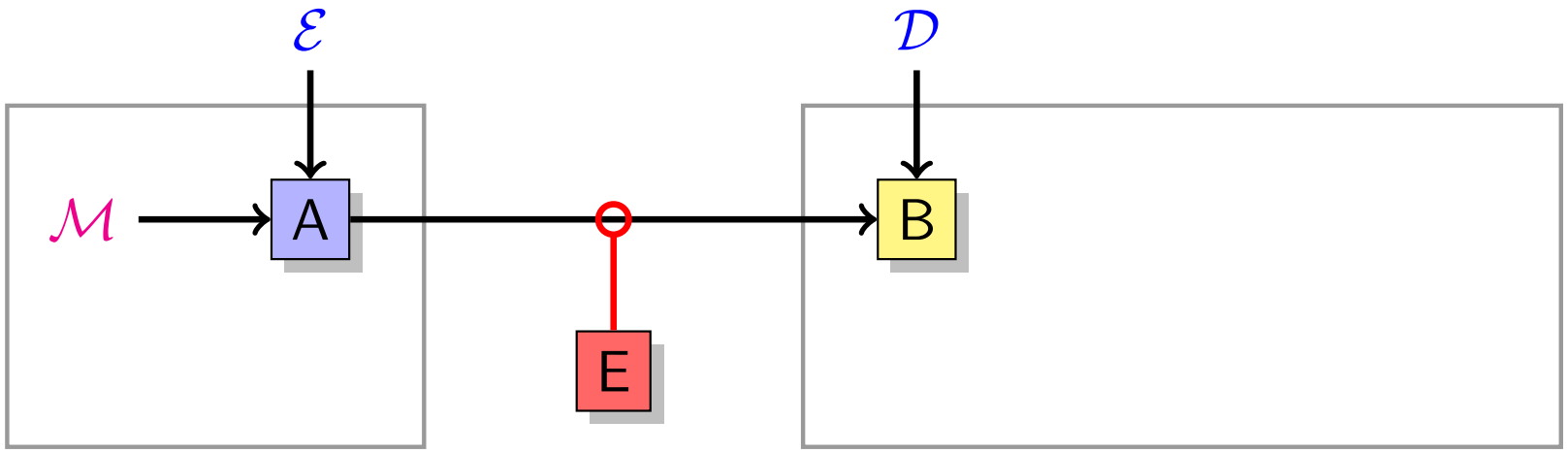

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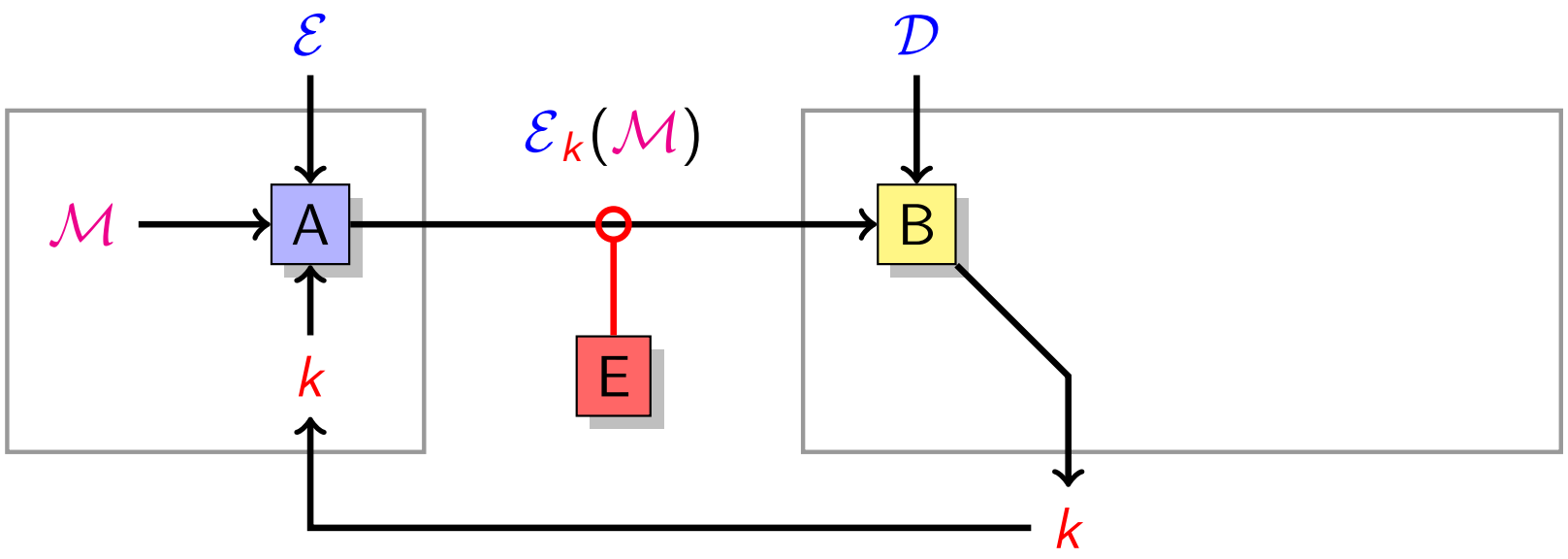

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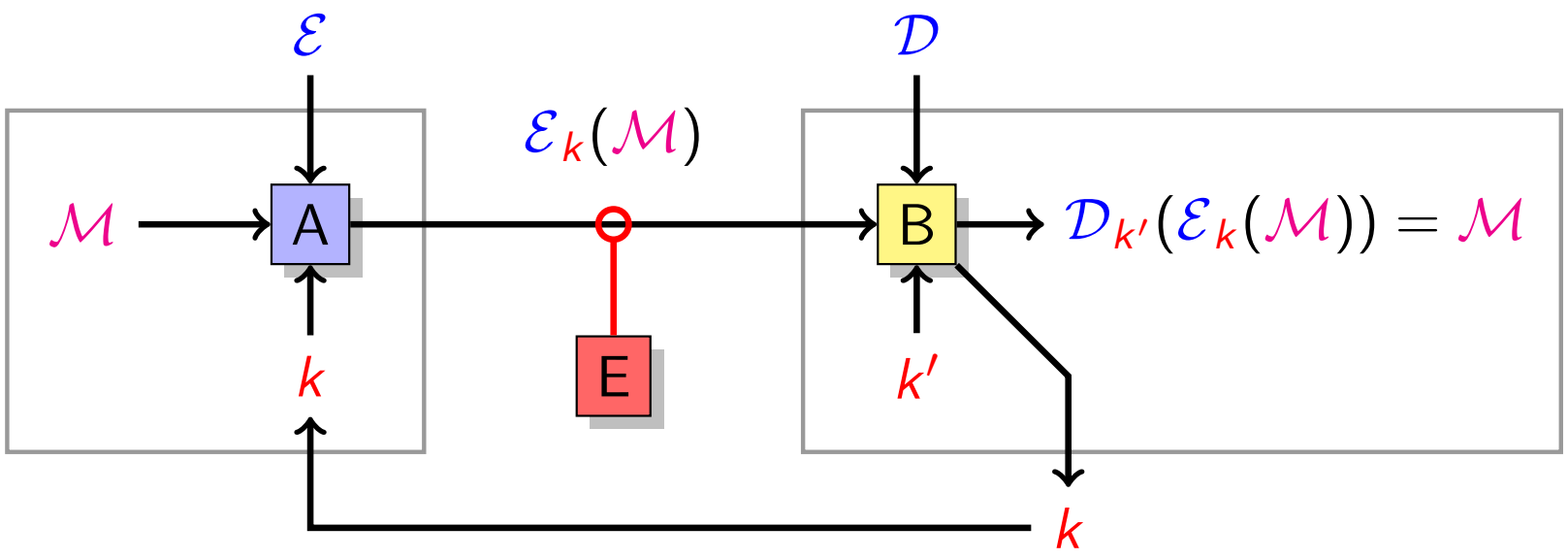

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- k': B's private key (must be kept secret)
- $\mathcal{D}_{k'}(\mathcal{E}_k(\mathcal{M}))$: deciphered text

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Published in 1978 by Ron Rivest, Adi Shamir and Leonard Adleman [17]

Key generation (Alice side)

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- Private key (kept secret by Alice): d and also $p, q, \varphi(n)$
- Public key (published): (n, e)

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Theoretical security: integer factorization, *i.e.* computing (p, q) knowing n, is not possible when n is large enough

Modular Exponentiation

Computation of operations such as : $a^b \bmod n$

$$a^b = \underbrace{a \times a \times a \times a \times \ldots \times a \times a \times a}_{a \text{ appears } b \text{ times}}$$

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Fast exponentiation principle:

$$\begin{aligned} a^b &= (a^2)^{\frac{b}{2}} && \text{when } b \text{ is even} \\ &= a \times (a^2)^{\frac{b-1}{2}} && \text{when } b \text{ is odd} \end{aligned}$$

Least significant bit of the exponent: $\texttt{bit} = 0 \rightsquigarrow$ even and $\texttt{bit} = 1 \rightsquigarrow$ odd

Square and Multiply Algorithm

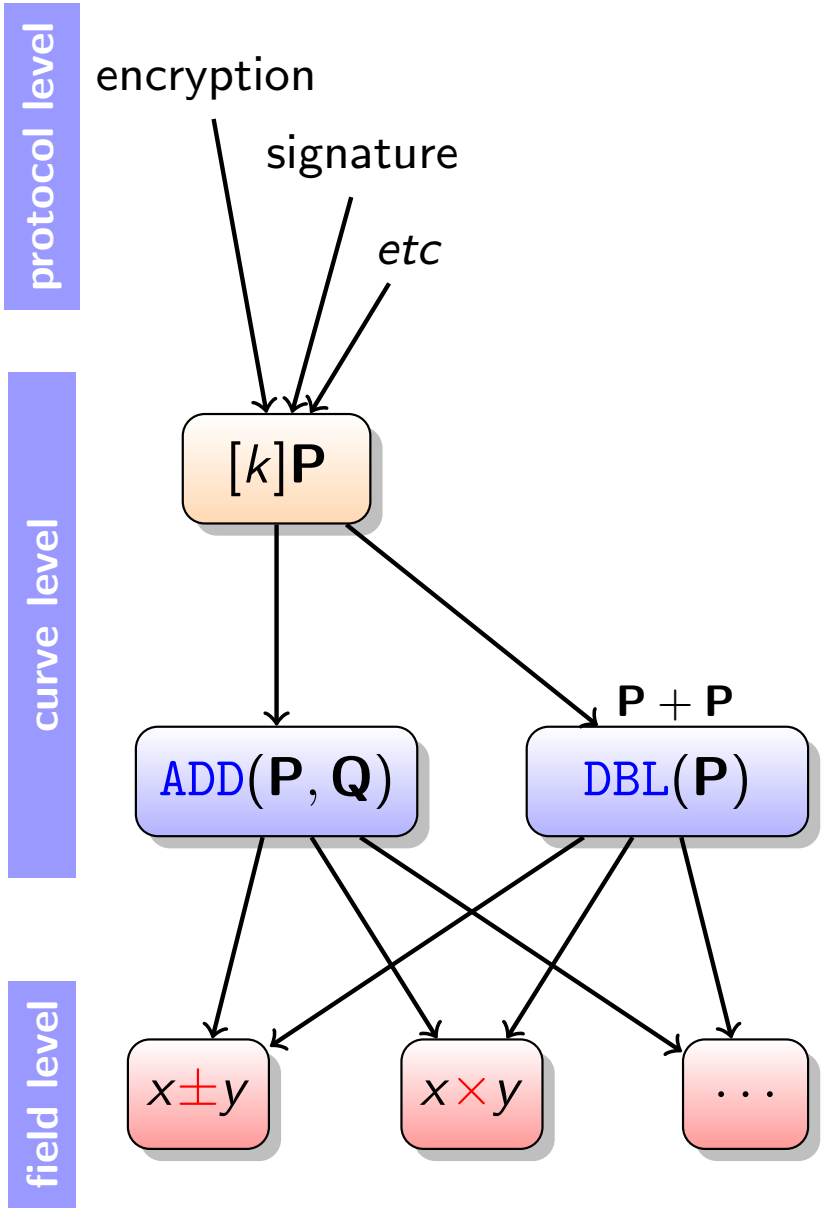
input: a, b, n where $b = (b_{t-1} b_{t-2} \ldots b_1 b_0)_2$

output: $a^b \bmod n$

$r = 1$
for i **from** 0 **to** $t-1$ **do**
  if $b_i = 1$ **then**
    $r = r \cdot a \mod n$
  endif
  $a = a^2 \mod n$
endfor
return r

This is the right to left version (there exists a left to right one)

Hardware Accelerators for Elliptic Curve Crypto.



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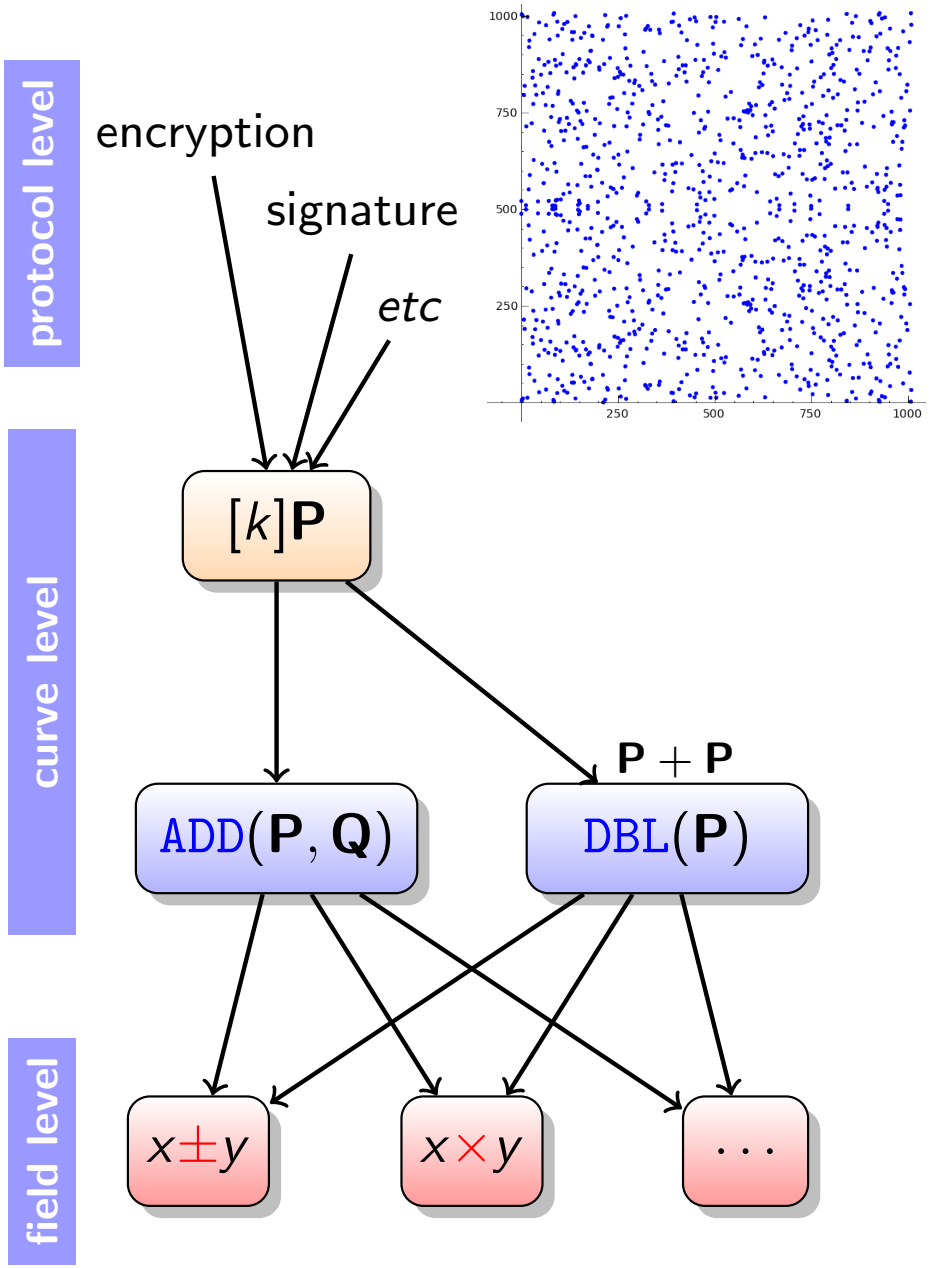

$E : y^2 = x^3 + 4x + 20$ over GF(1009)

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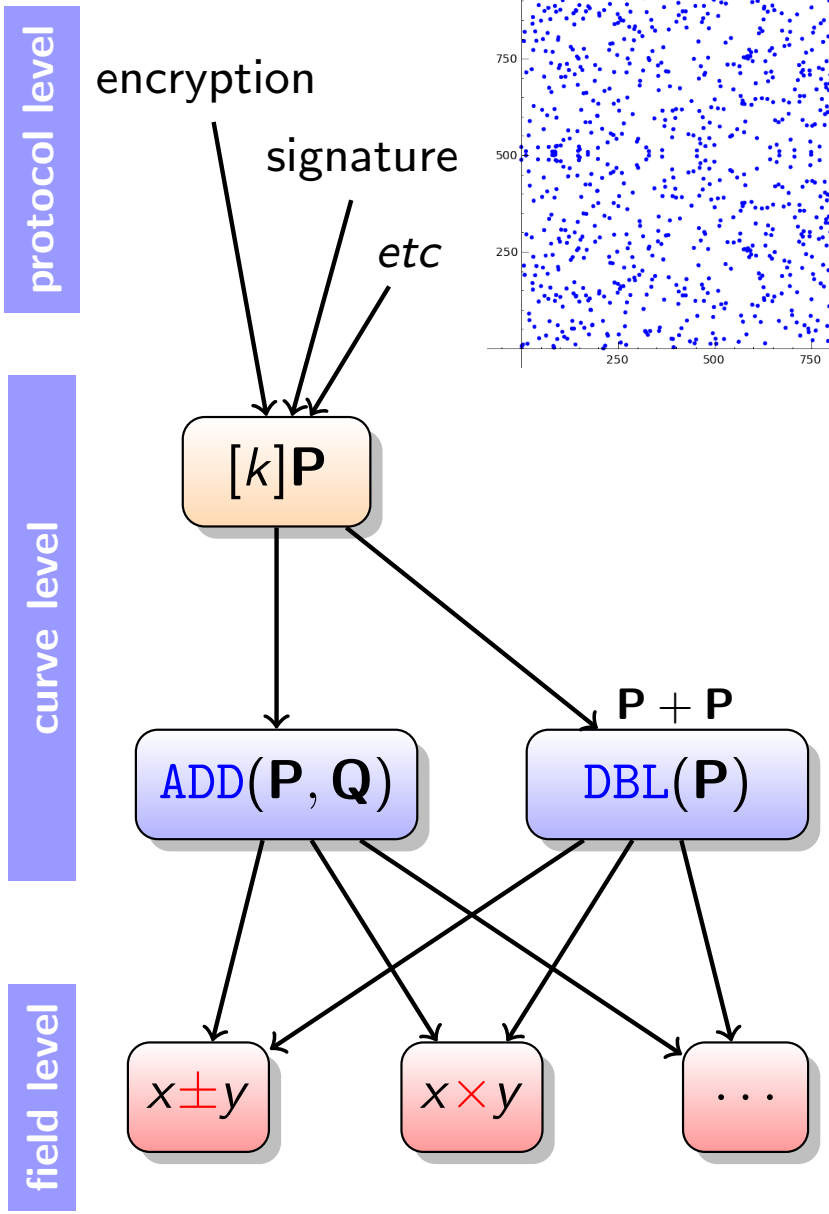

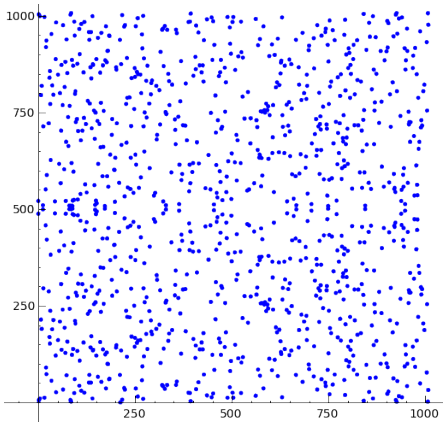

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coordinates: $x, y, z \in \mathrm{GF}(\cdot)$

$\mathrm{GF}(p)$, $\mathrm{GF}(2^m)$, t : 200–600 bits

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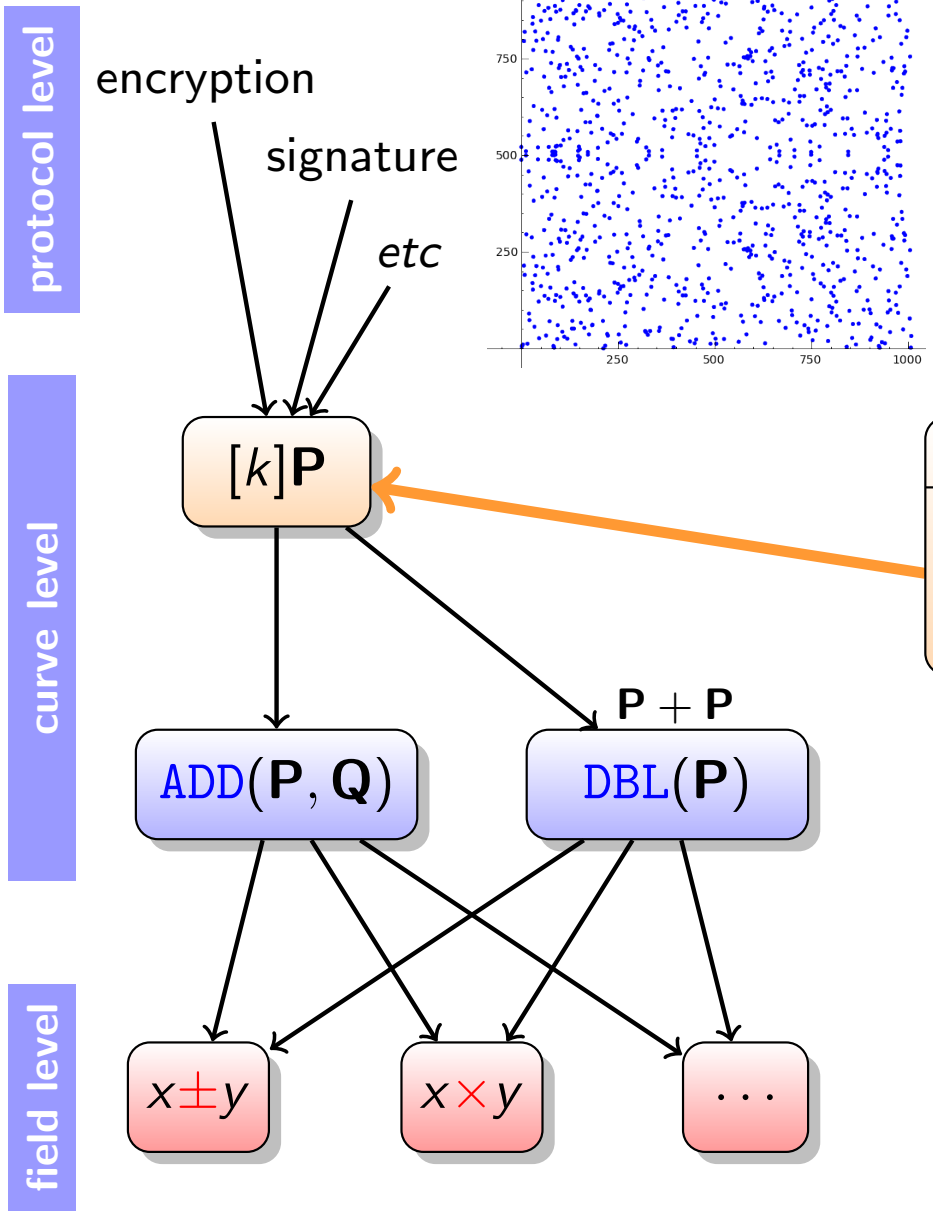

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```
for i from 0 to t − 1 do
    if k_i = 1 then Q = ADD(P, Q)
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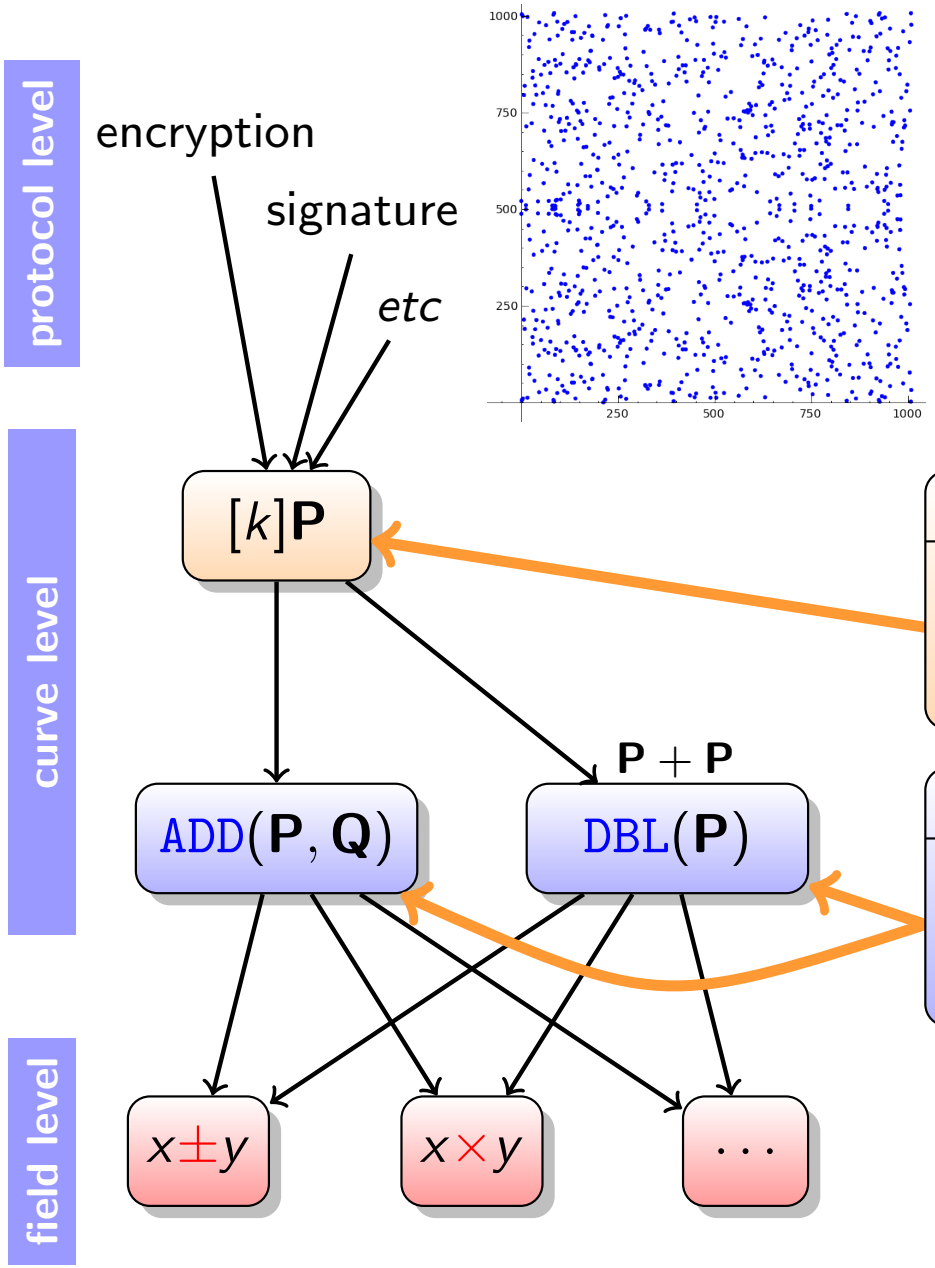

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Point addition/doubling operations

sequence of finite field operations

DBL: $v_1 = z_1^2, v_2 = x_1 - v_1, \ldots$

ADD: $w_1 = z_1^2, w_2 = z_1 \times w_1, \ldots$

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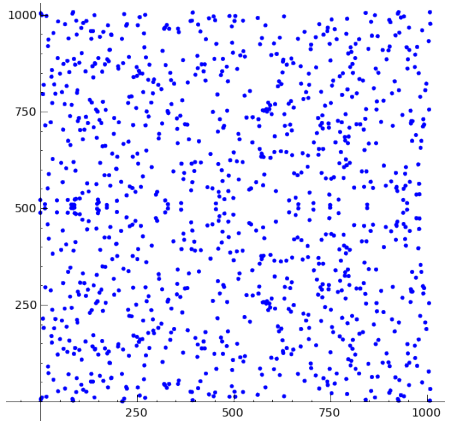

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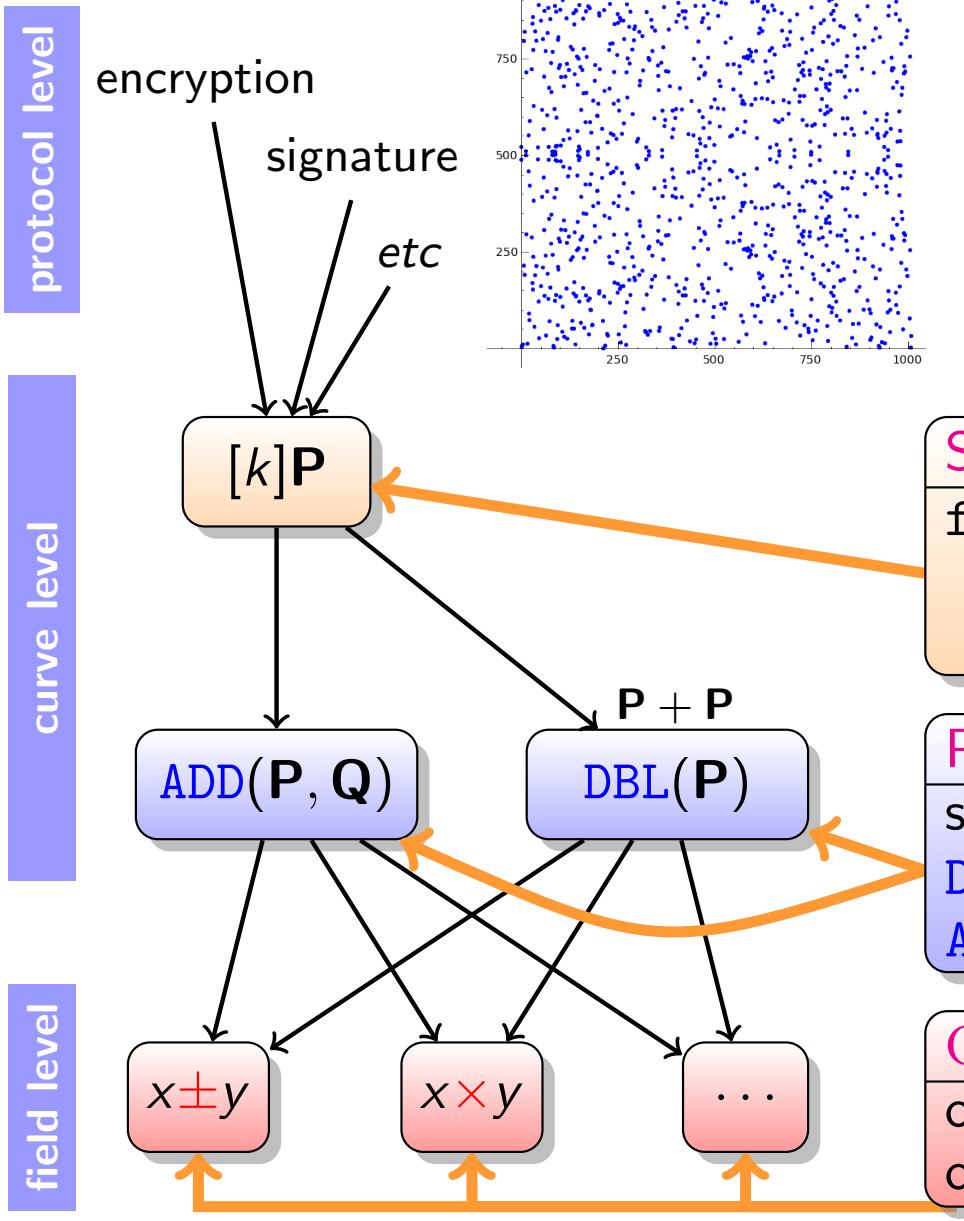

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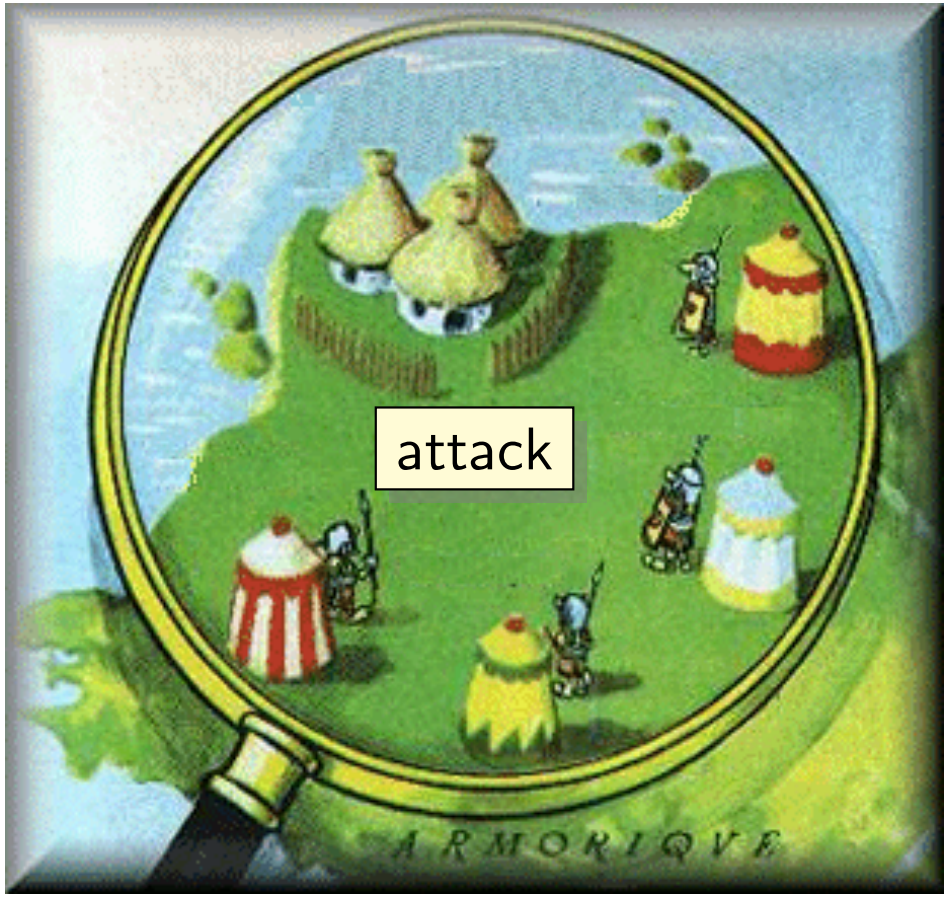
$\mathrm{GF}(p)$ or $\mathrm{GF}(2^m)$ operations

operation modulo large prime ($\mathrm{GF}(p)$) or irreducible polynomial ($\mathrm{GF}(2^m)$)

Attacks



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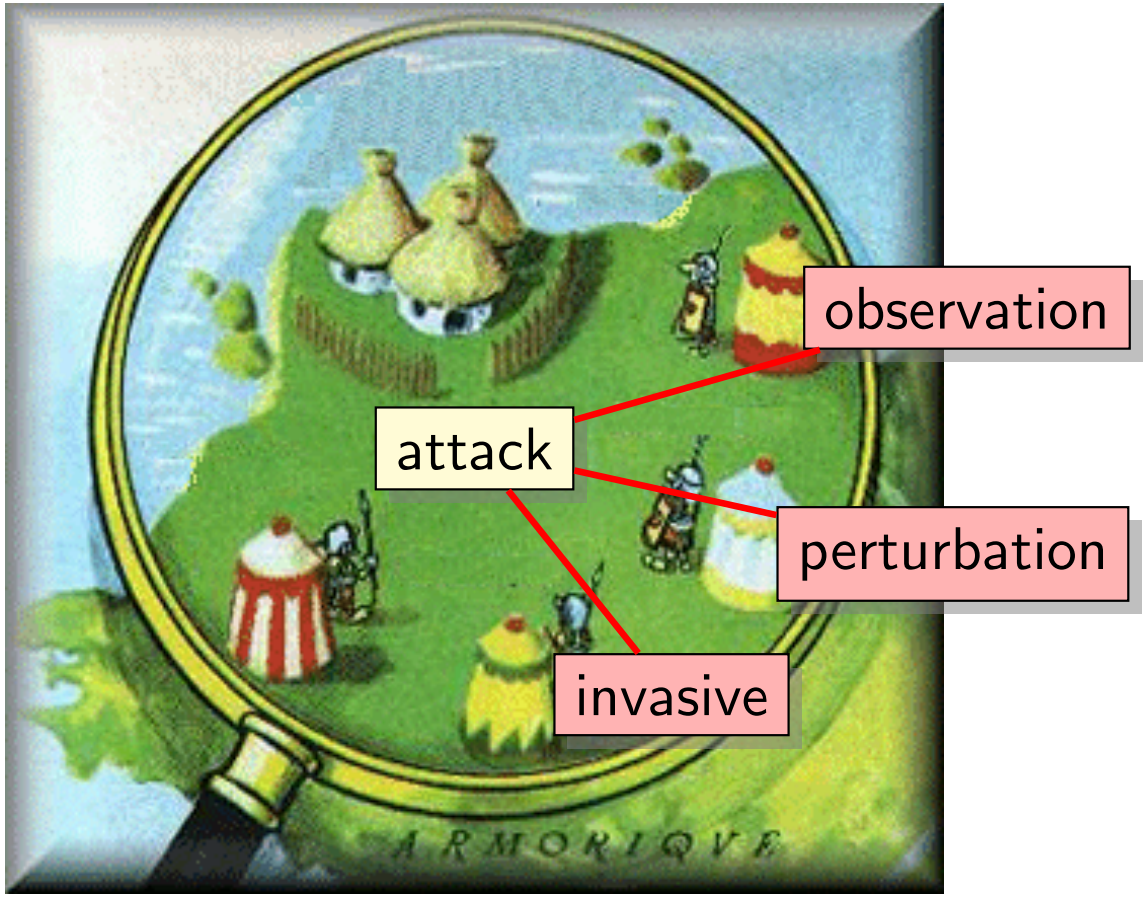

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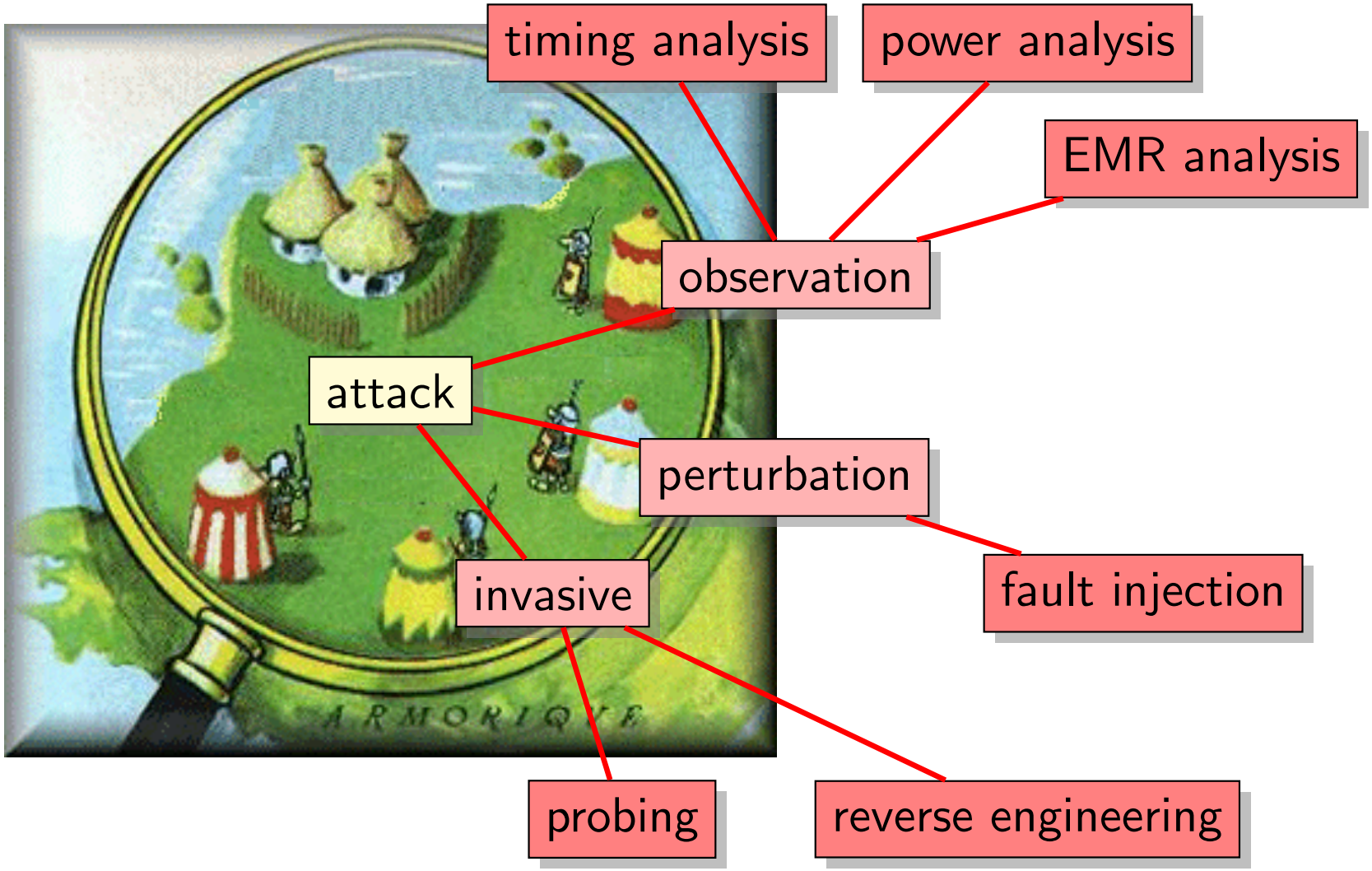

EMR = Electromagnetic radiation

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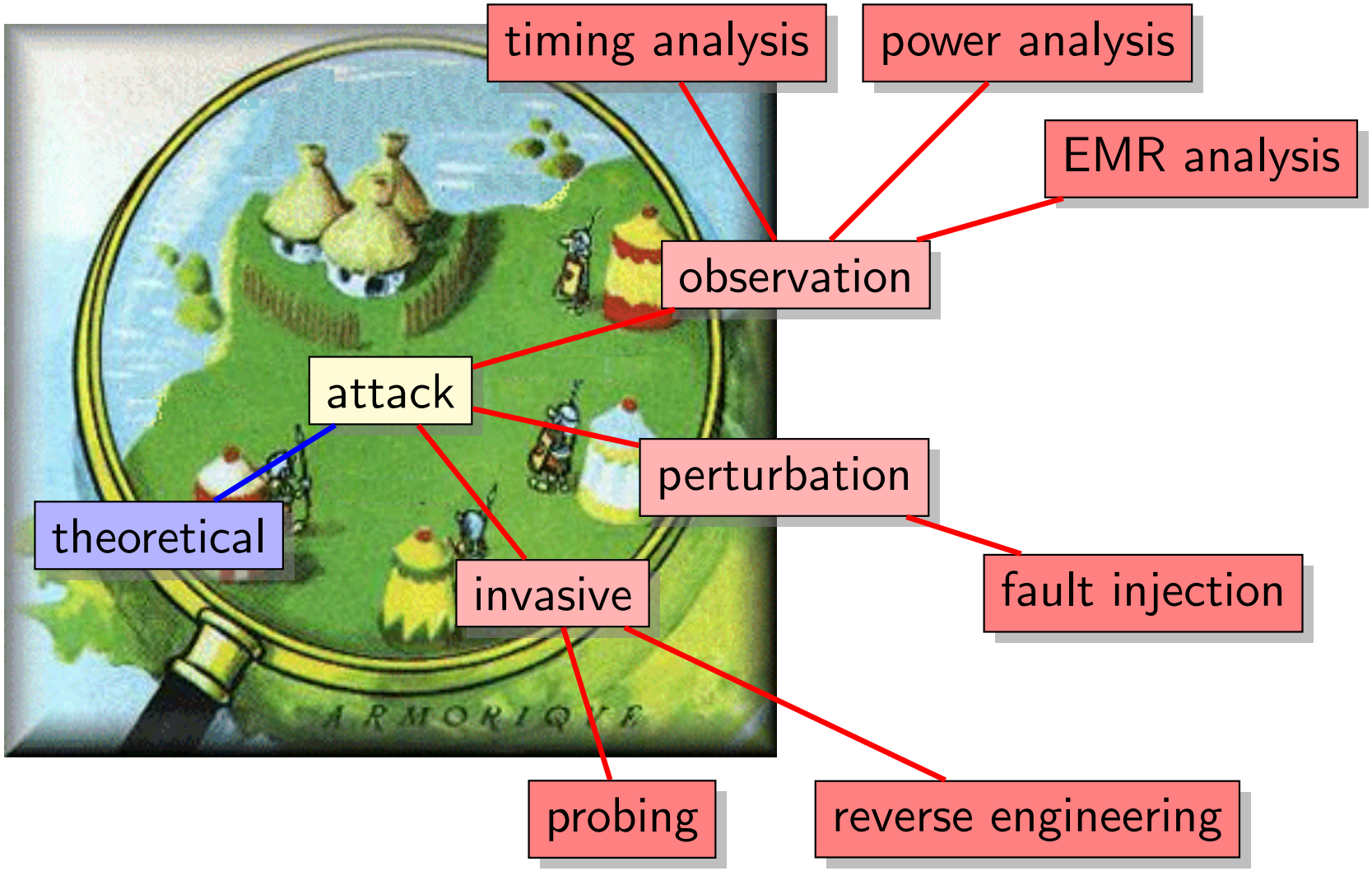

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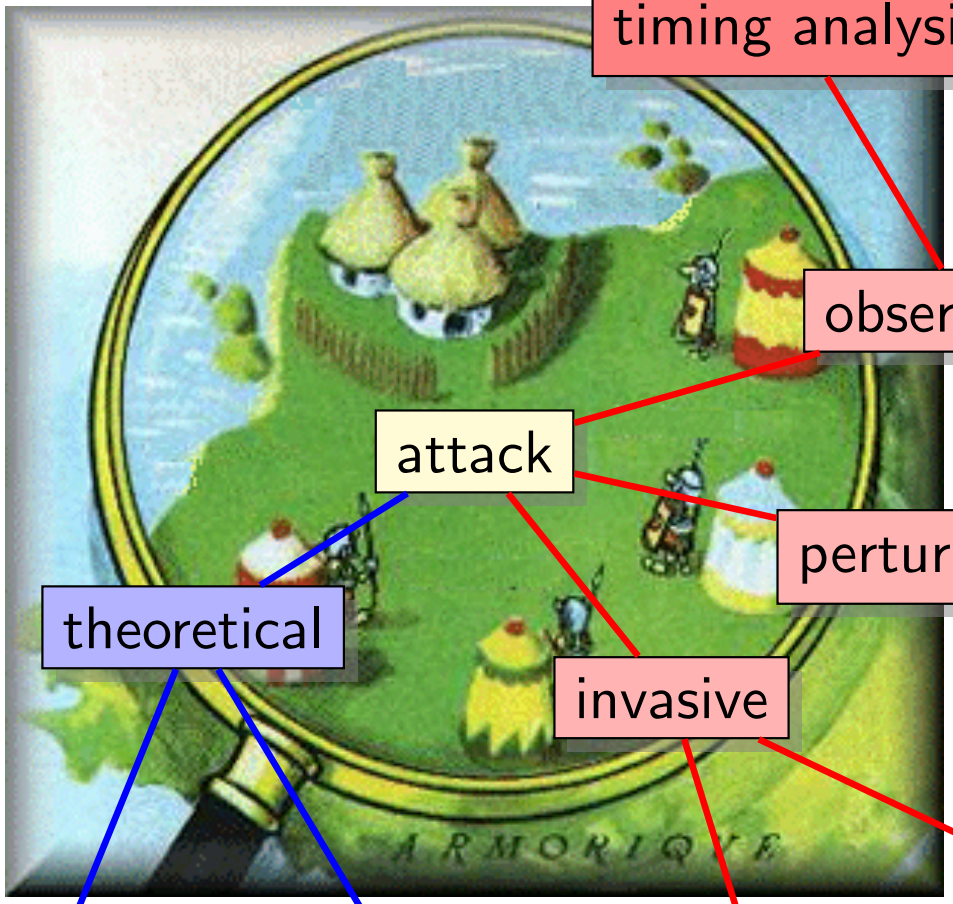

timing analysis

power analysis

EMR analysis

observation

attack

perturbation

theoretical

fault injection

invasive

advanced algorithms

probing

reverse engineering

optimized programming

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Attack: attempt to find, without any knowledge about the secret:

- the message (or parts of the message)
- informations on the message
- the secret (or parts of the secret)

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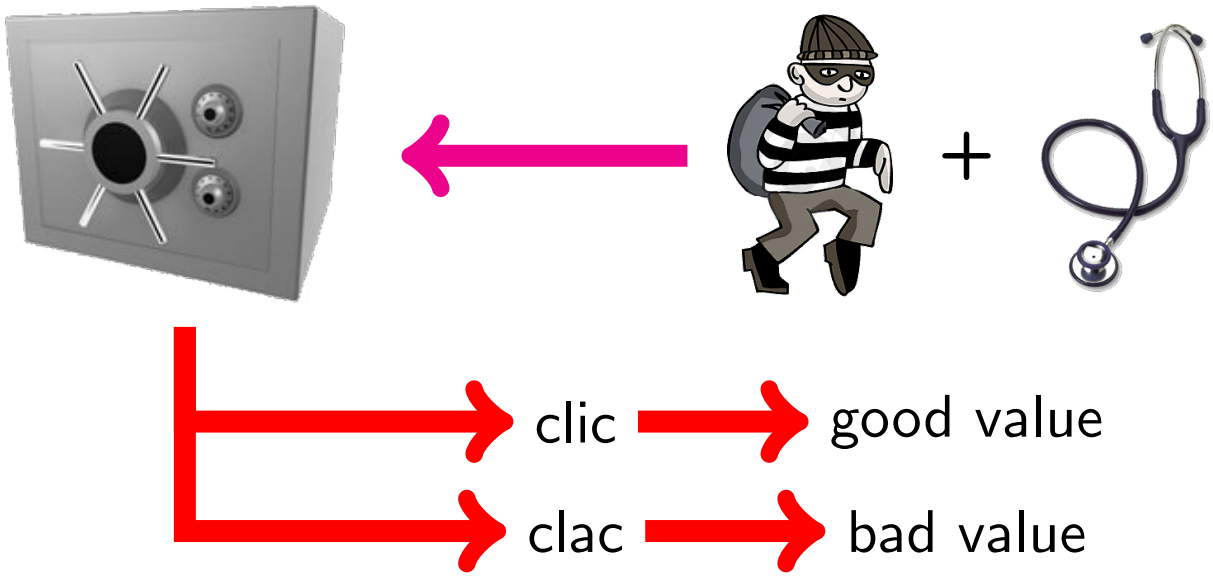
"Old style" side channel attacks:



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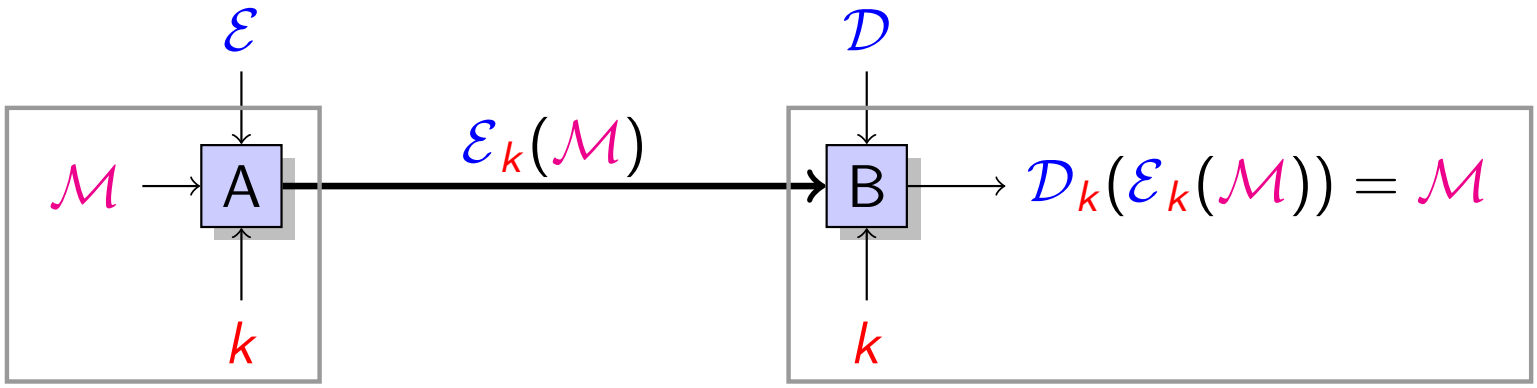
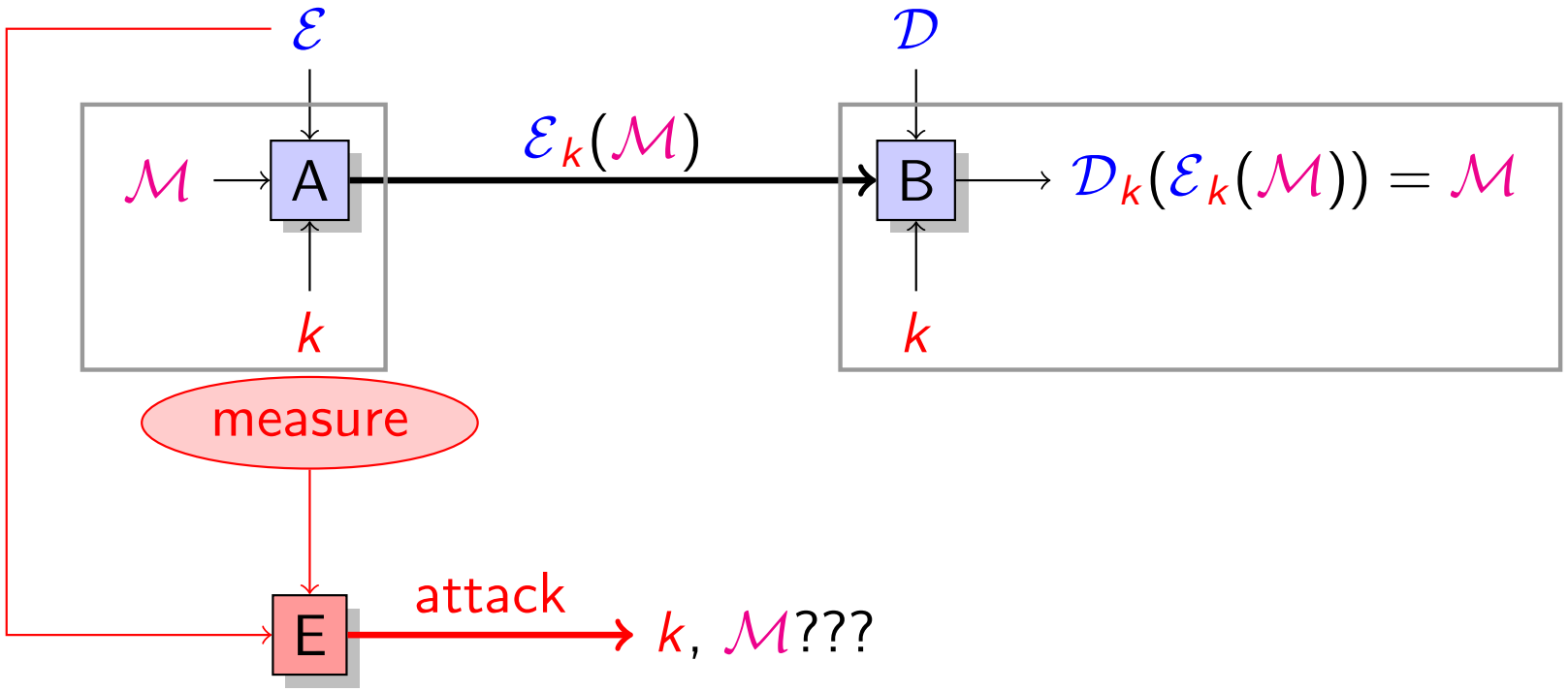


General principle: measure external parameter(s) on running device in order to deduce internal informations

Side Channel Attacks (SCAs) (2/2)



General principle: measure external parameter(s) on running device in order to deduce internal informations

What Should be Measured?

Answer: everything that can "enter" and/or "get out" in/from the device

- power consumption
- electromagnetic radiation
- temperature
- sound
- computation time
- number of cache misses
- number and type of error messages
- ...

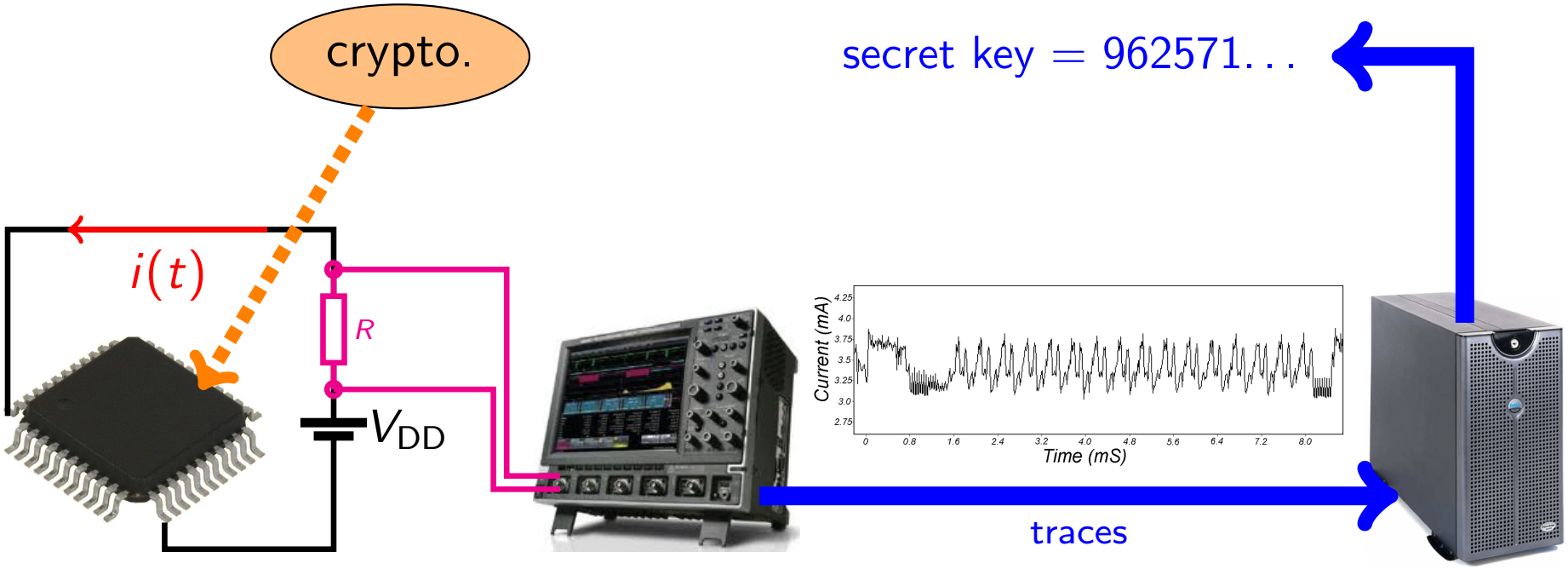
The measured parameters may provide informations on:

- global behavior (temperature, power, sound...)
- local behavior (EMR, # cache misses...)

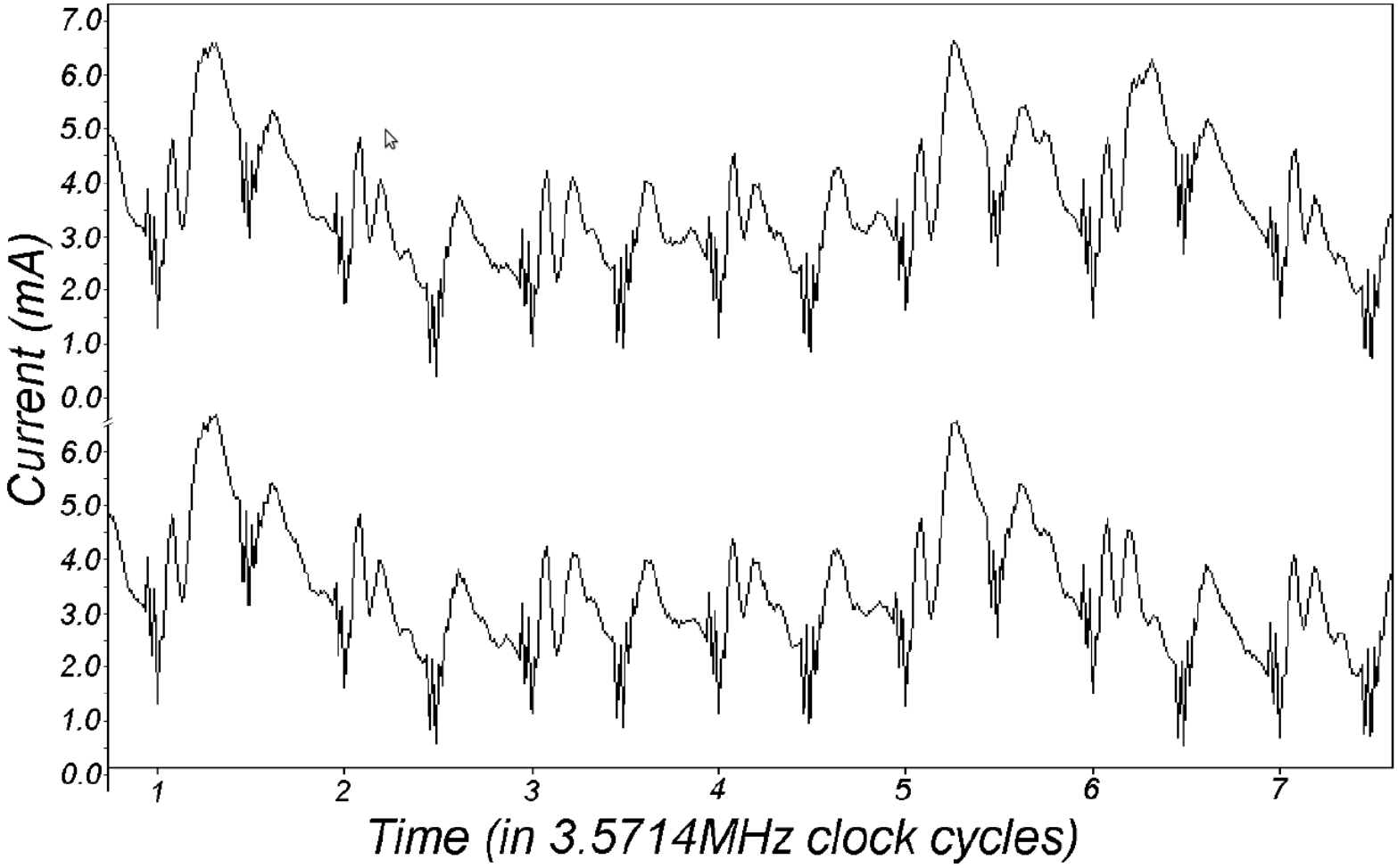
Power Consumption Analysis

General principle:

1. measure the current $i(t)$ in the cryptosystem
2. use those measurements to "deduce" secret informations

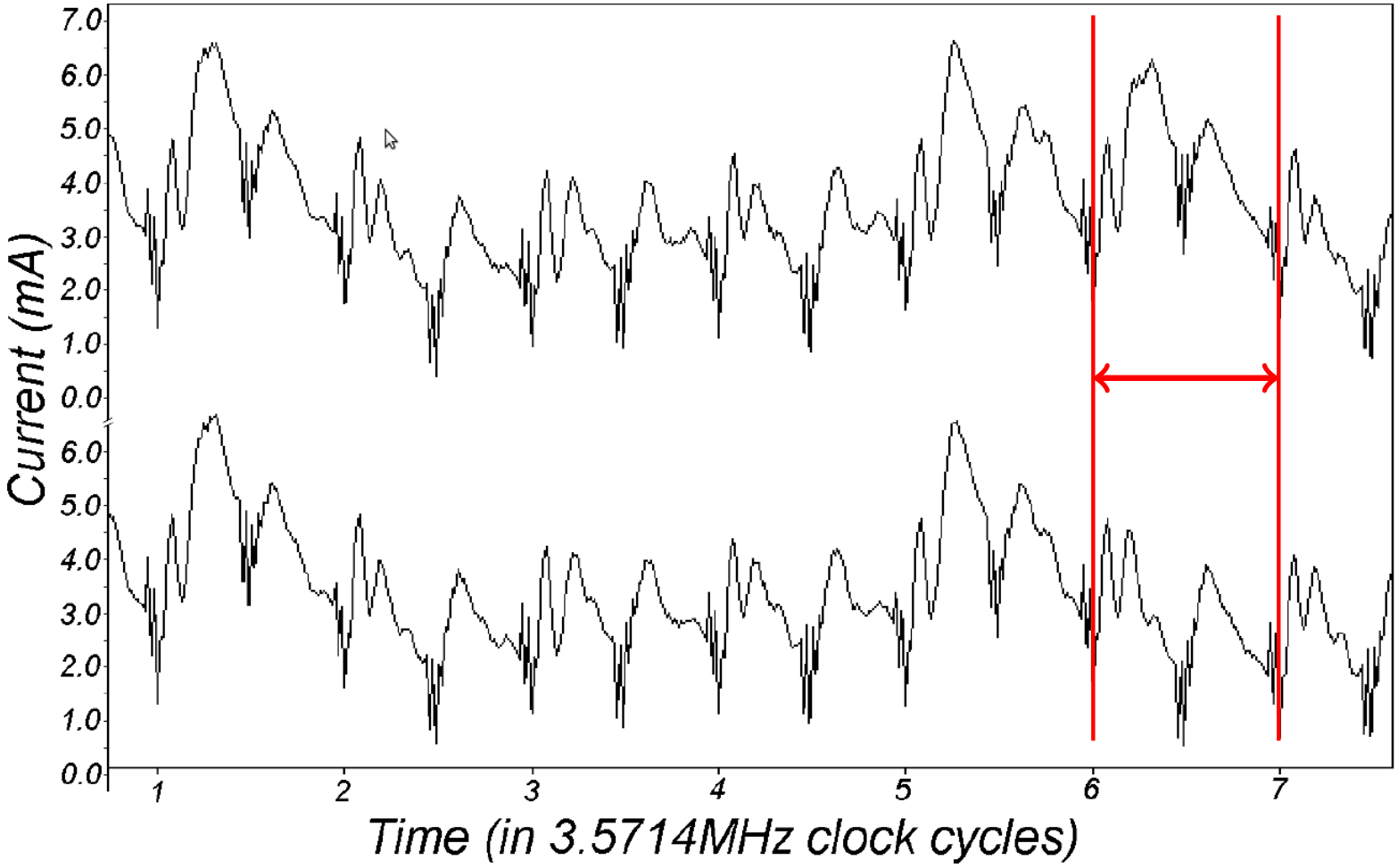


Simple Power Analysis (SPA)



Source: [11]

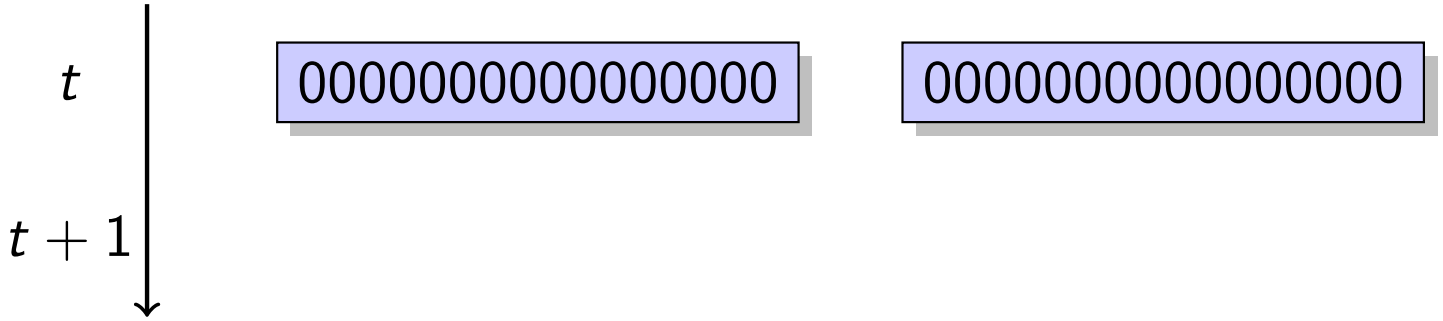
Simple Power Analysis (SPA)



Source: [11]

Limits of the SPA

Example of behavior difference: (activity into a register)



Limits of the SPA

Example of behavior difference: (activity into a register)

t	0000000000000000	0000000000000000
$t+1$	1111111111111111	0000000000000001

Limits of the SPA

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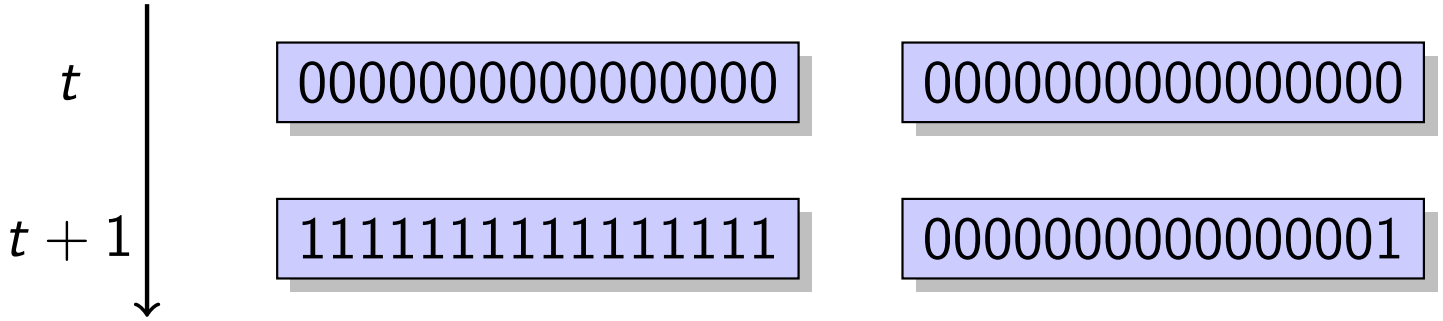


Important: a small difference may be evaluated has a noise during the measurement → traces cannot be distinguished

Question: what can be done when differences are too small?

Limits of the SPA

Example of behavior difference: (activity into a register)

t	0000000000000000	0000000000000000
$t+1$	1111111111111111	0000000000000001

Important: a small difference may be evaluated has a noise during the measurement → traces cannot be distinguished

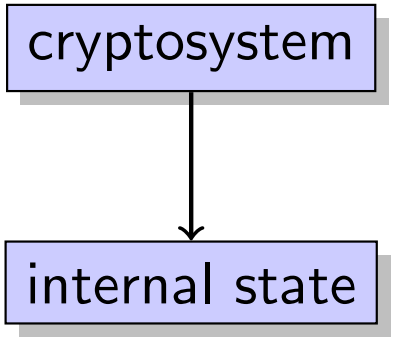
Question: what can be done when differences are too small?

Answer: use statistics over several traces

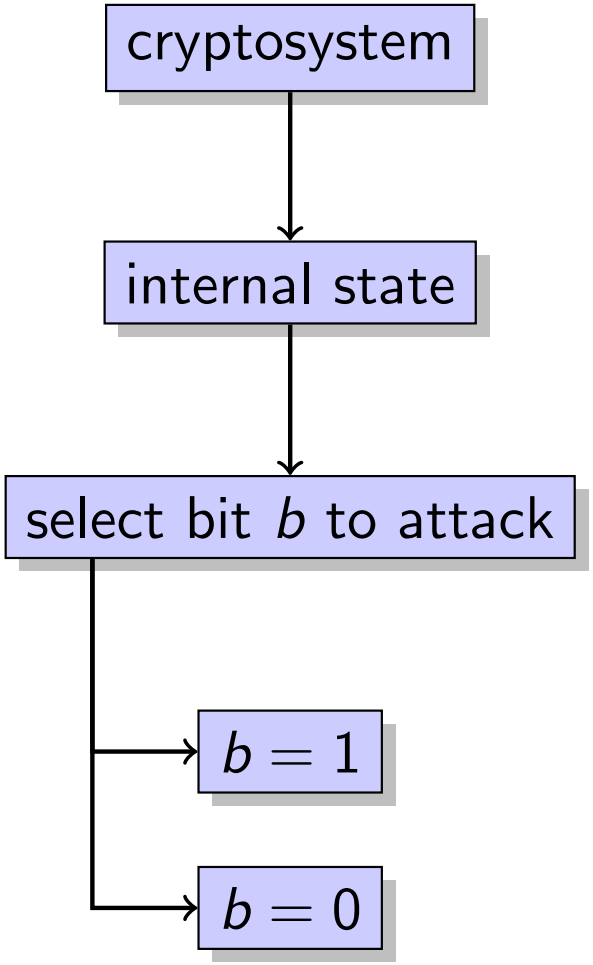
Differential Power Analysis (DPA)

cryptosystem

Differential Power Analysis (DPA)



Differential Power Analysis (DPA)



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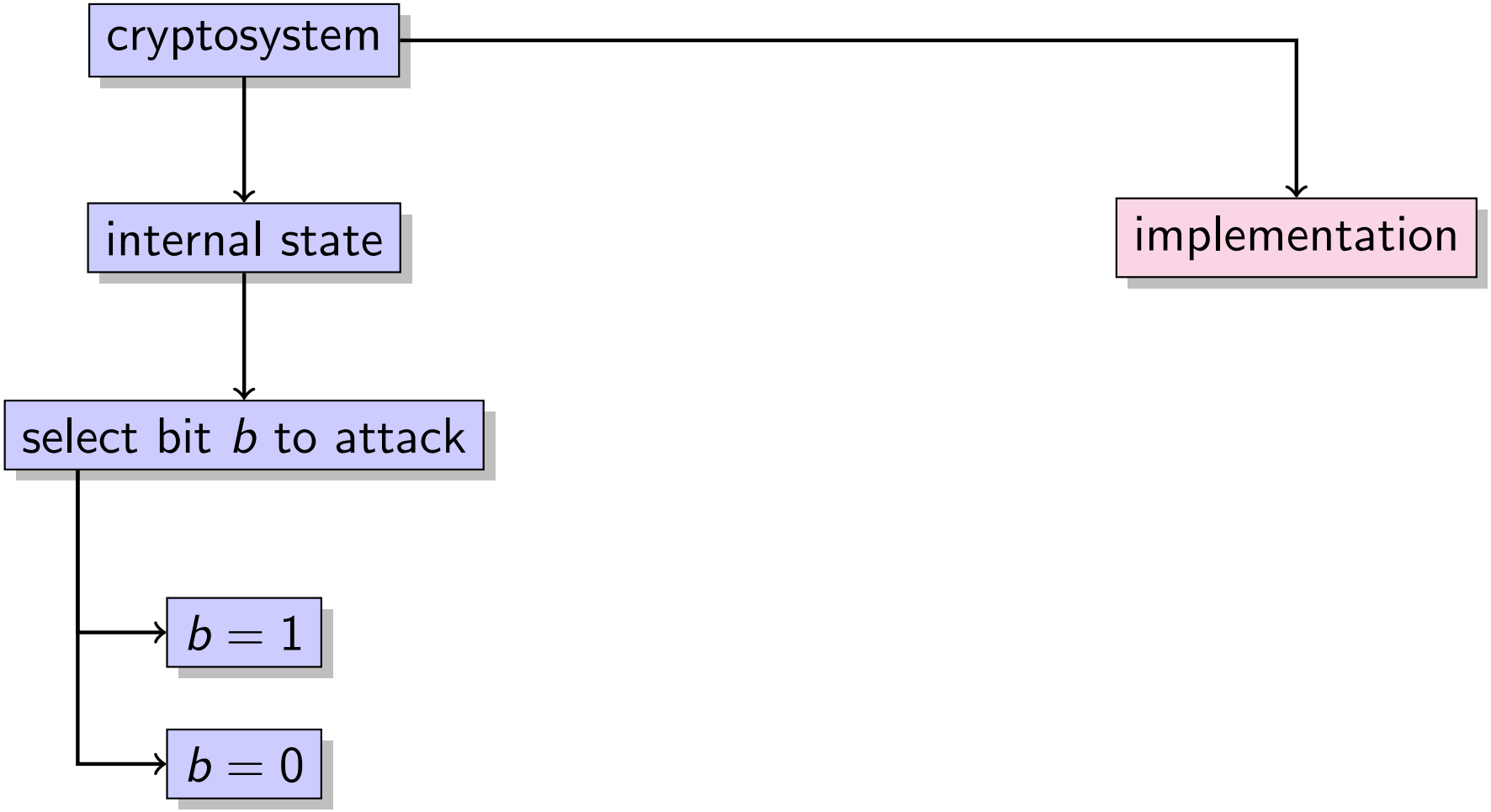
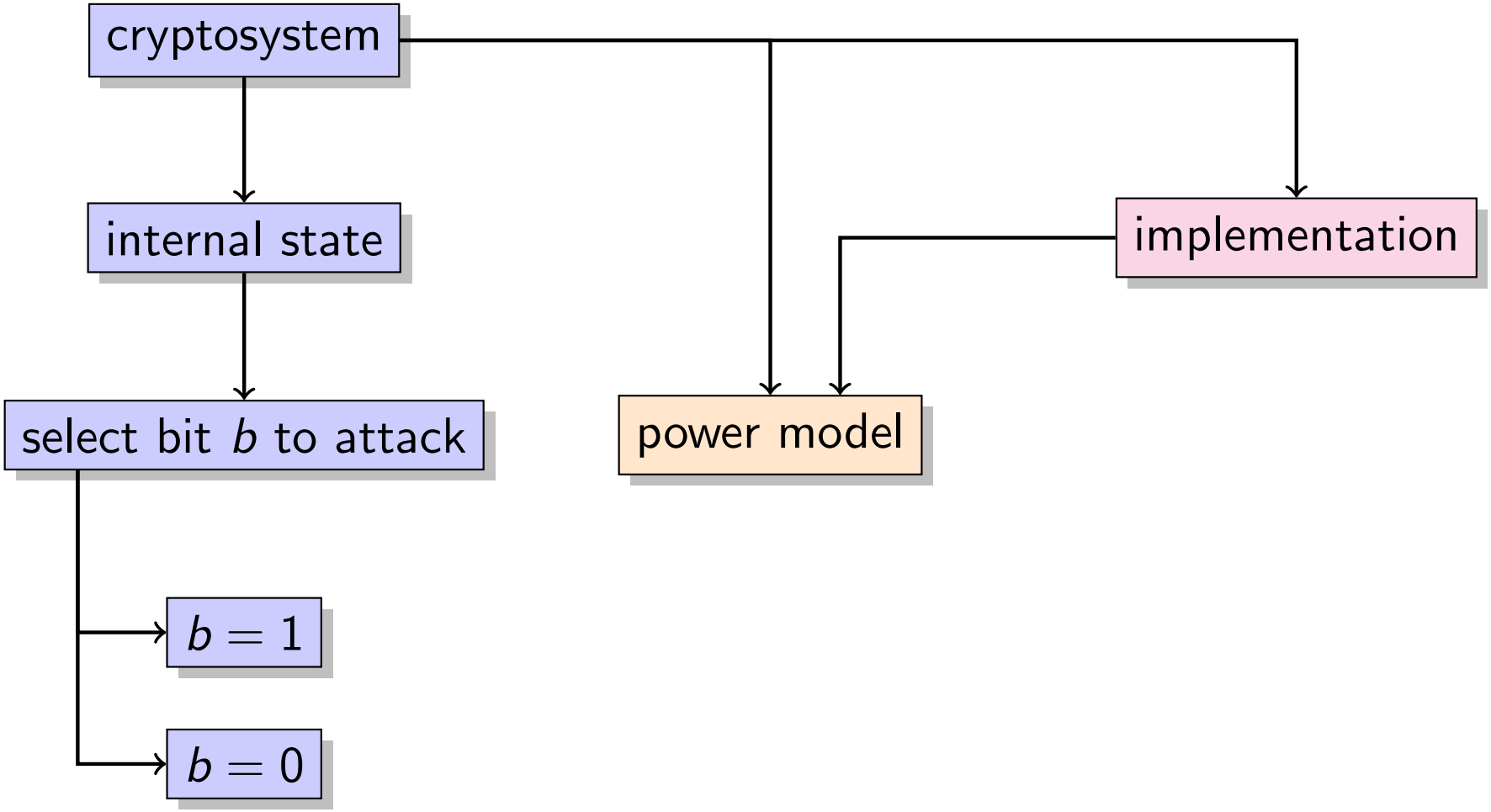


Differential Power Analysis (DPA)



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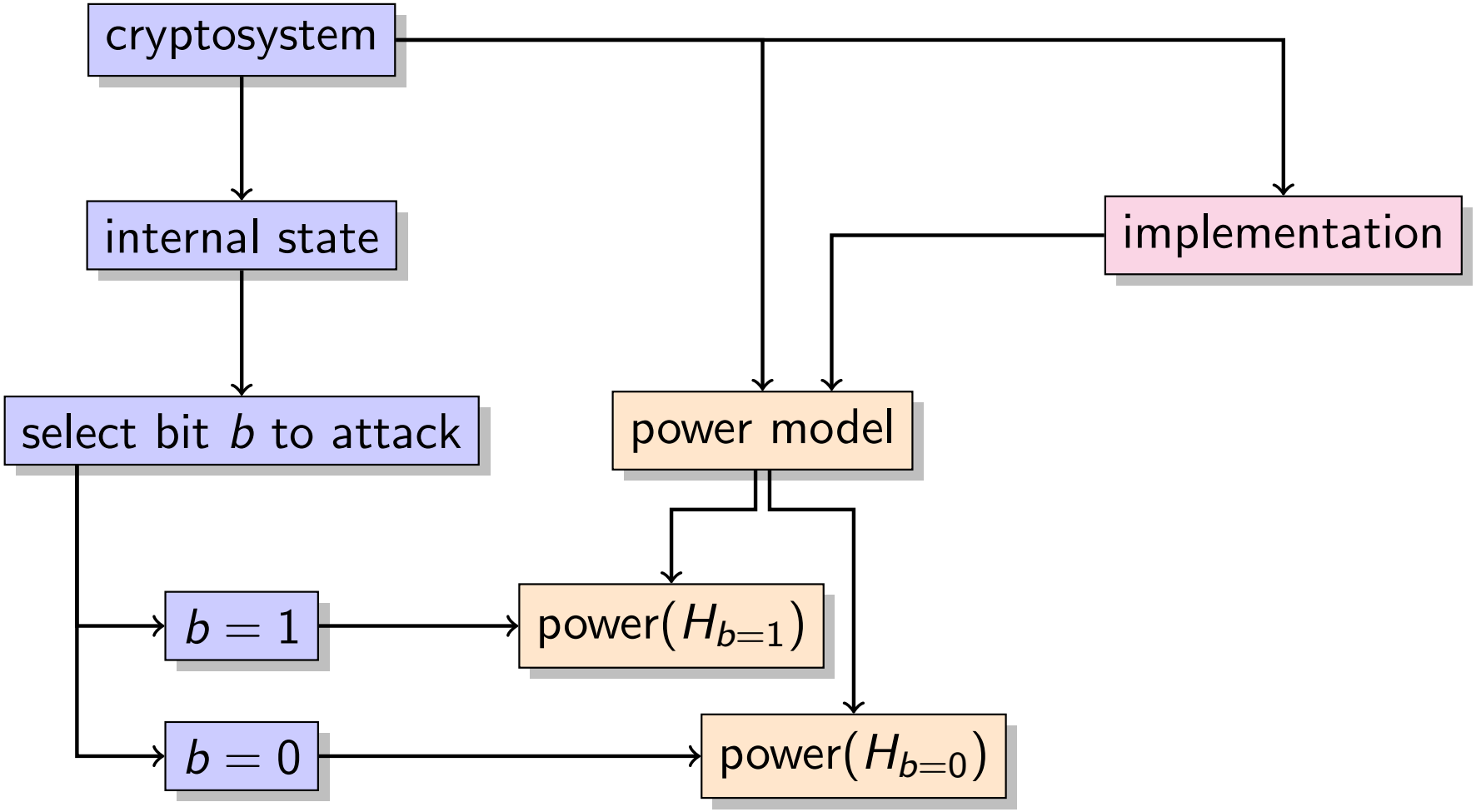
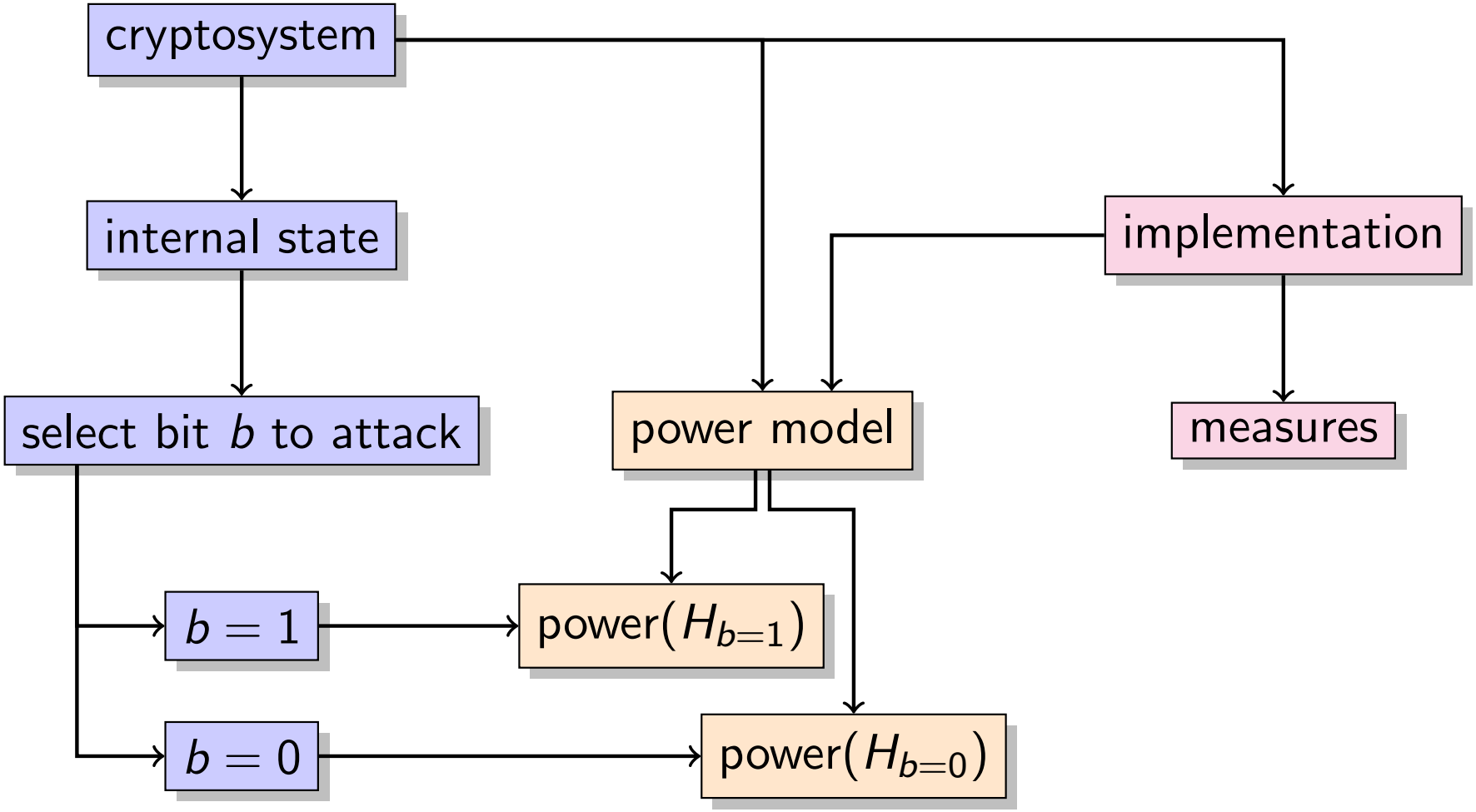


Differential Power Analysis (DPA)



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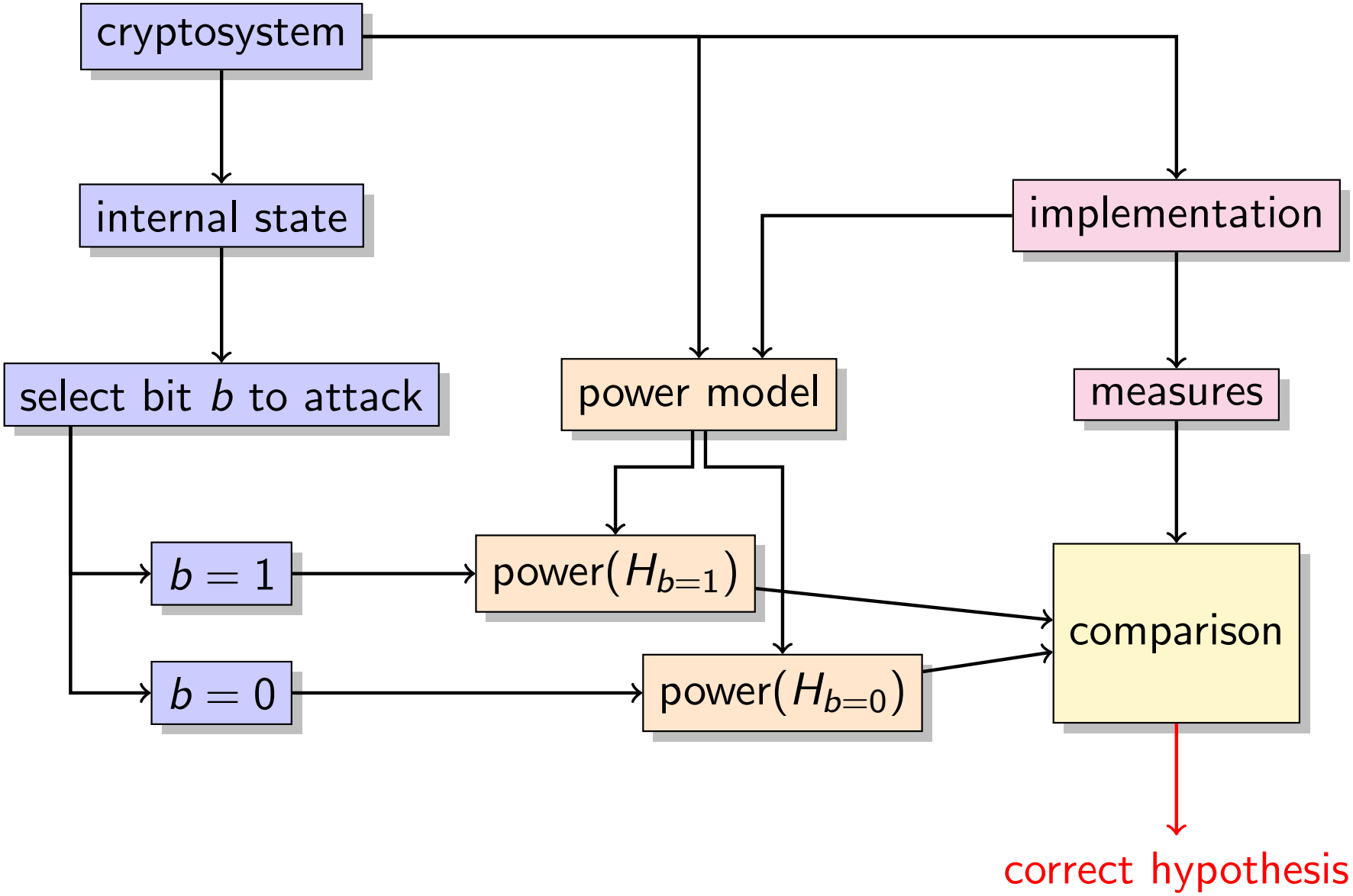
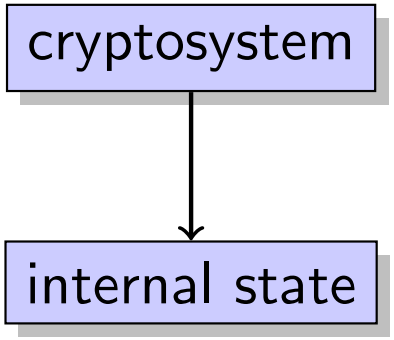


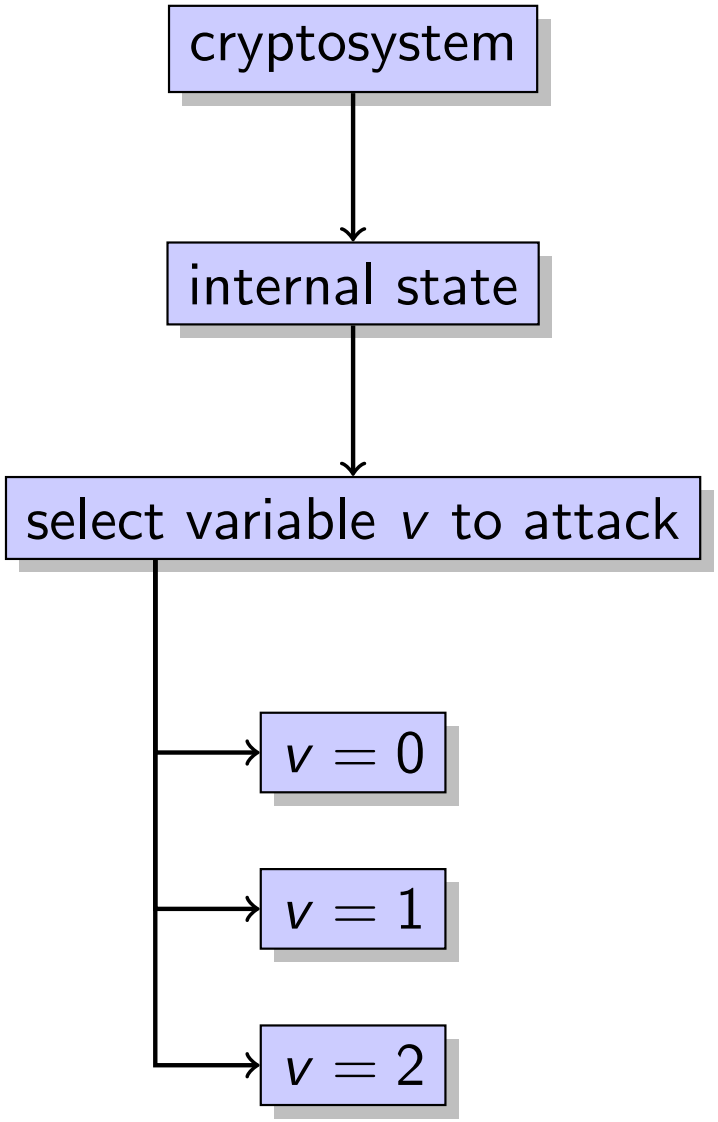
Template Attack

cryptosystem

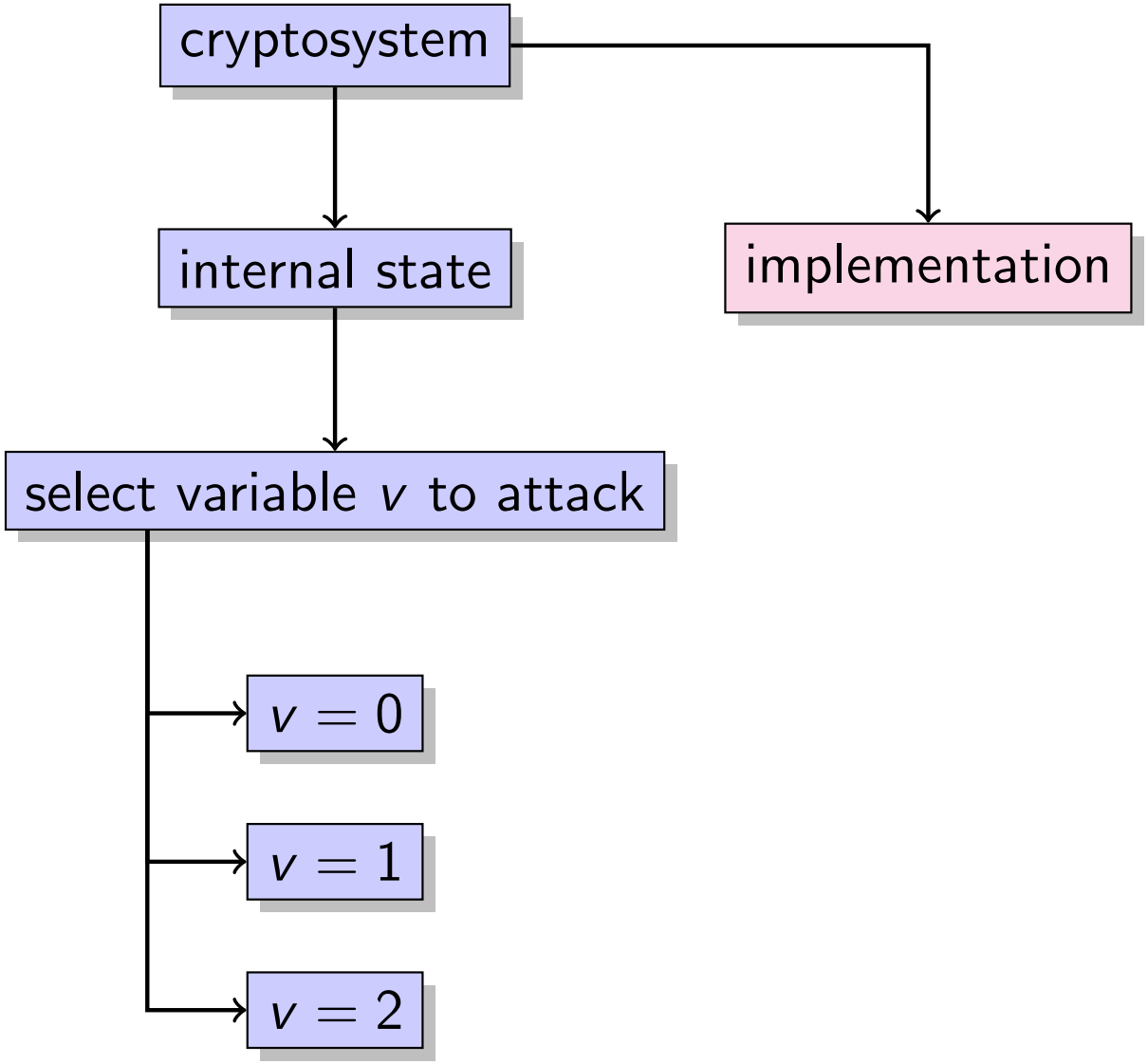
Template Attack



Template Attack



Template Attack



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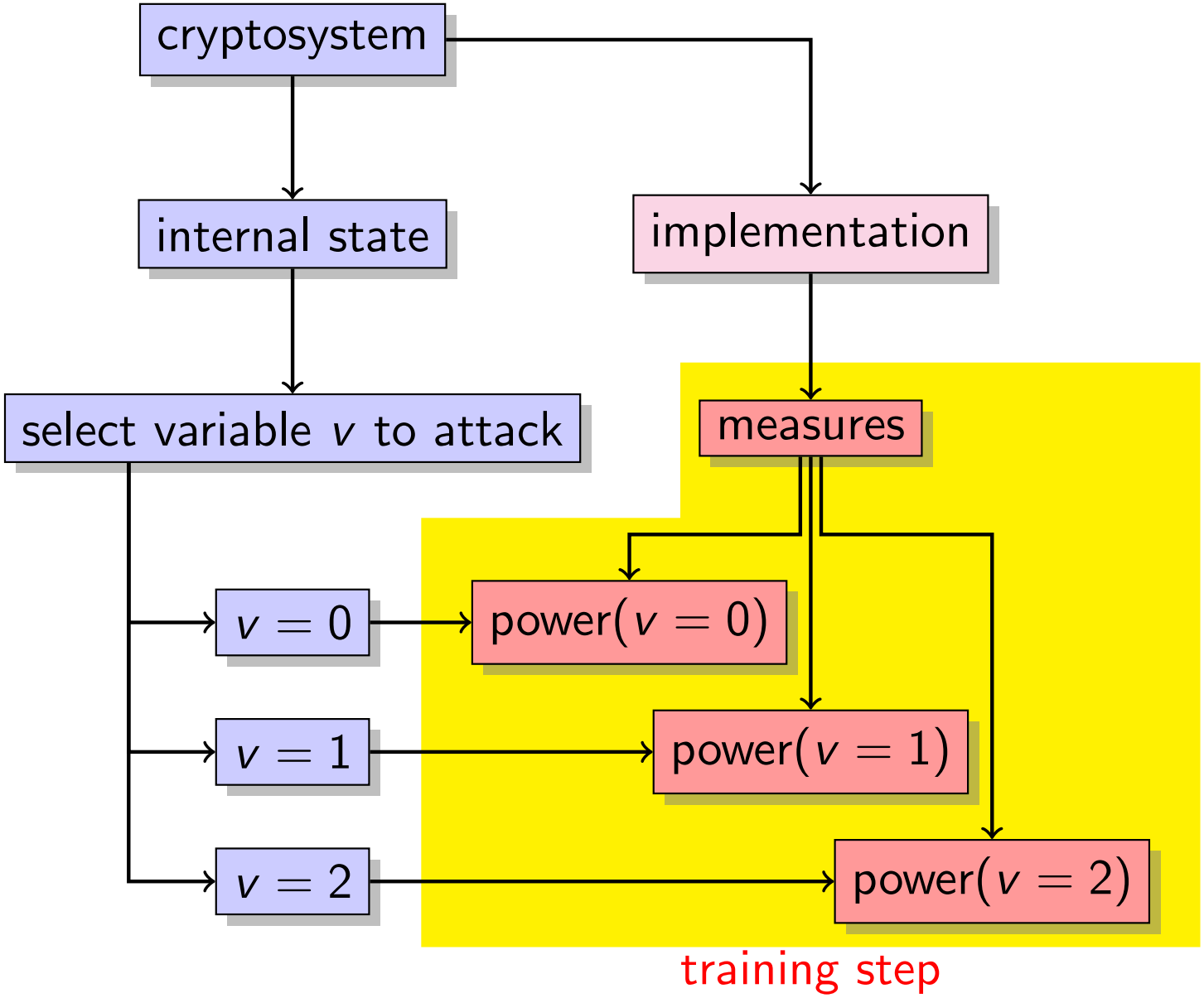
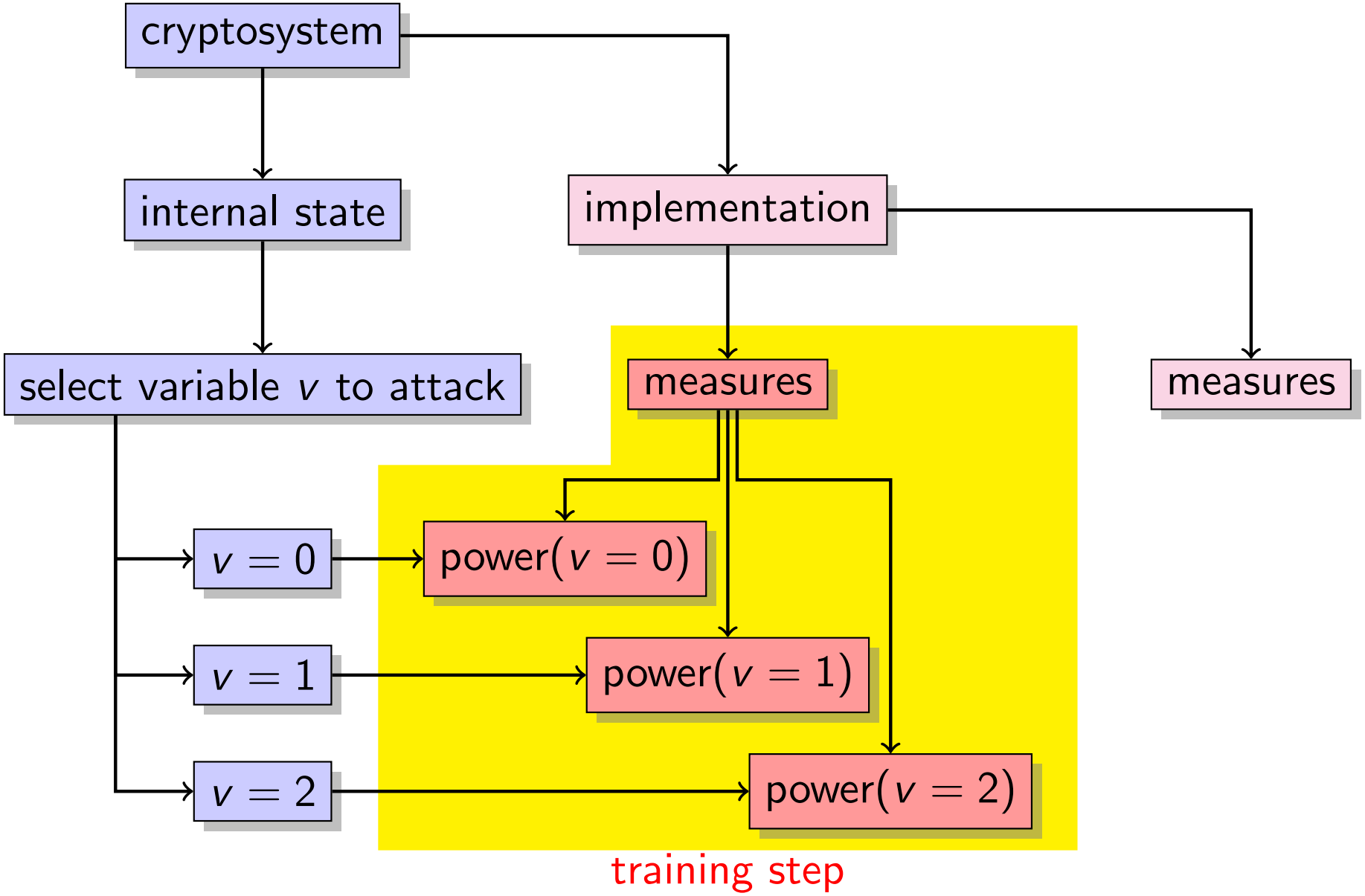


Template Attack



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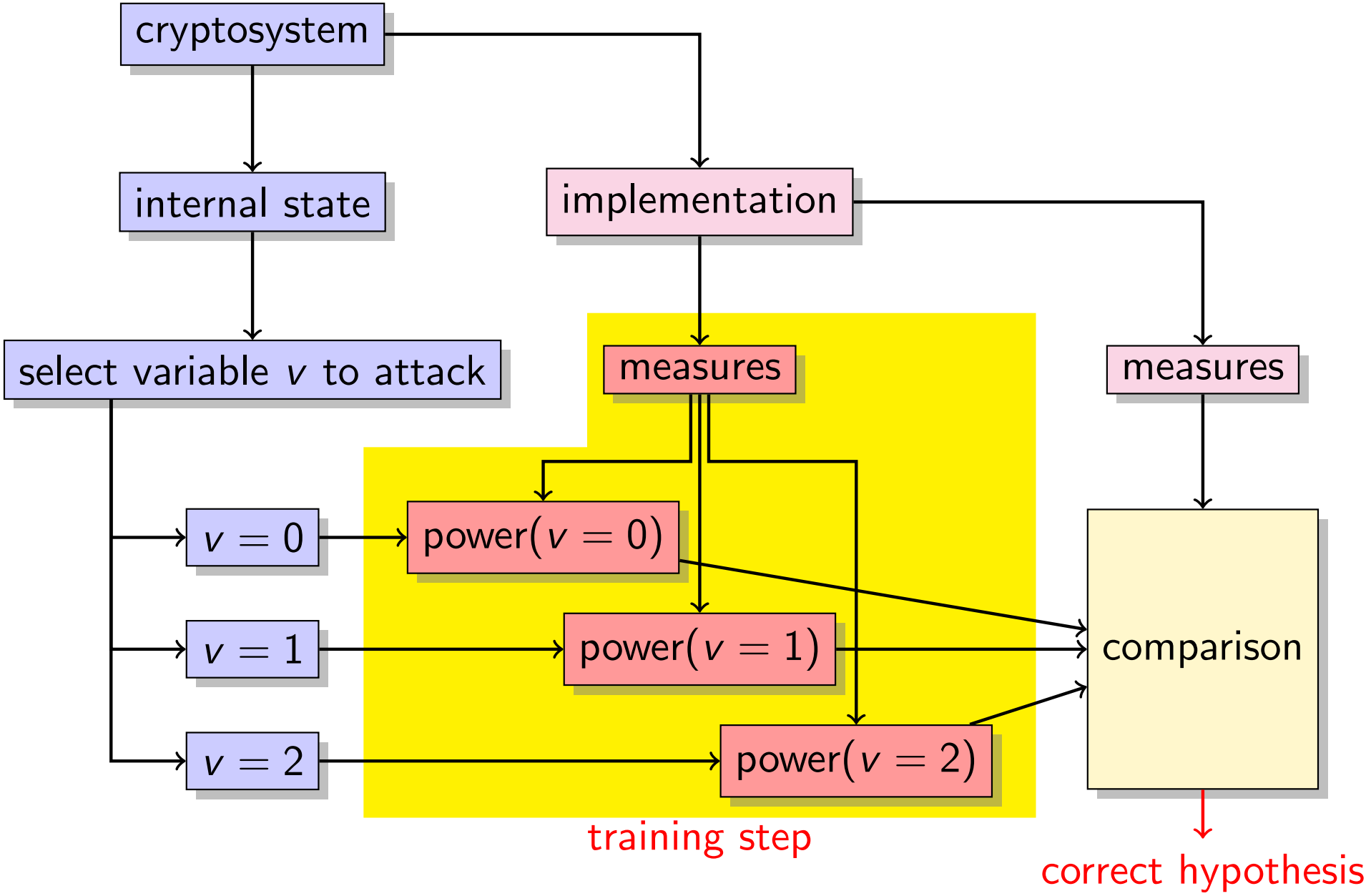
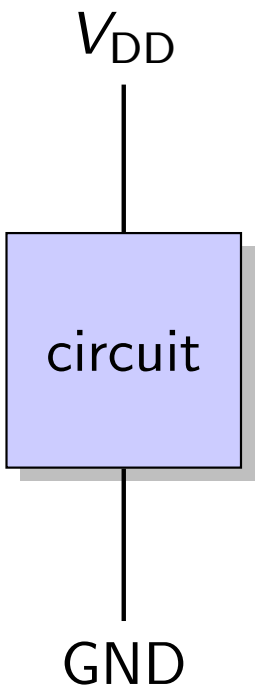


Electromagnetic Radiation Analysis

General principle: use a probe to measure the EMR



EMR measurement:

Electromagnetic Radiation Analysis

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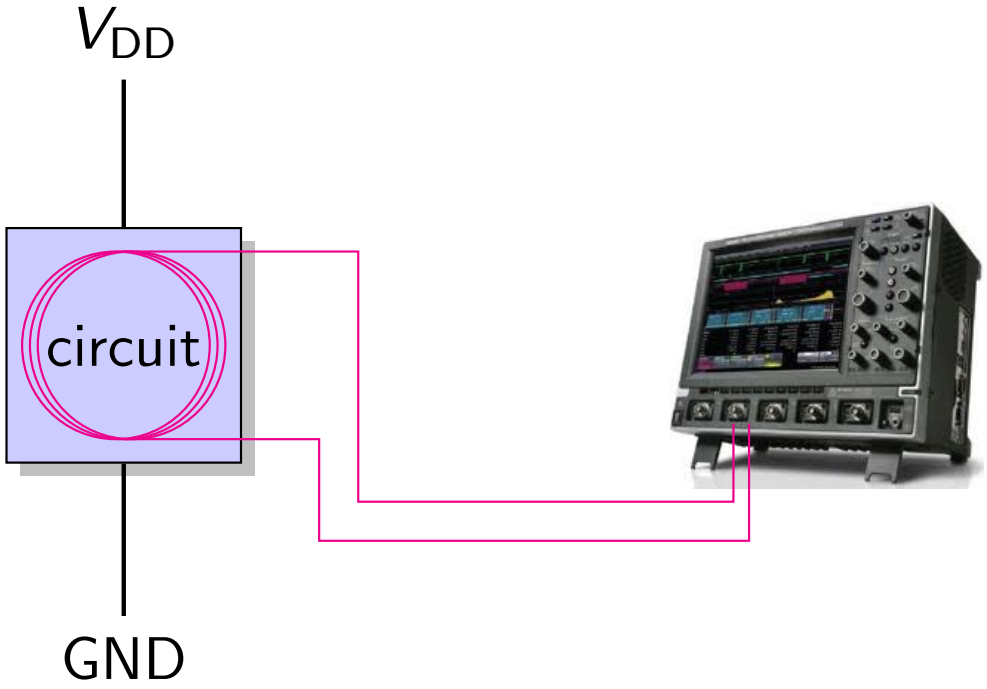

EMR measurement:

- global EMR with a large probe

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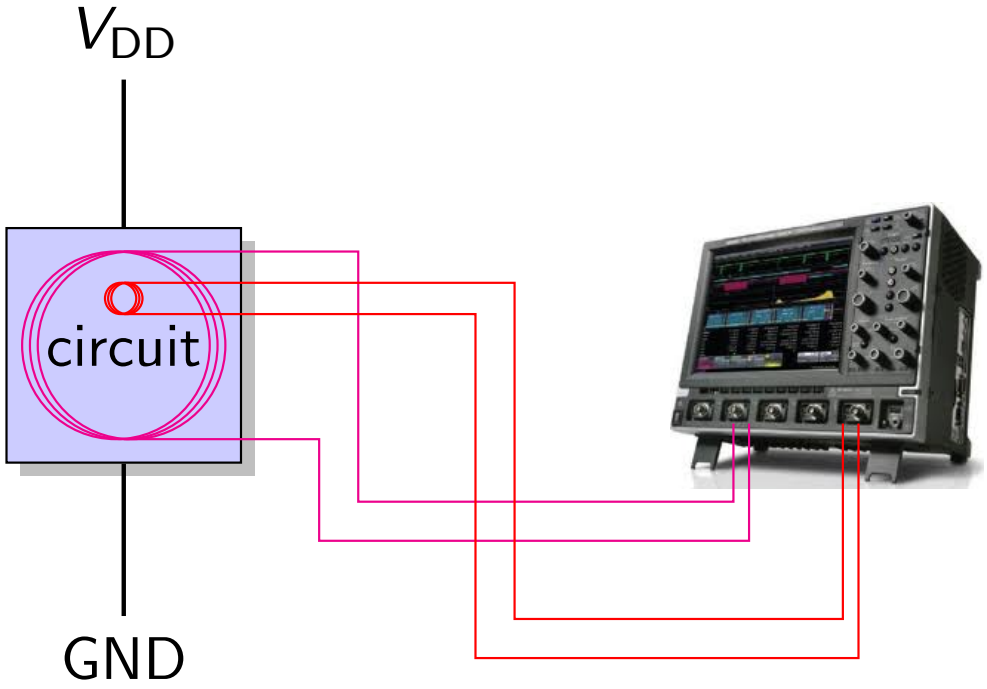
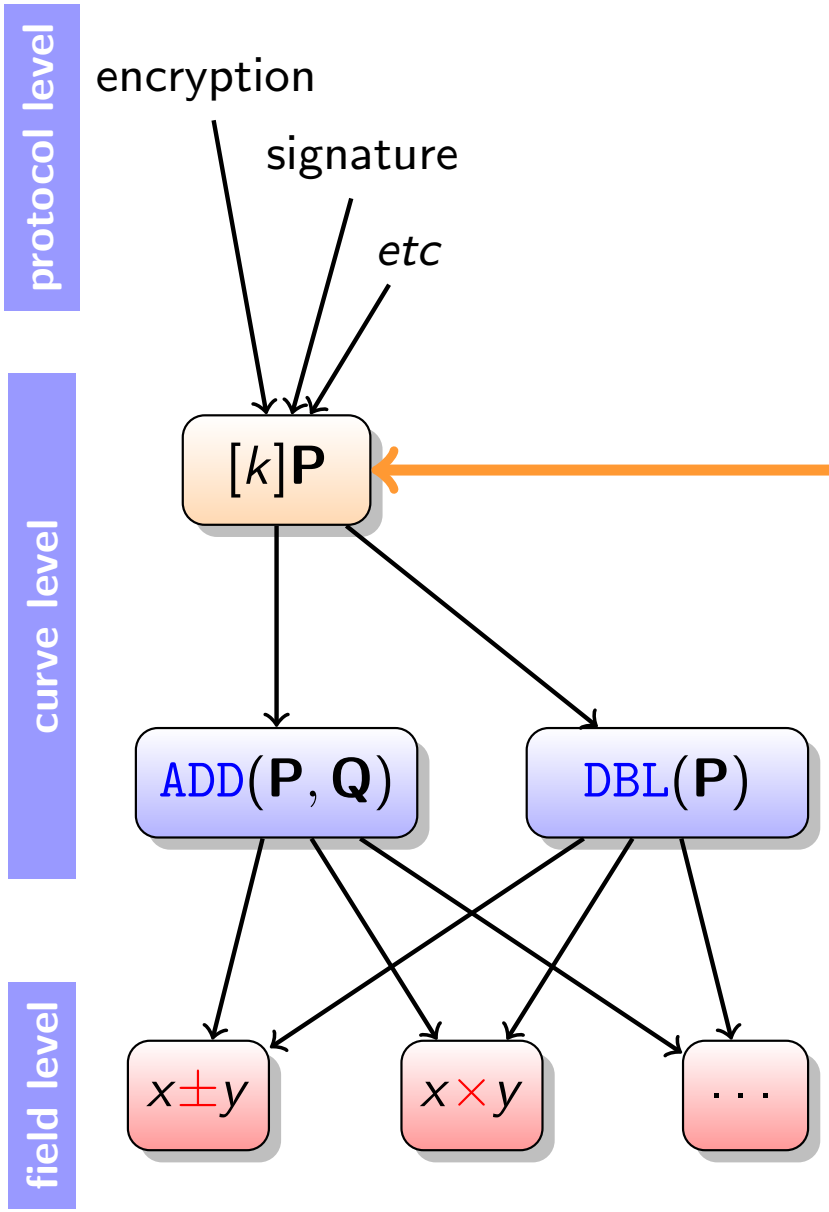


EMR measurement:

- global EMR with a large probe
- local EMR with a micro-probe

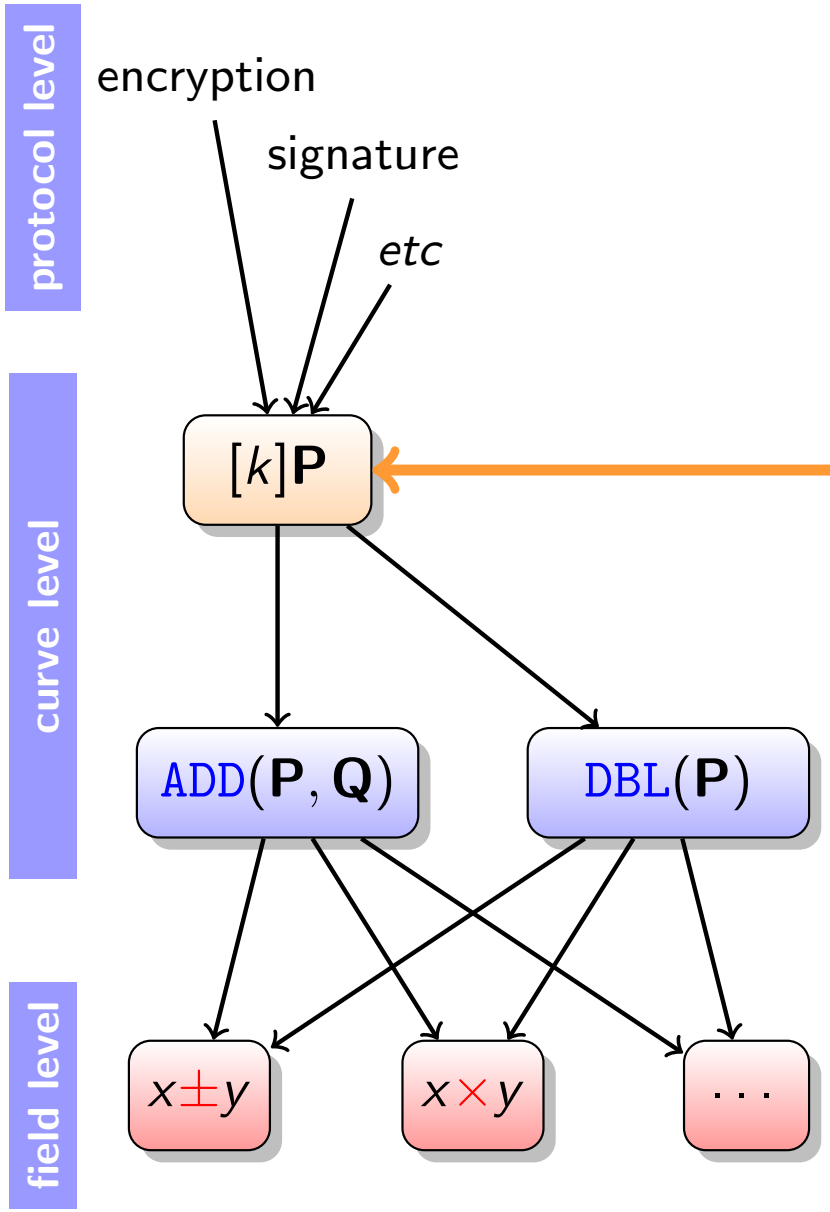
Side Channel Attack on ECC

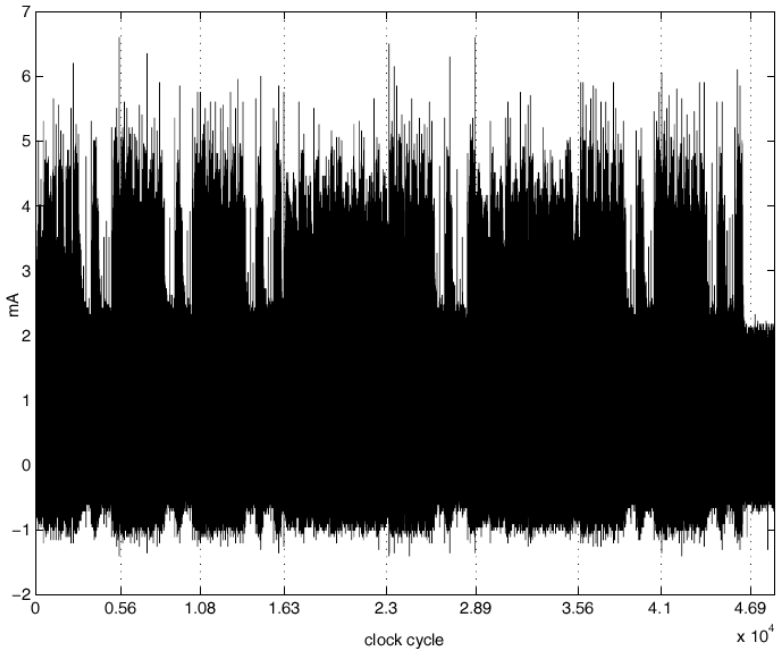


Scalar multiplication operation

```
for i from 0 to t − 1 do
    if k_i = 1 then Q = ADD(P, Q)
    P = DBL(P)
```

Side Channel Attack on ECC





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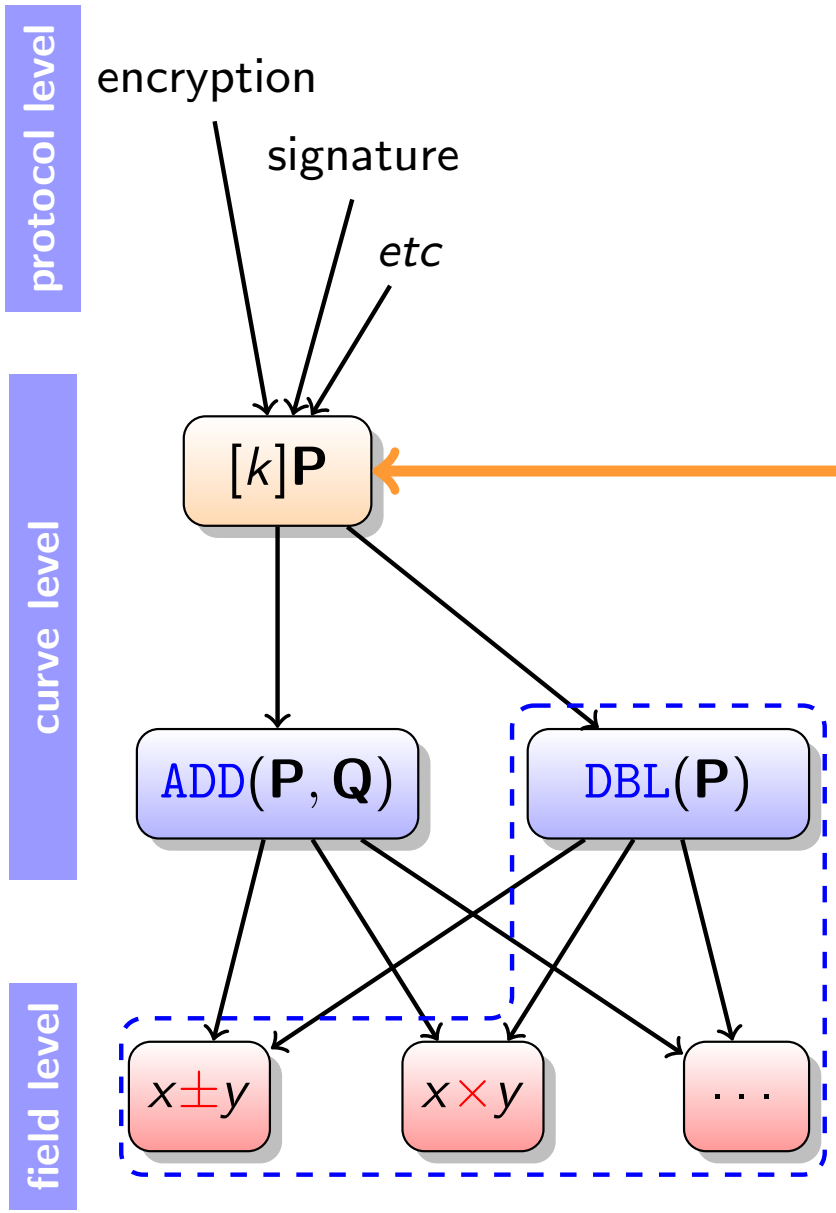

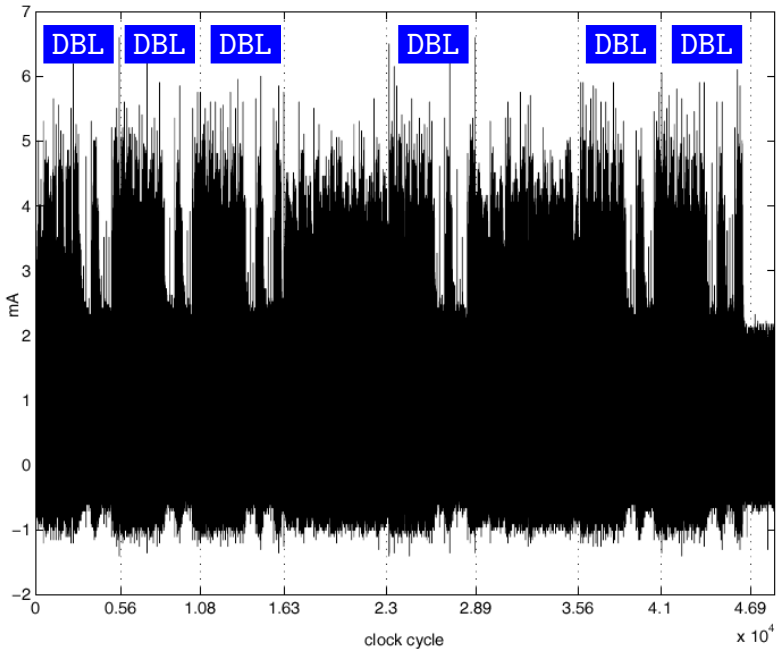

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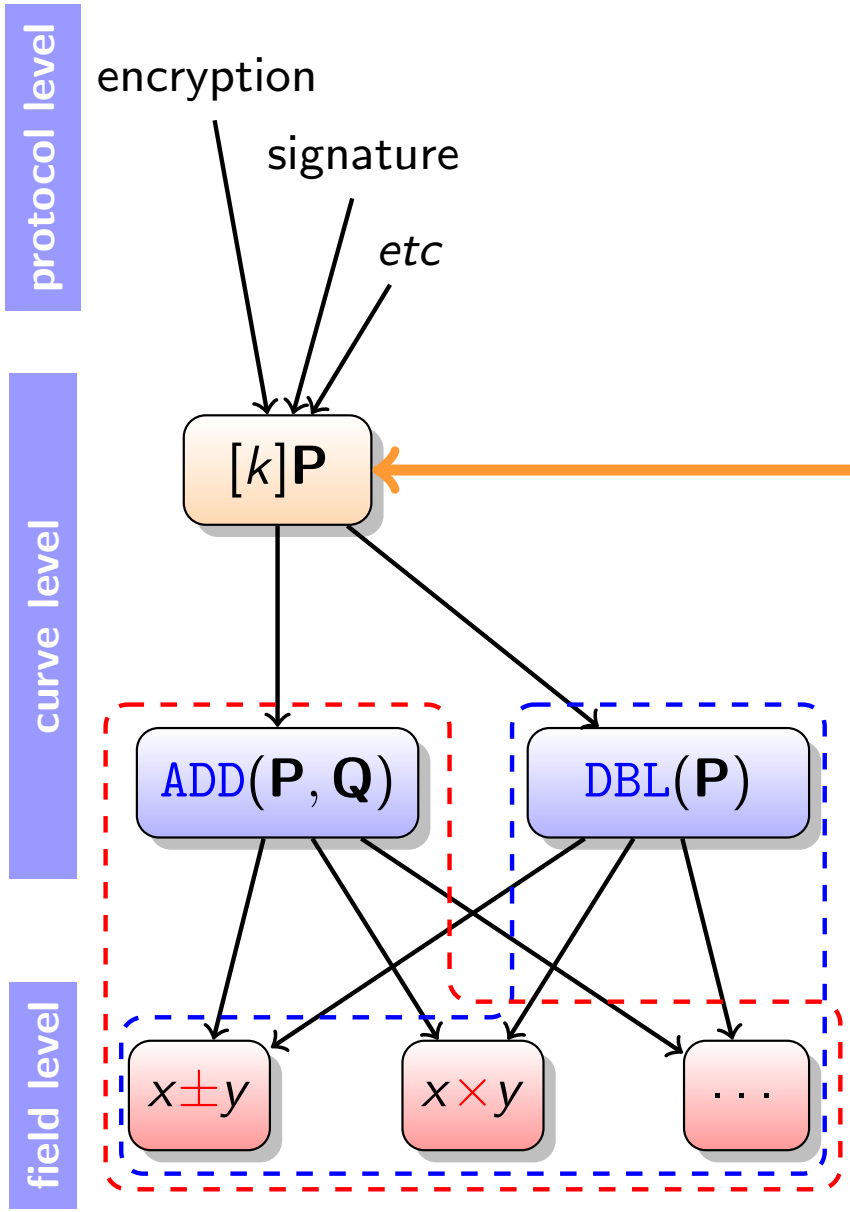

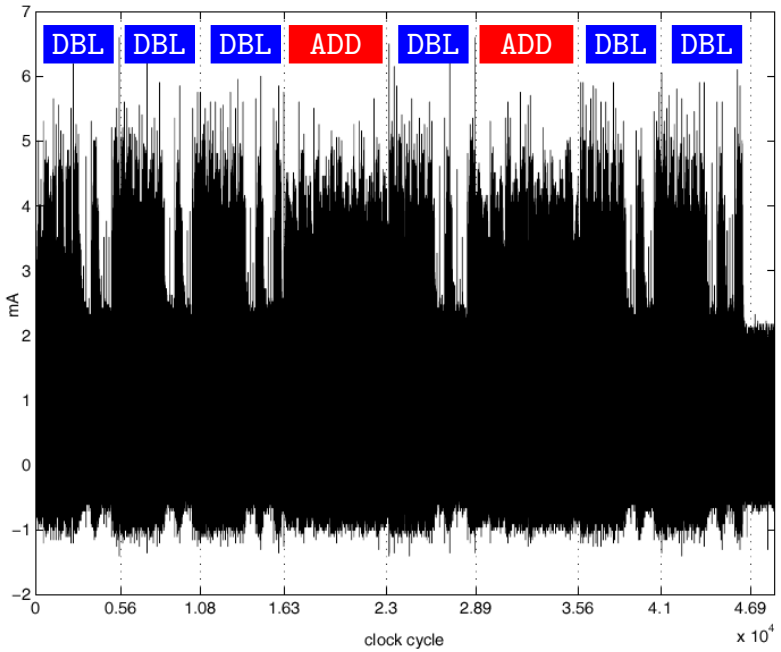

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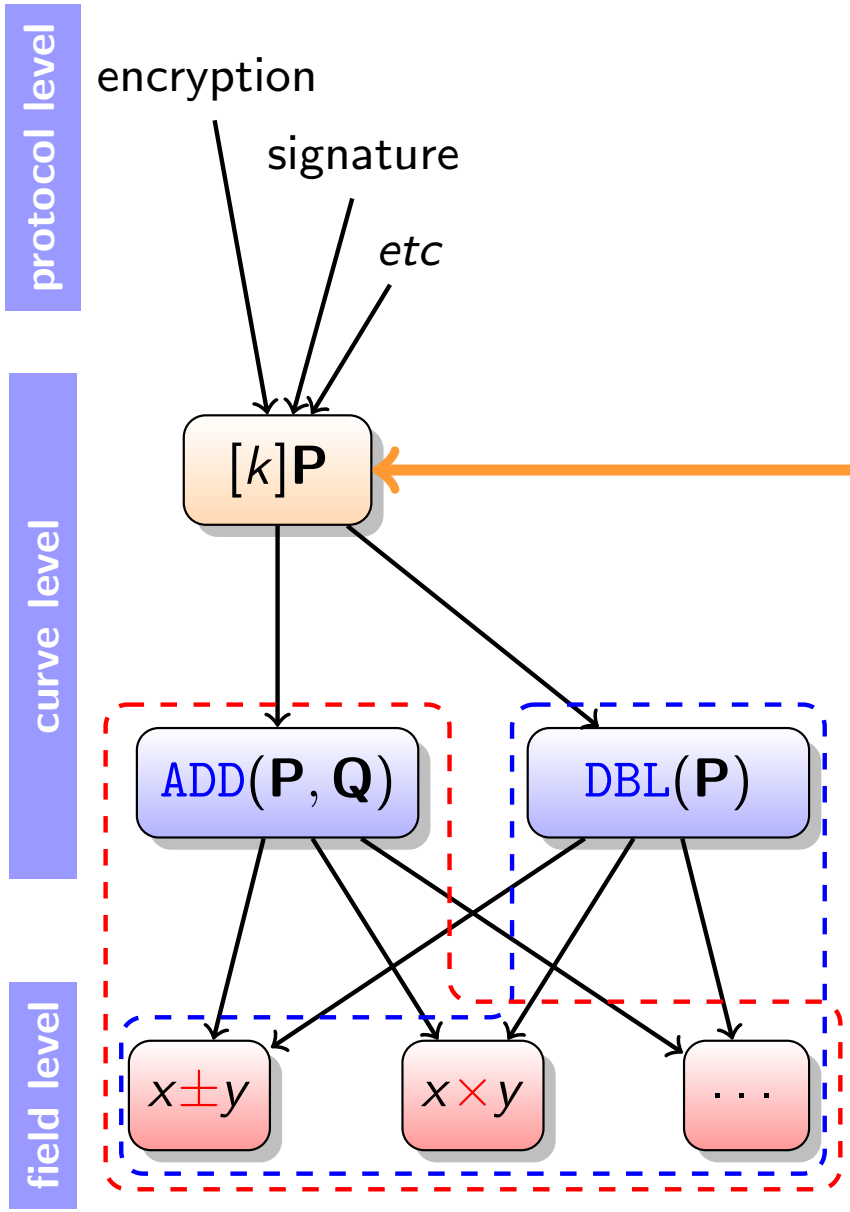

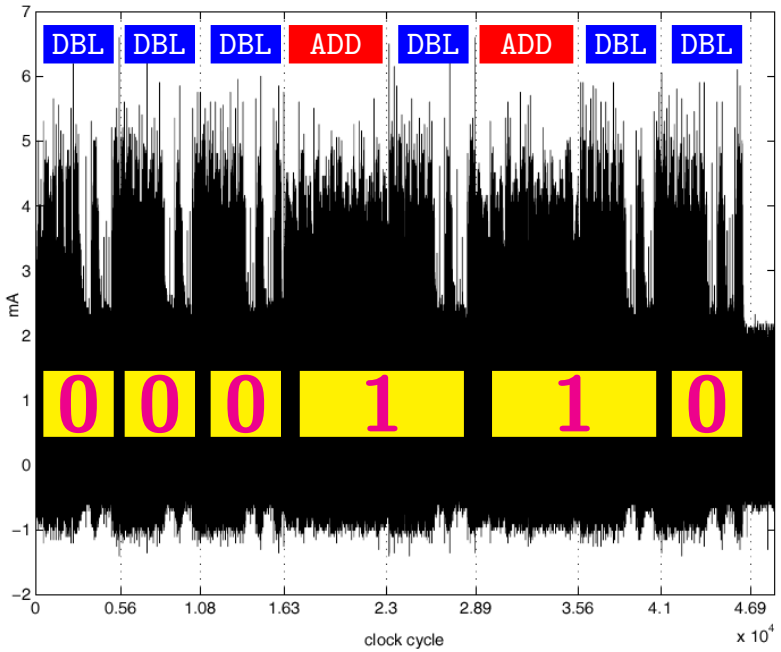

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- simple power analysis (& variants)

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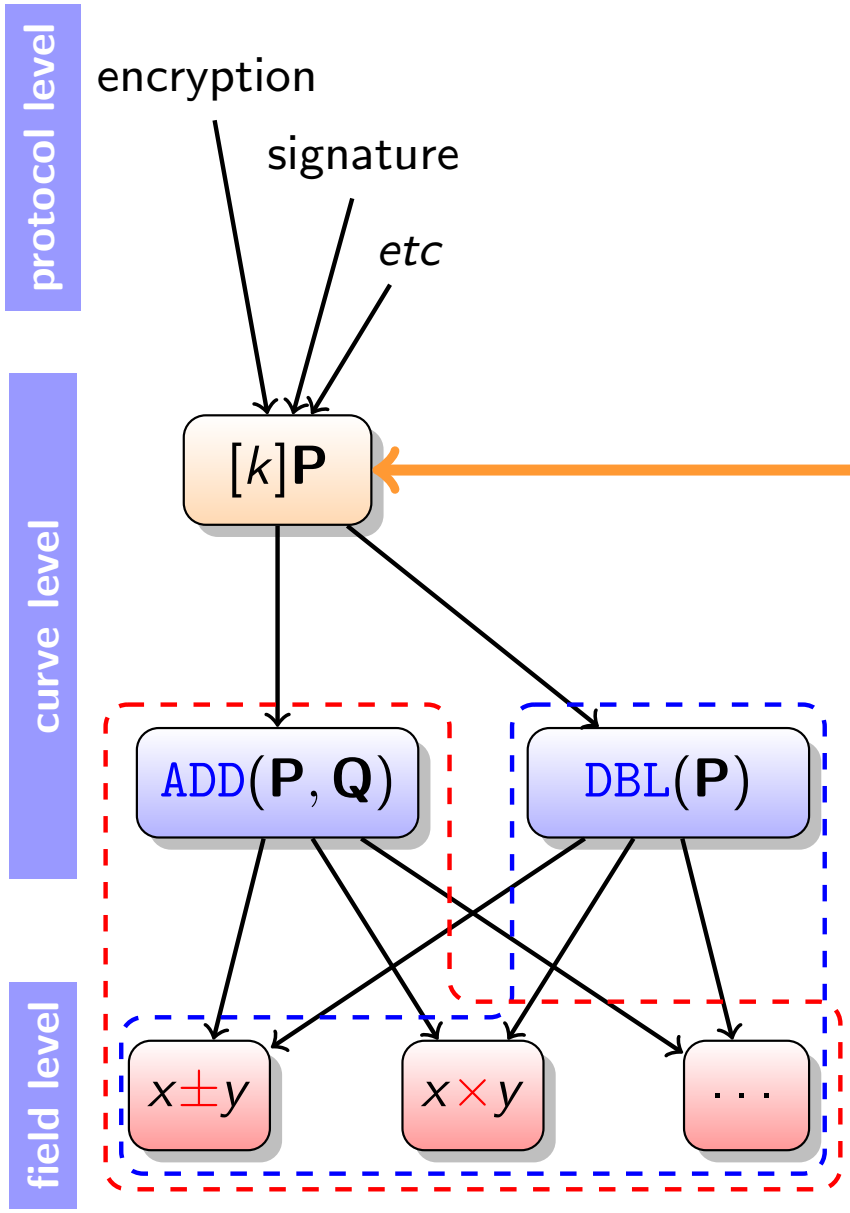

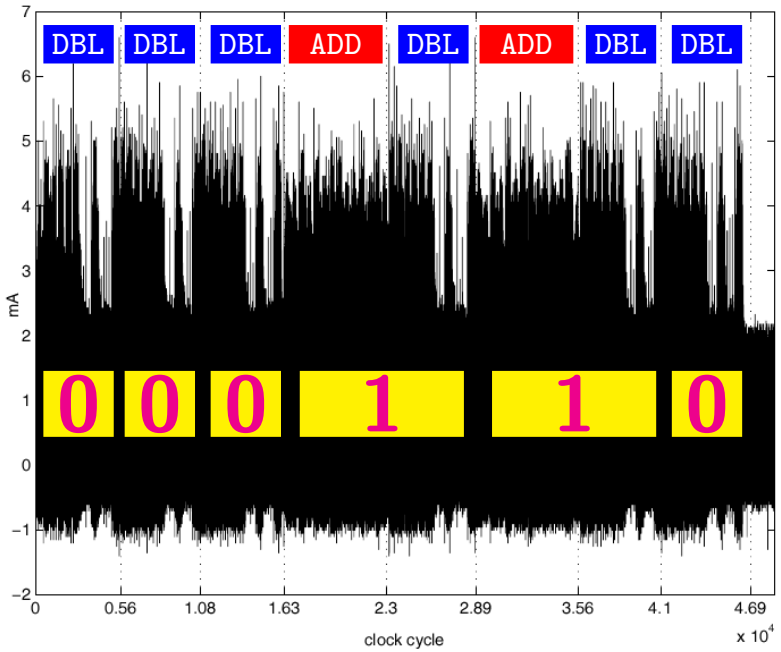

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- simple power analysis (& variants)
- differential power analysis (& variants)
- horizontal/vertical/templates/...attacks

Fault Injection Attacks

Objective: alter the correct functioning of a system "from outside"

Fault effects examples:

- modify a value in a register
- modify a value in the memory hierarchy
- modify an address (data location or code location)
- modify a control signal (e.g. status flag, branch direction)
- skip/modify the instruction decoding
- delay/advance propagation of internal control signals
- etc.

Also called perturbation attacks

Fault Injection Techniques

Typical techniques:

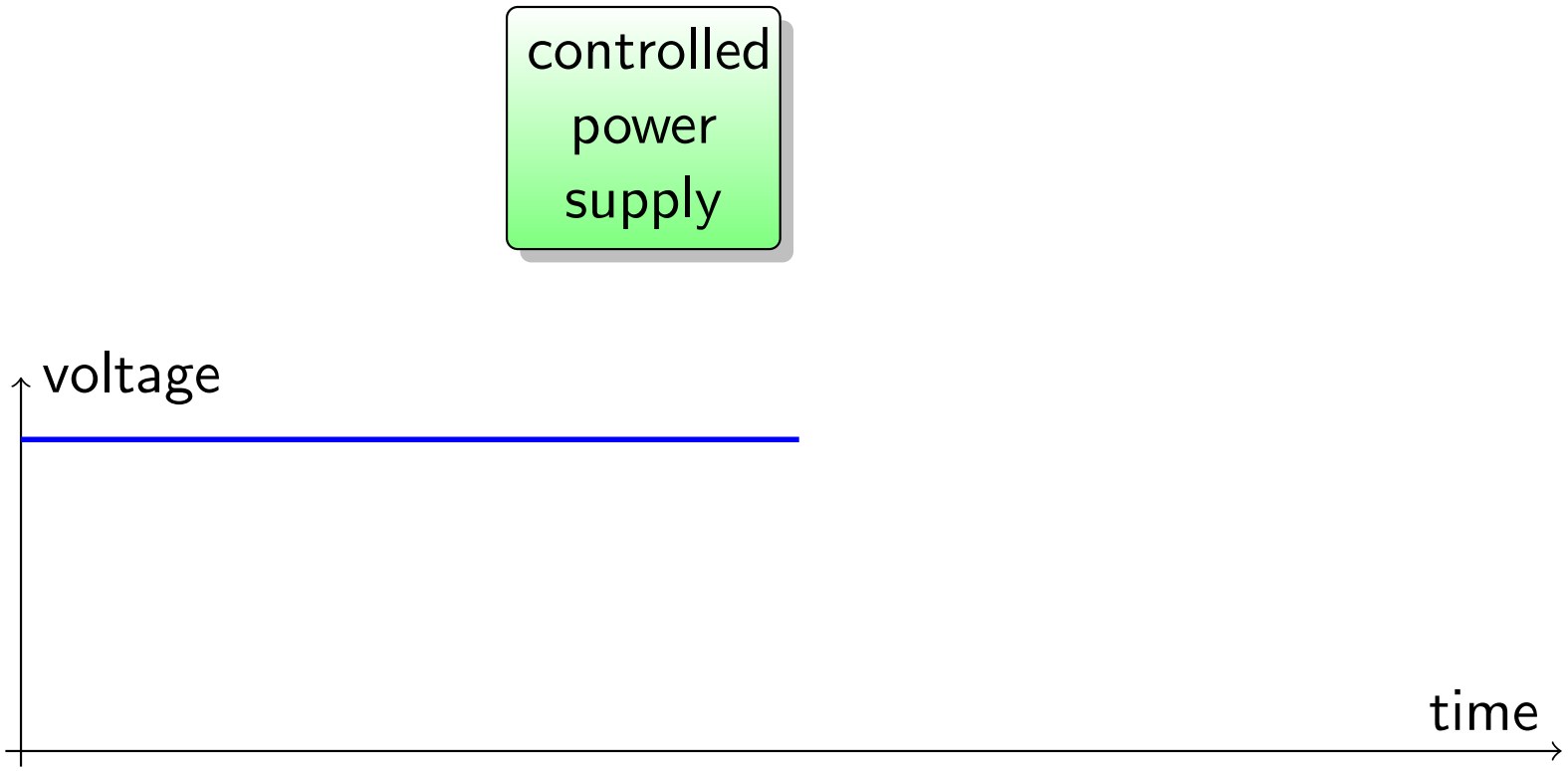
- perturbation in the power supply voltage
- perturbation of the clock signal
- temperature (over/under-heating the chip)
- radiation or electromagnetic (EM) disturbances
- exposing the chip to intense lights or beams
- etc

Accuracy:

- time: part of clock cycle, clock cycle, code block (instruction sequence)
- space: gate, block, unit, core, chip, package
- value: set to a specific value, bit flip, stuck-at 0 or 1, random modification

Perturbation on the Power Supply

Principle:



- Nominal power supply (e.g. $\approx [0.7, 1.2]$ V for current technologies)

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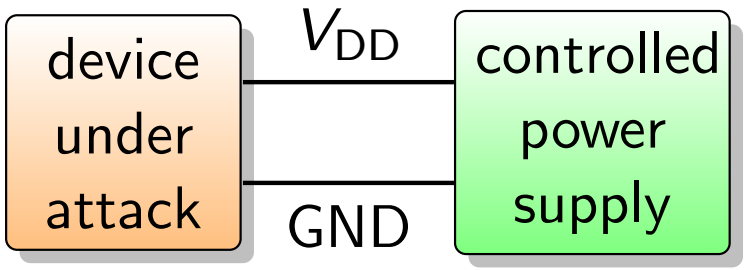

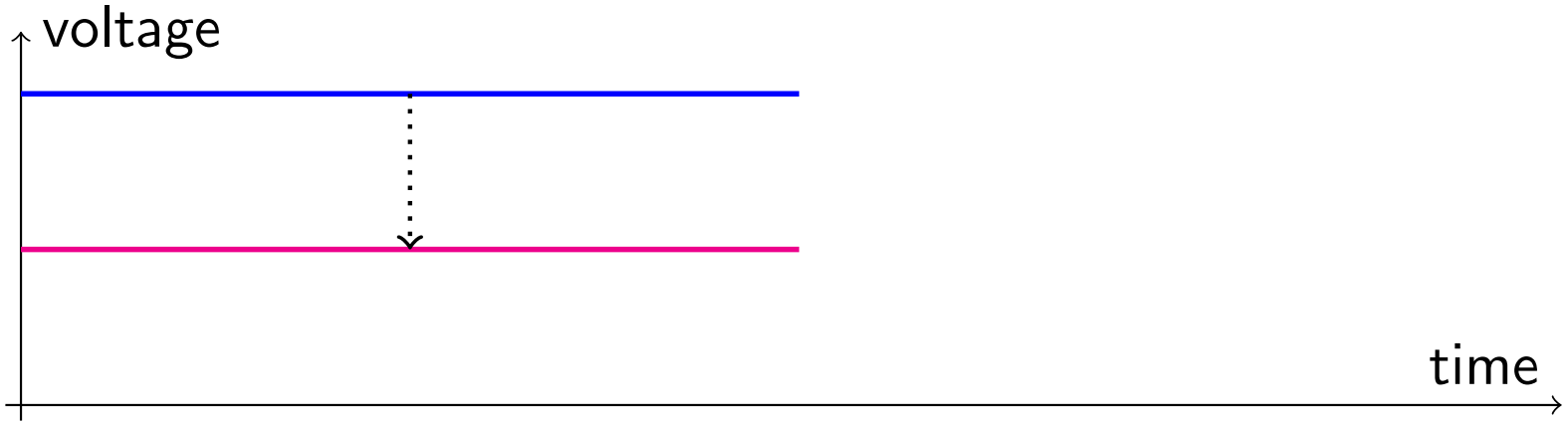

- Nominal power supply (e.g. $\approx [0.7, 1.2]$ V for current technologies)
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Perturbation on the Power Supply

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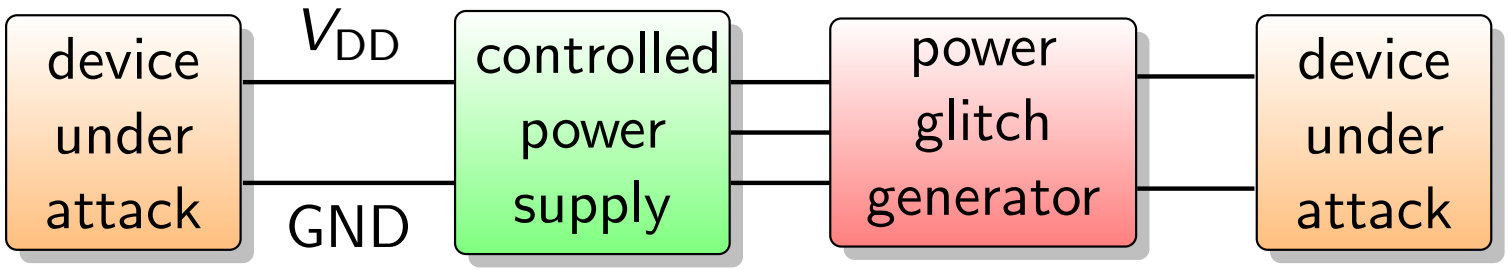

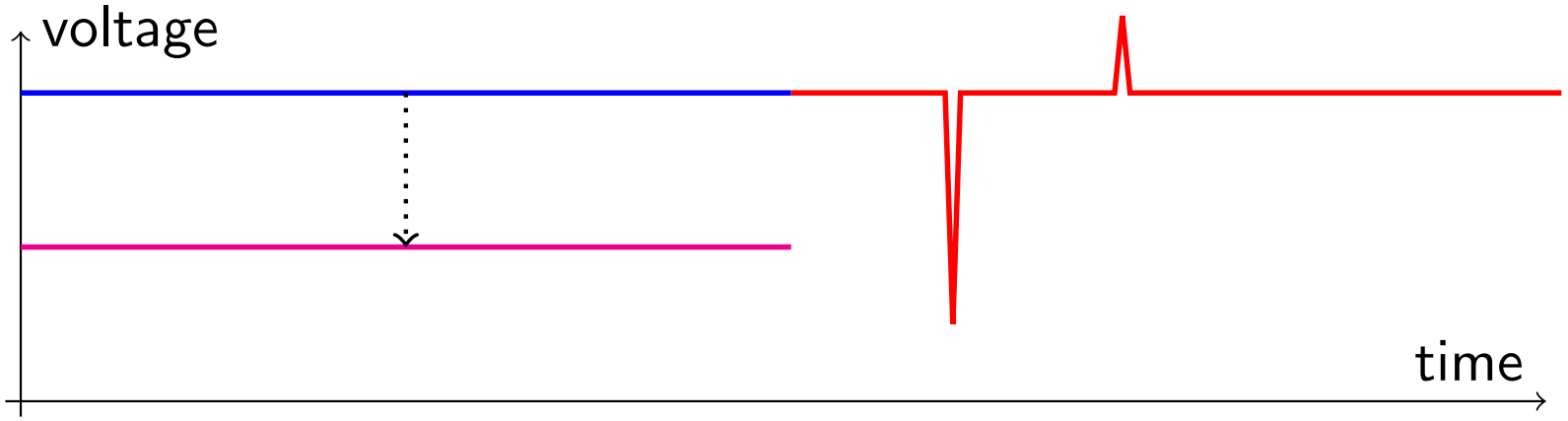

- Nominal power supply (e.g. $\approx [0.7, 1.2]$ V for current technologies)
- Non-nominal constant power supply (e.g. 0.7 V instead of 1.2 V)
- Glitches (dips, spikes) in the power supply at some selected moments

Under Powering Example

Source: paper [19] presented at EDCC 2008 conference

Setup: 130 nm smart card (1.2 V nominal V_{DD}) with AES crypto-processor

Measurement campaign: triples (msg, key, cypher) recorded for 100 V_{DD} in [775, 825] mV over 20,000 encryptions with comparison to a (RTL) simulation for one byte corruption in the state matrix at various rounds

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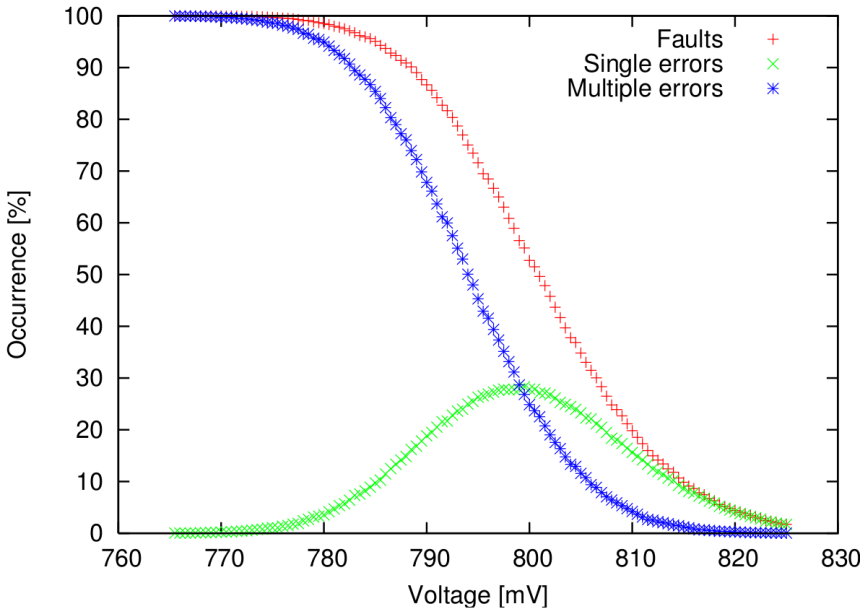

Observed behavior is compatible with setup violation model on a critical path (bell shape due to only one or multiple paths)

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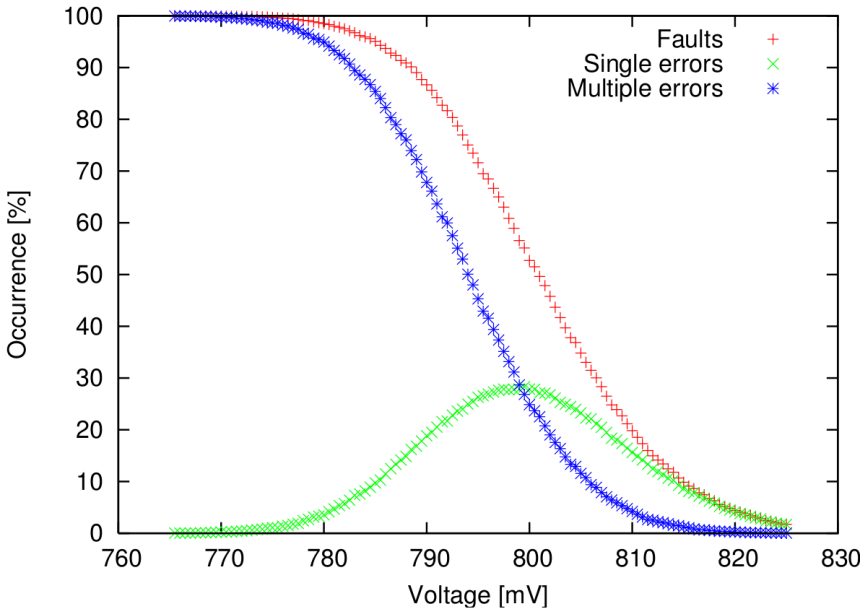
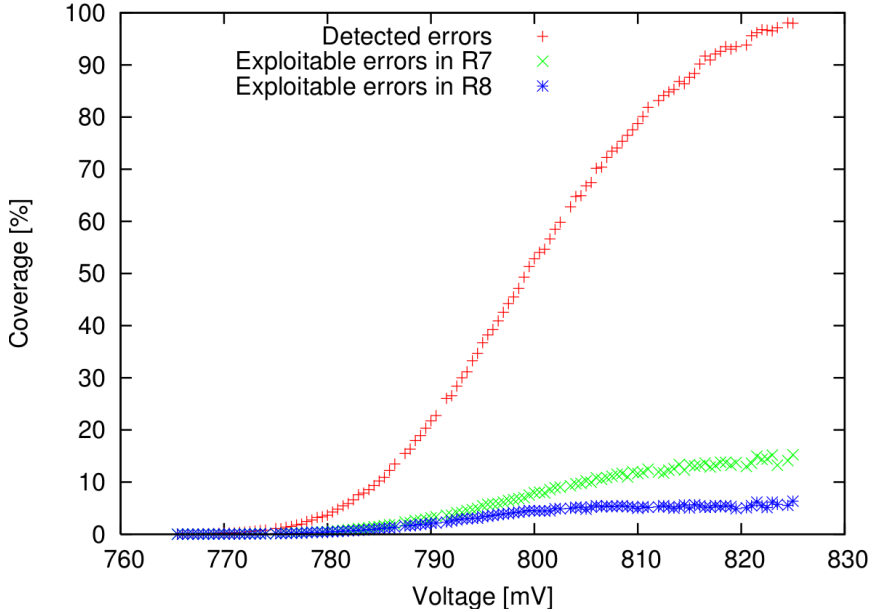


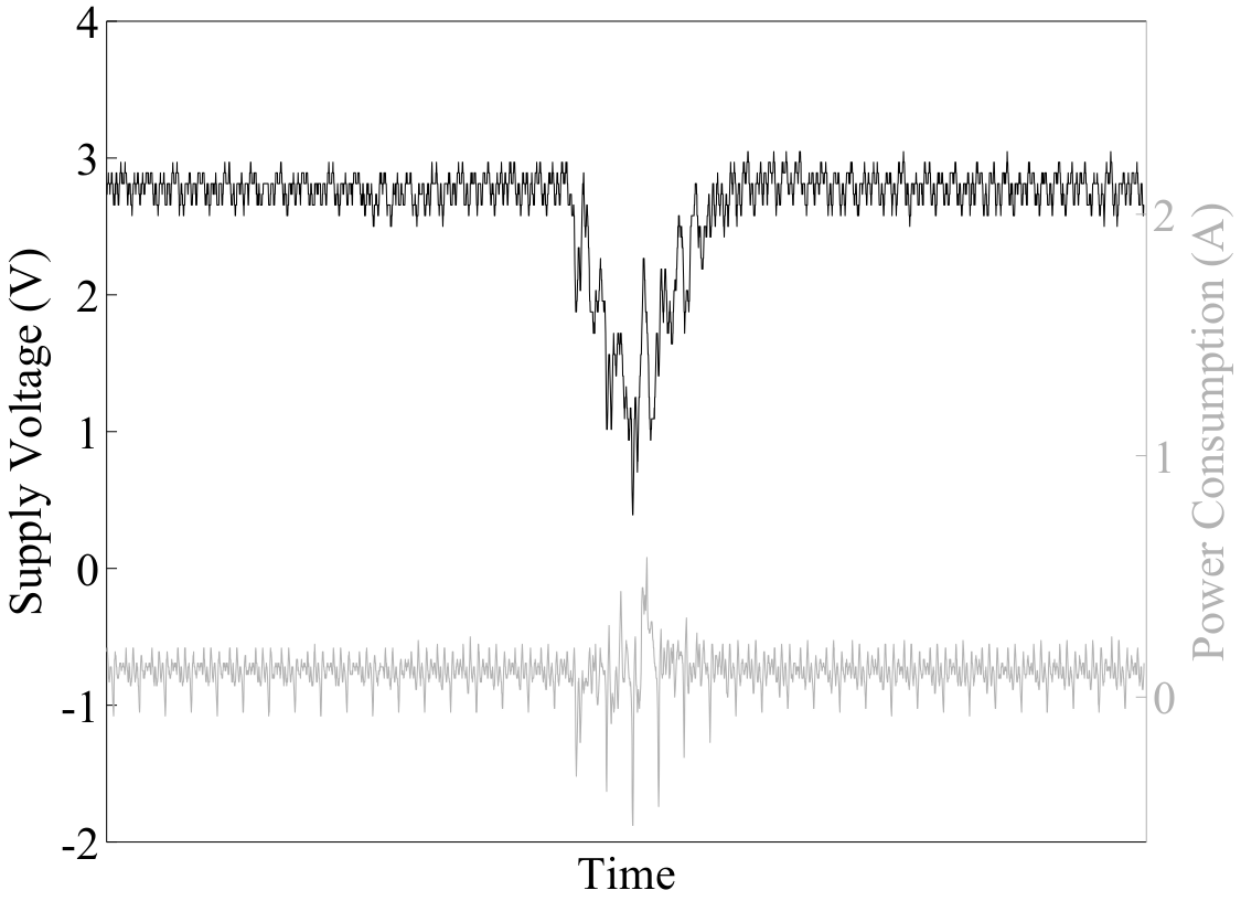


Observed behavior is compatible with setup violation model on a critical path (bell shape due to only one or multiple paths)

Power Glitching Example

Source: FDTC 2008 conference paper [18]

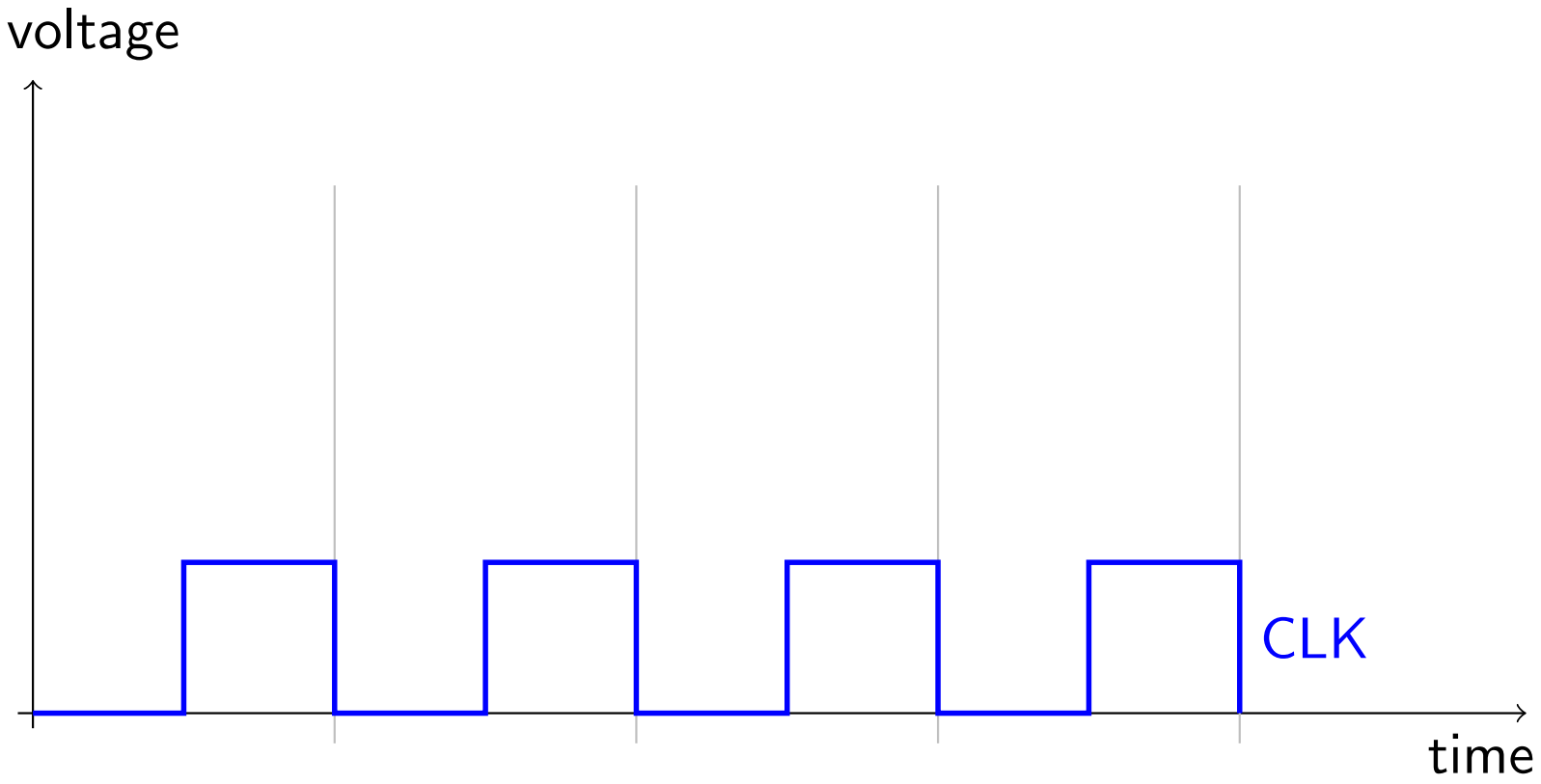
Setup: AVR microcontroller with RSA implementation



Attack result: a power glitch causes to skip some instruction

Perturbation on the External Clock

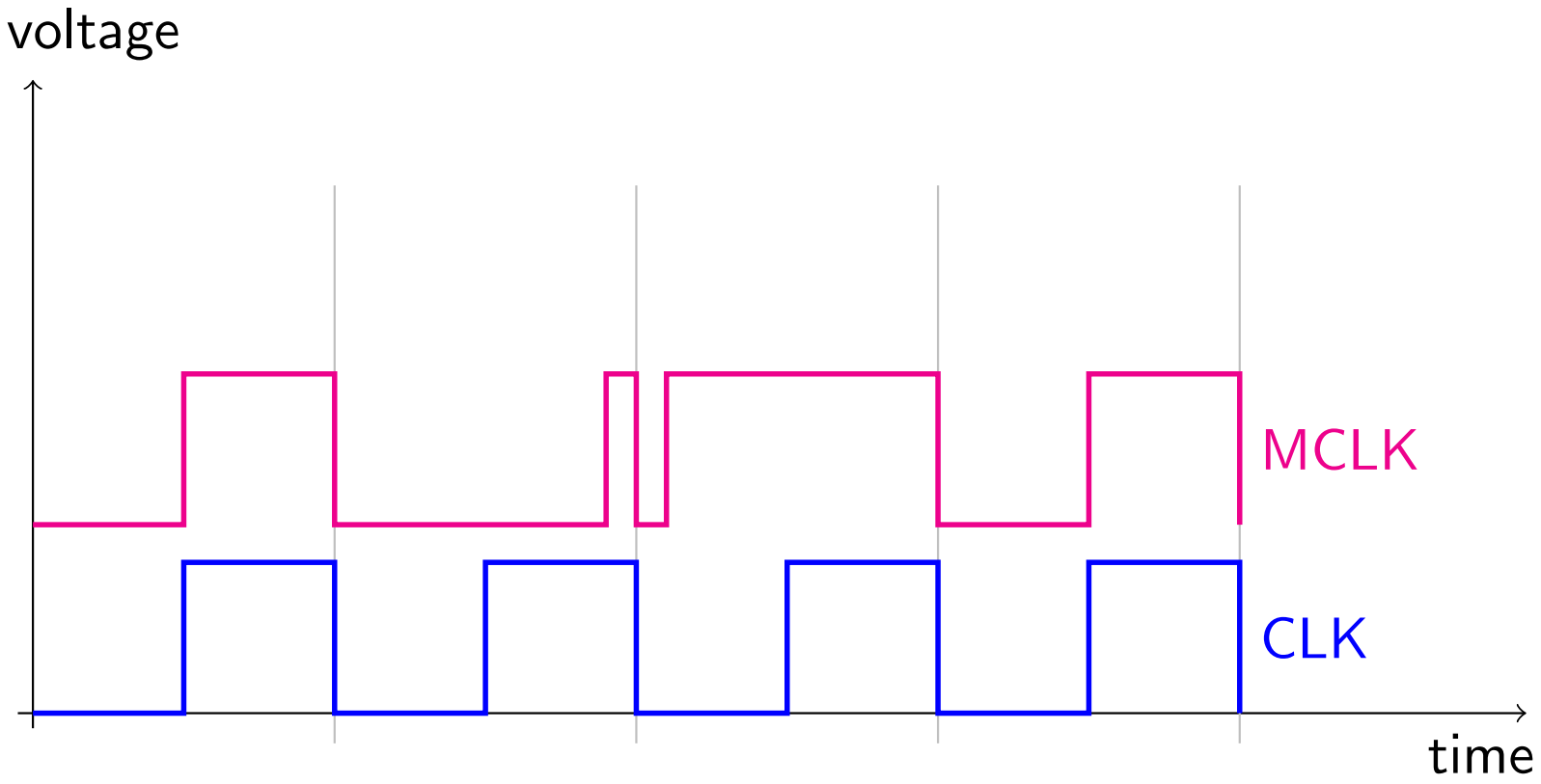
Principle:



- Normal clock (at a given frequency, duty cycle $\approx 50\%$)

Perturbation on the External Clock

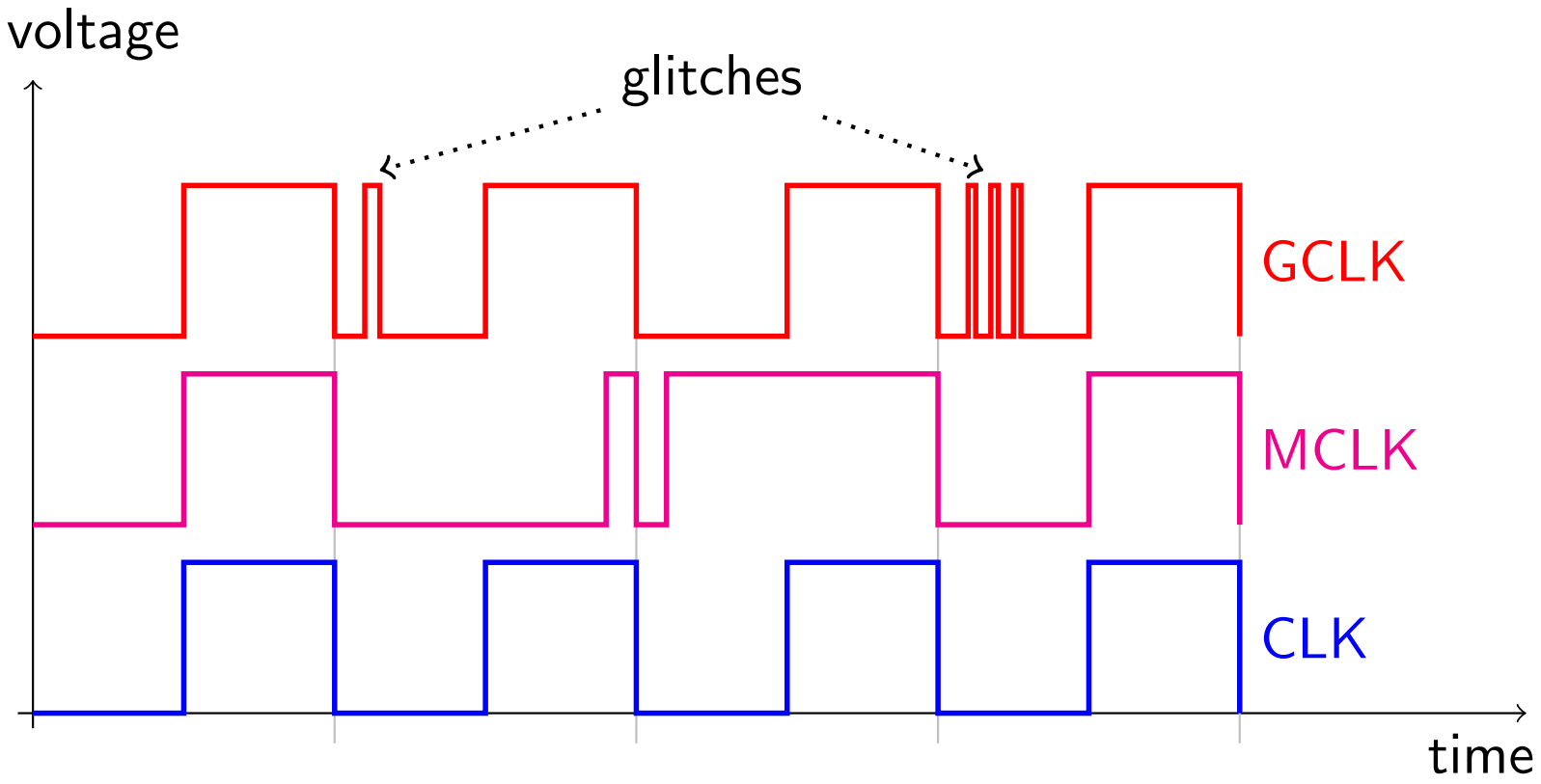
Principle:



- Normal clock (at a given frequency, duty cycle $\approx 50\%$)
- Clock with a modified duty cycle

Perturbation on the External Clock

Principle:



- Normal clock (at a given frequency, duty cycle $\approx 50\%$)
- Clock with a modified duty cycle
- Glitched clock
- Etc.

Glitchy Clock Generation Example

Source: paper [10] published in J. Crypto. Eng. 2011

Setup: Virtex-II Pro FPGA (on SASEBO card) used to generate a "glitchy" clock for several programmable time parameters

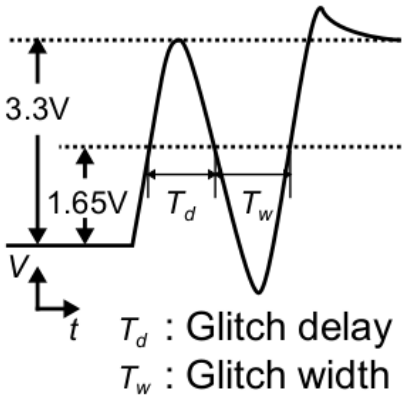


Fig. 3. Image of glitchy-clock cycle.

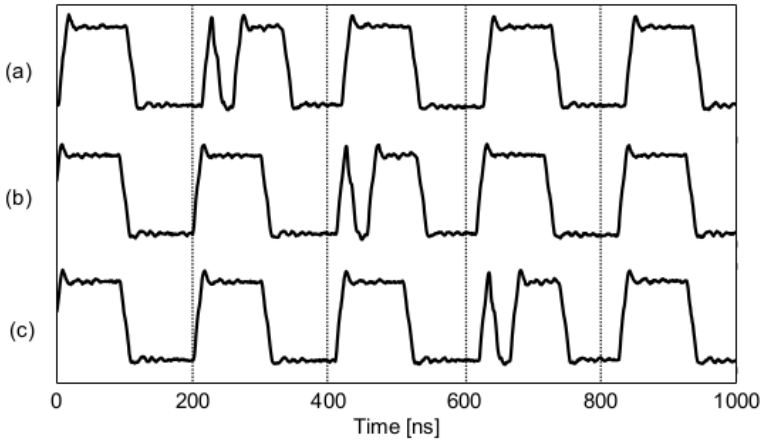
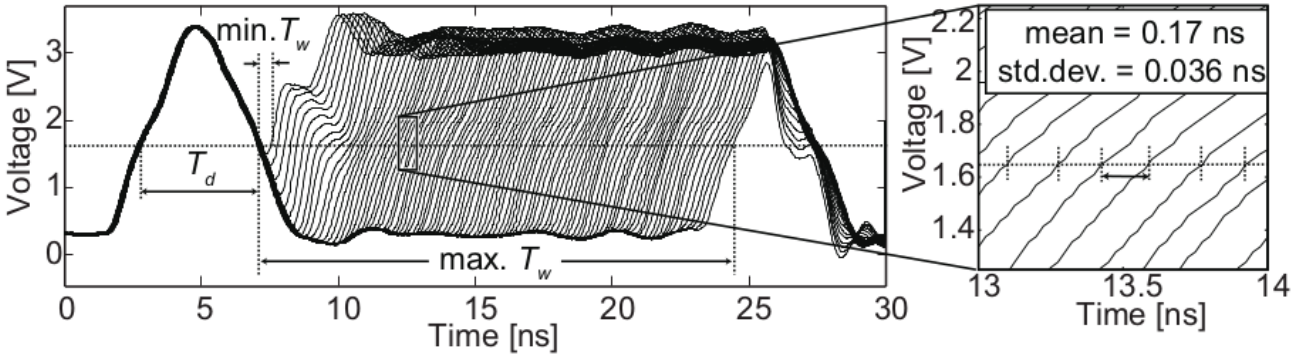


Fig. 4. Examples of glitchy-clock signals.



Clock Glitch Attack Example

Source: paper [1] presented at FDTC 2011 conference

Setup: AVR ATMega 163 microcontroller @ 1MHz

mode	glitch period	cycle	instruction	opcode (bin)
normal	-	i	`NOP`	0000 0000 0000 0000
normal	-	$i+1$	`EOR R15,R5`	0010 0100 1111 0101

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mode	glitch period	cycle	instruction	opcode (bin)
normal	-	i	`NOP`	0000 0000 0000 0000
normal	-	$i+1$	`SER R18`	1110 1111 0010 1111

Clock Glitch Attack Example

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glitch	59 ns	$i+1$	`NOP`	0000 0000 0000 0000

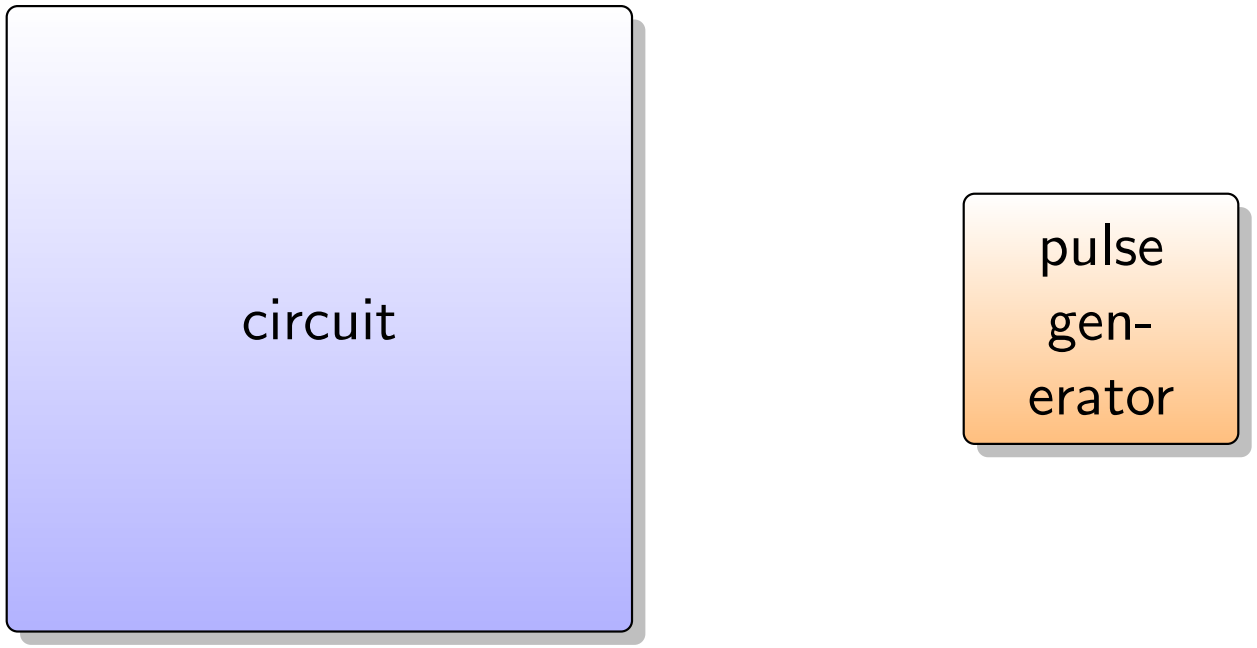
mode	glitch period	cycle	instruction	opcode (bin)
normal	-	i	`NOP`	0000 0000 0000 0000
normal	-	$i+1$	`SER R18`	1110 1111 0010 1111
glitch	61 ns	$i+1$	`LDI R18,0xEF`	1110 1110 0010 1111
glitch	60 ns	$i+1$	`SBC R12,R15`	0000 1000 0010 1111
glitch	59 ns	$i+1$	`NOP`	0000 0000 0000 0000

mode	glitch period	cycle	instruction	opcode (bin)
normal	-	i	`TST R12`	0010 0000 1100 1100
normal	-	$i+1$	`BREQ PC+0x02`	1111 0000 0000 1001
normal	-	$i+2$	`SER R26`	1110 1111 1010 1111

mode	glitch period	cycle	instruction	opcode (bin)
normal	-	i	`TST R12`	0010 0000 1100 1100
normal	-	$i+1$	`BREQ PC+0x02`	1111 0000 0000 1001
normal	-	$i+2$	`SER R26`	1110 1111 1010 1111
glitch	57 ns	$i+2$	`LDI R26,0xEF`	1110 1110 1010 1111
glitch	56 ns	$i+2$	`LDI R26,0xCF`	1110 1100 1010 1111
glitch	52 ns	$i+2$	`LDI R26,0x0F`	1110 0000 1010 1111
glitch	45 ns	$i+2$	`LDI R16,0x09`	1110 0000 0000 1001
glitch	32 ns	$i+2$	`LD R0,Y+0x01`	1000 0000 0000 1001
glitch	28 ns	$i+2$	`LD R9,Y`	1000 0000 0000 1000
glitch	27 ns	$i+2$	`LDI R16,0x09`	1110 0000 0000 1001
glitch	15 ns	$i+2$	`BREQ PC+0x02`	1111 0000 0000 1001

Electromagnetic Perturbations

Principle:



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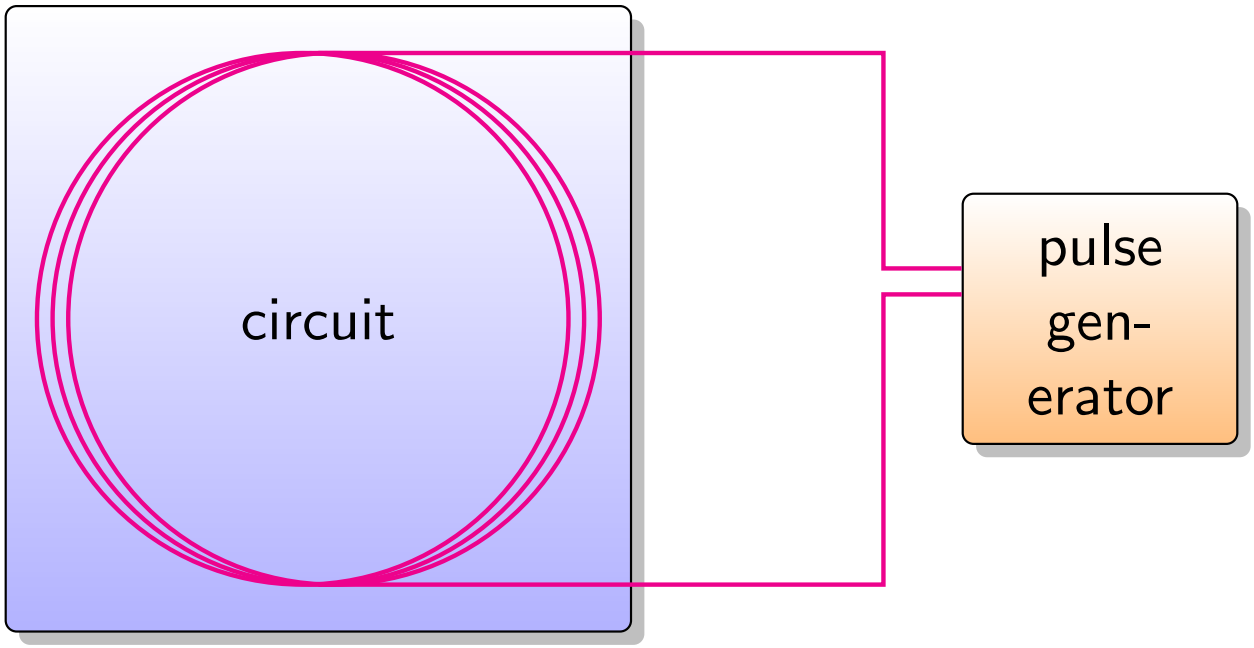

- large antenna

Electromagnetic Perturbations

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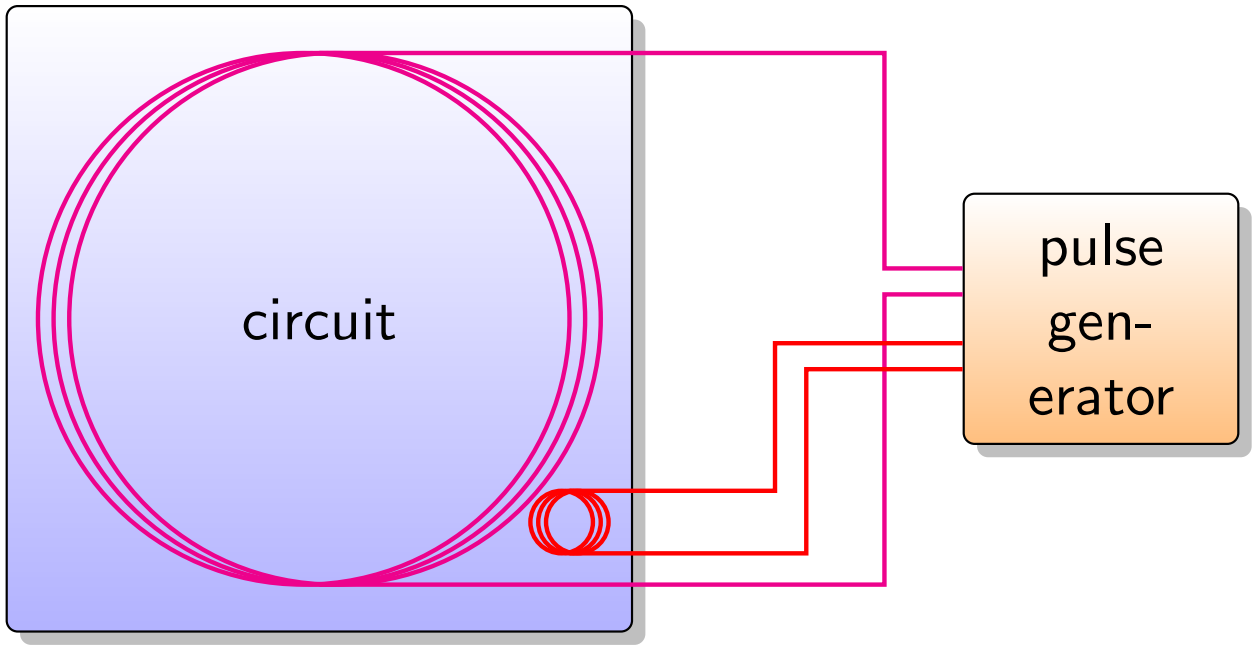

- large antenna
- micro-antenna

Electromagnetic Perturbations

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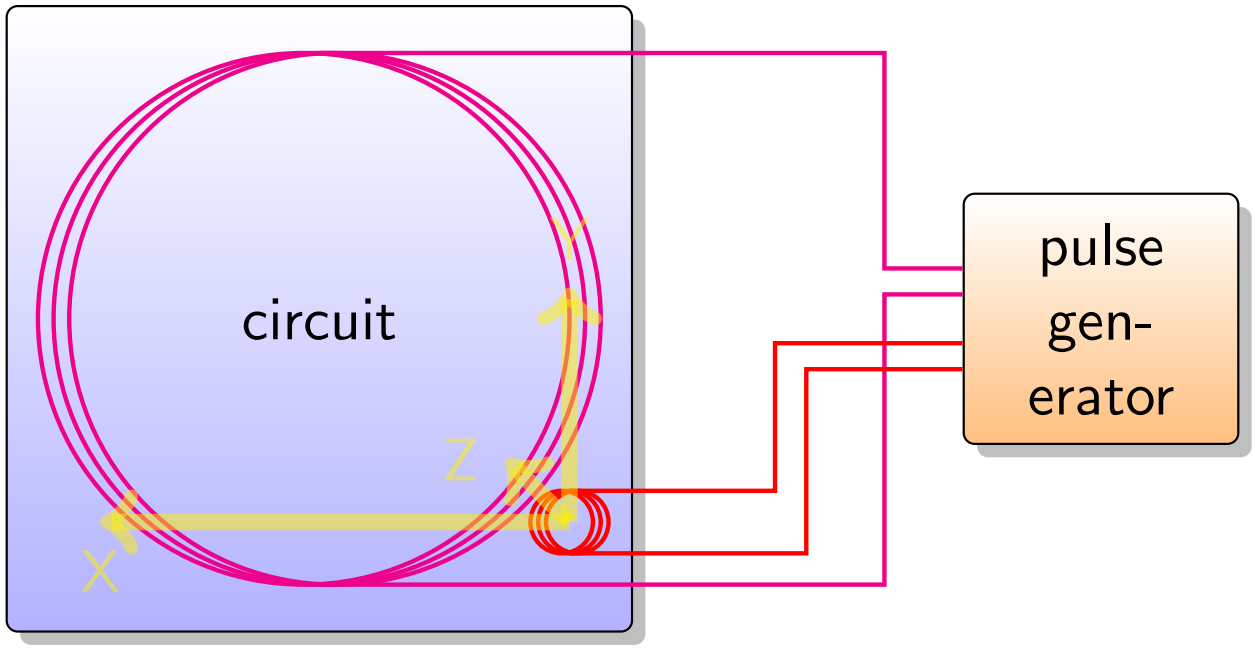


- large antenna
- micro-antenna with motorized (X,Y,Z) stage/table

Electromagnetic Attack Example

Source: article [12] presented at FDTC 2013 conference

Setup: 32-b Cortex-M3 ARM microprocessor (CMOS 130 nm SoC at 56 MHz), magnetic antenna with pulses in [-200, 200] V and [10, 200] ns

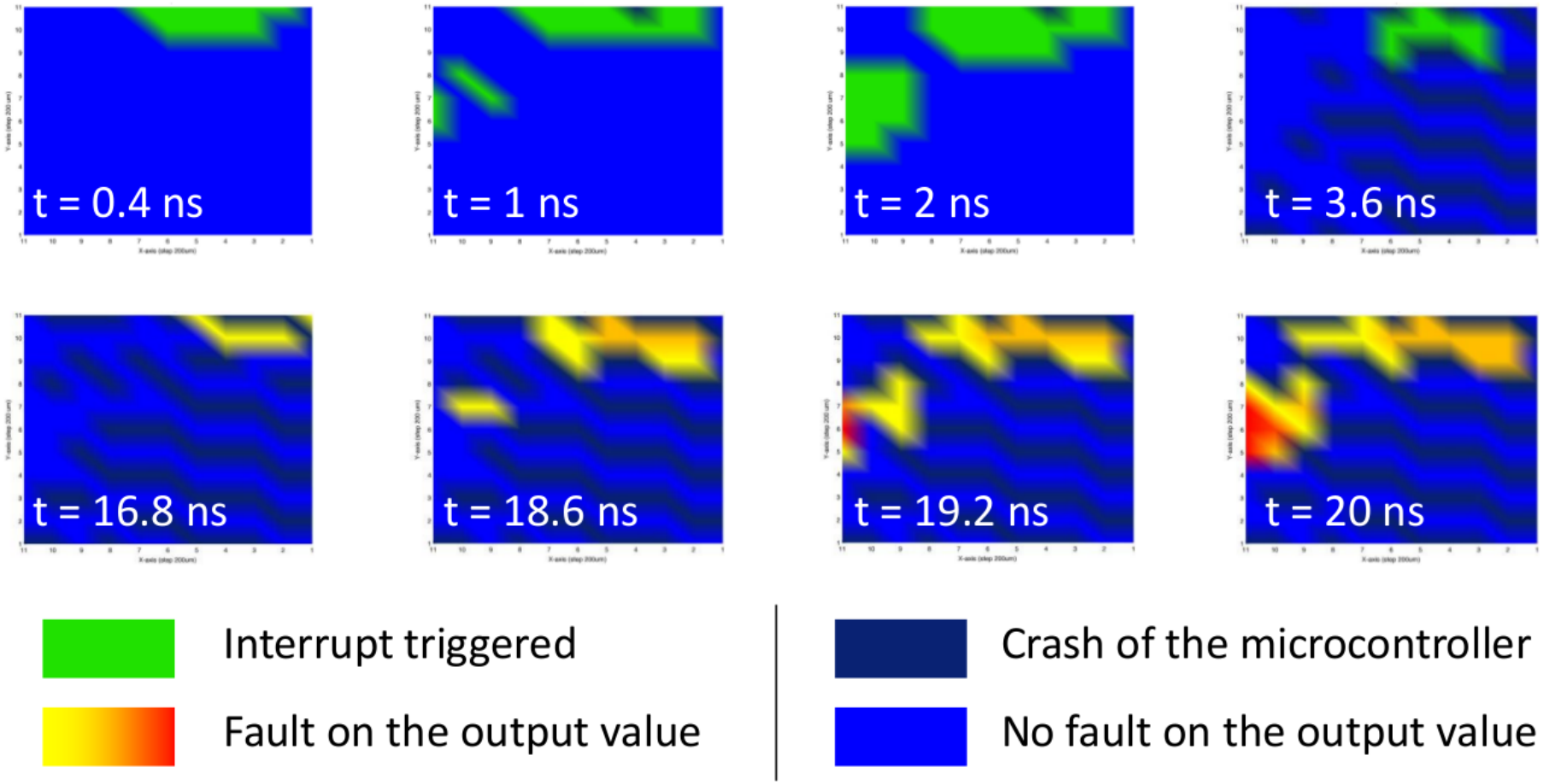


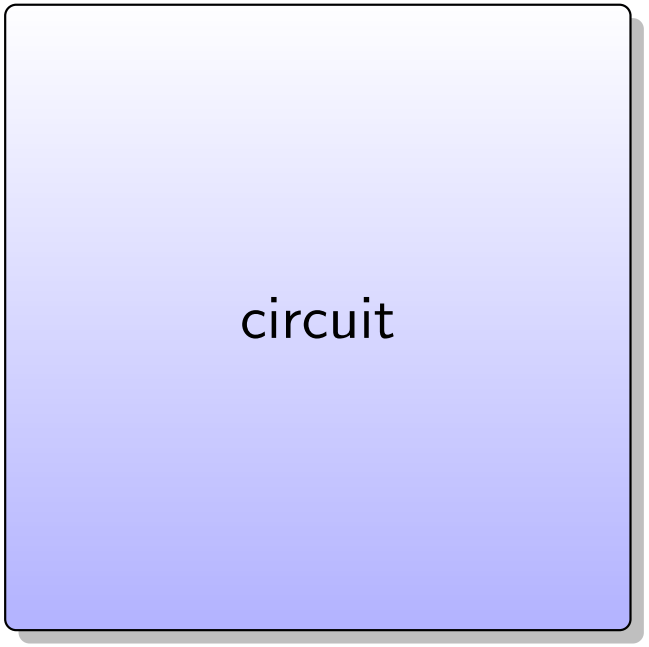
Figure 3: Impact of the probe's position

Loaded value: 12345678

Pulse voltage [V]	Loaded value	Occurrence rate [%]
170	1234 5678	100
172	1234 5678	100
174	9234 5678	73
176	FE34 5678	30
178	FFF4 5678	53
180	FFFD 5678	50
182	FFFF 7F78	46
184	FFFF FFFB	40
186	FFFF FFFF	100
188	FFFF FFFF	100
190	FFFF FFFF	100

Lights / Lasers

Principle:



Lights / Lasers

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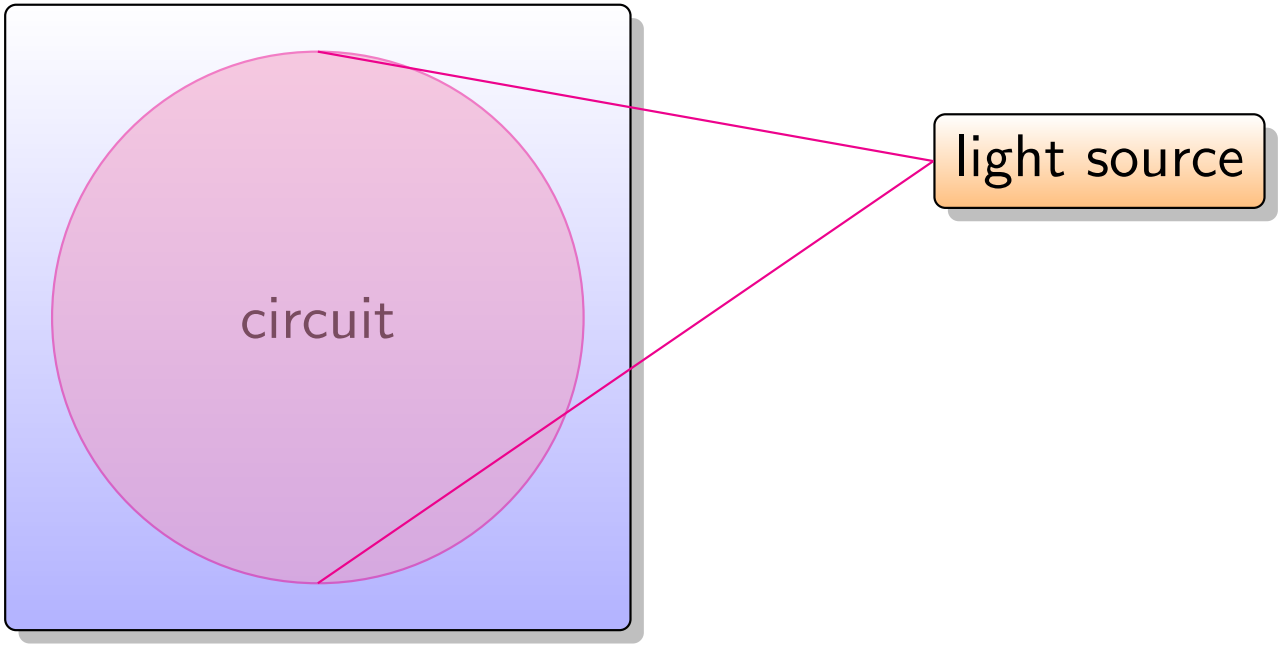

- large illuminated area (flash light with microscope)

Lights / Lasers

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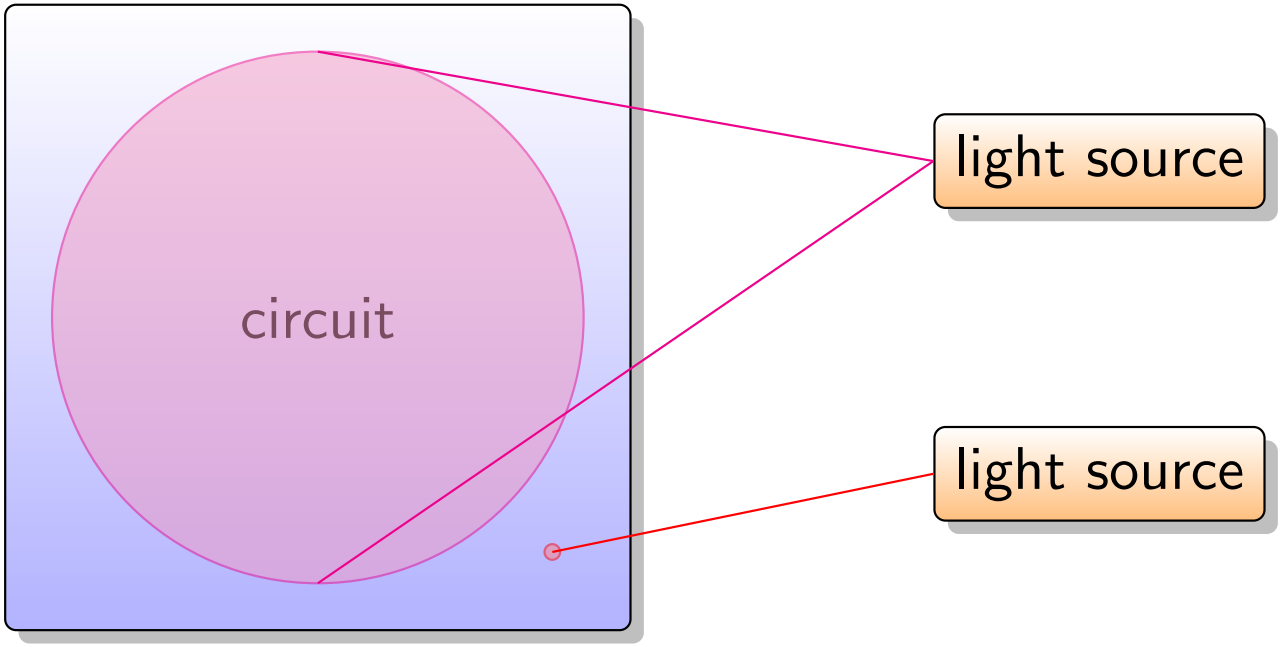

- large illuminated area (flash light with microscope)
- small "spot" (laser with variable locations)

Differential Fault Analysis

Most of time, exploiting only one fault does not provide enough information

- Accurately injecting fault is difficult
- The fault causes a few perturbations

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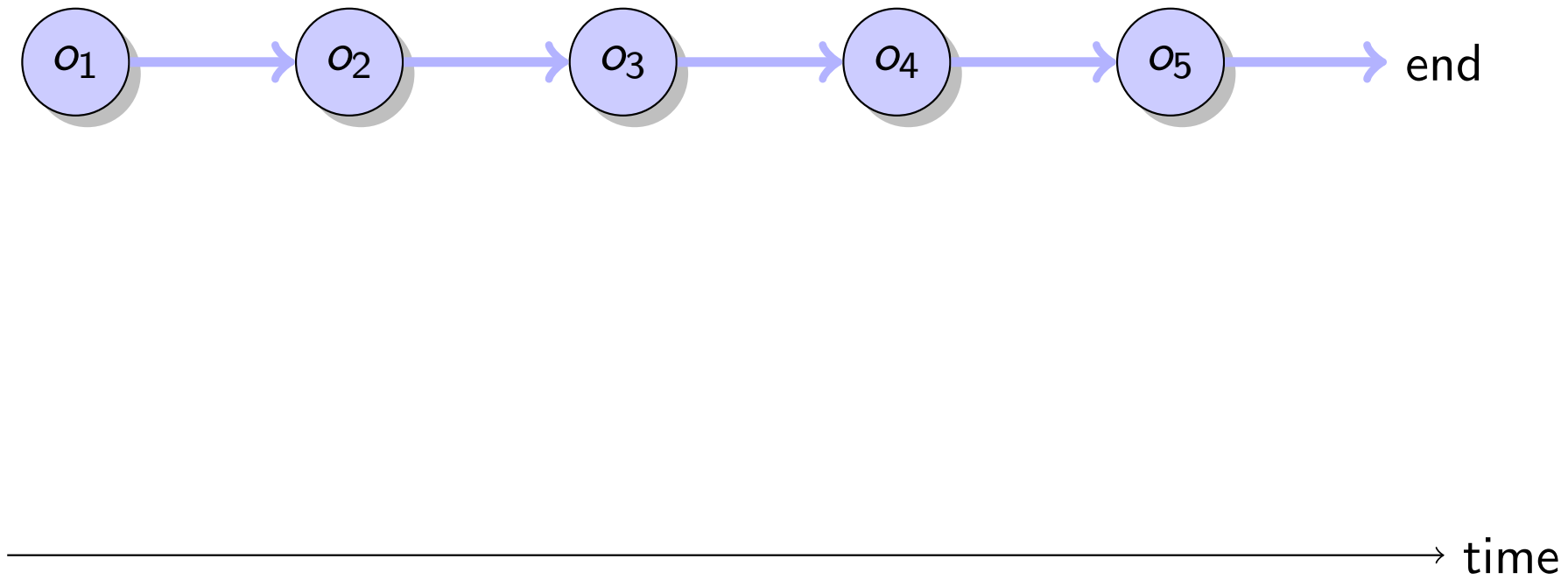
Then, use statistical correlation(s)

Safe Error Attack

Principle: exploit the link (or the lack of link) between injected fault(s) during "useful" (or "useless") operations and the final result



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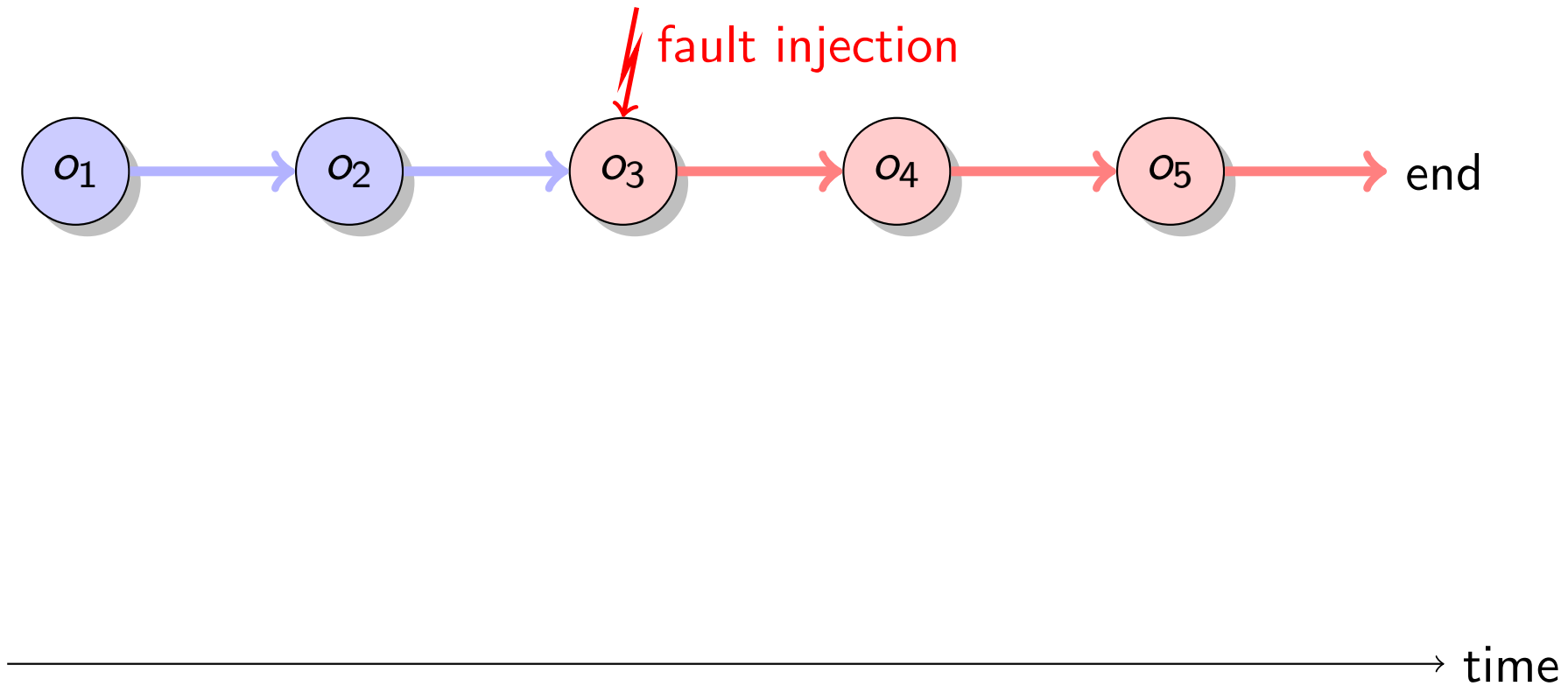

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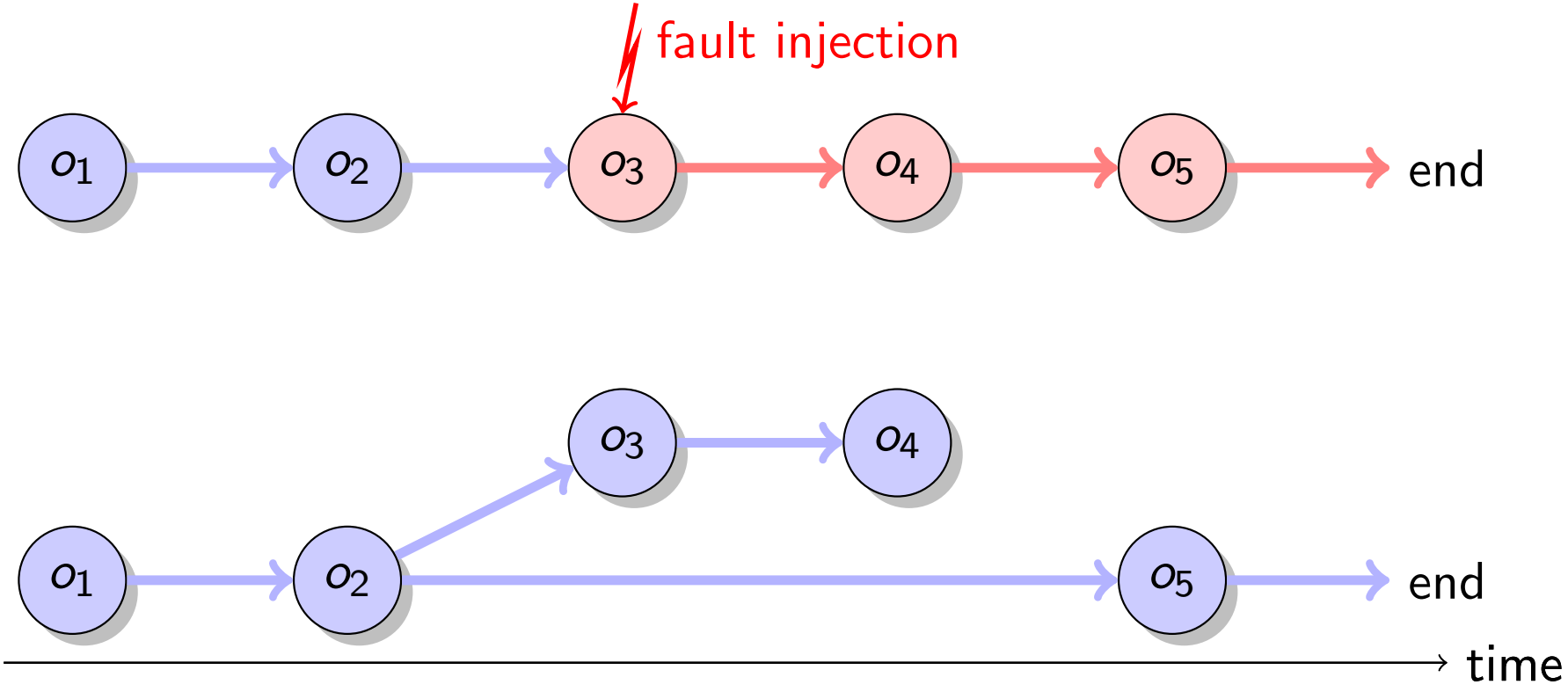

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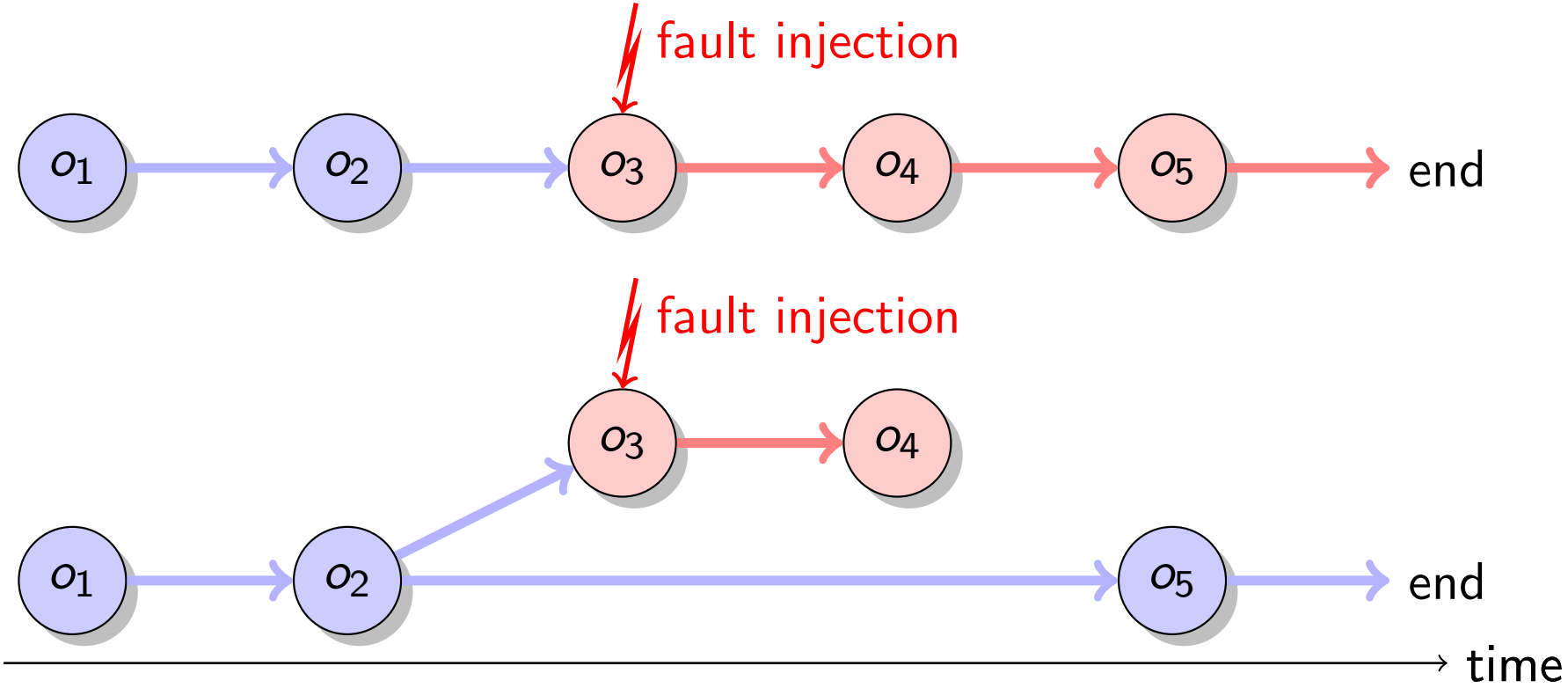
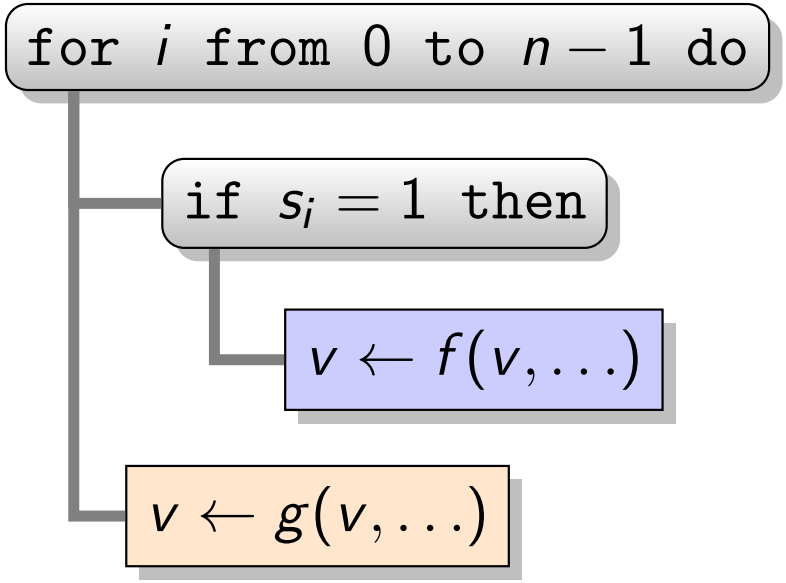
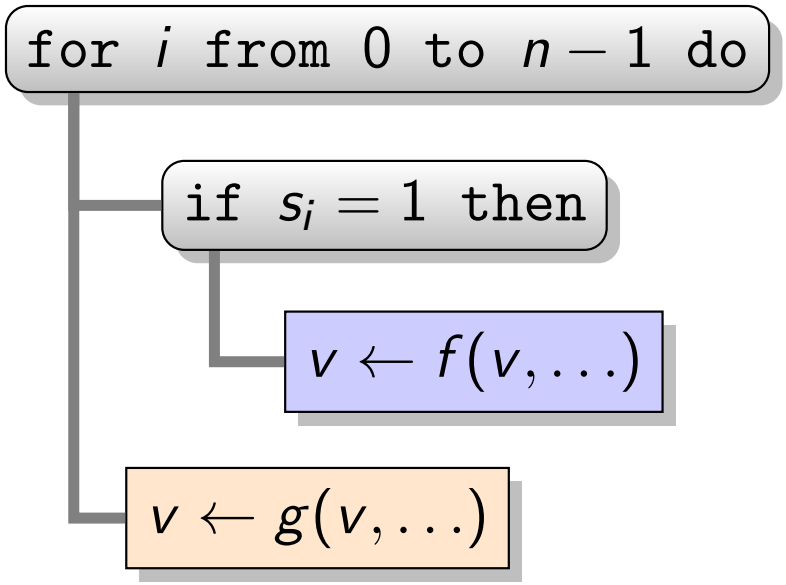


Safe Error Attack Example in Asymmetric Crypto



Safe Error Attack Example in Asymmetric Crypto

WEAK against SPA



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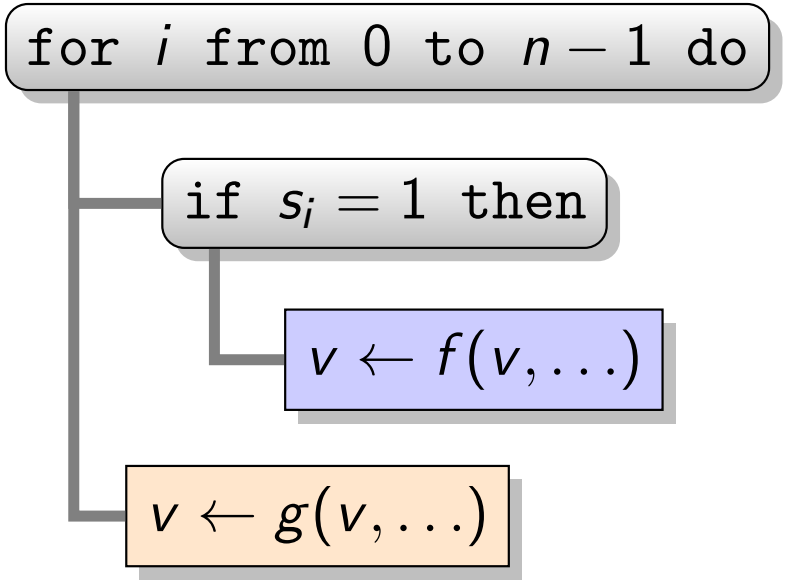

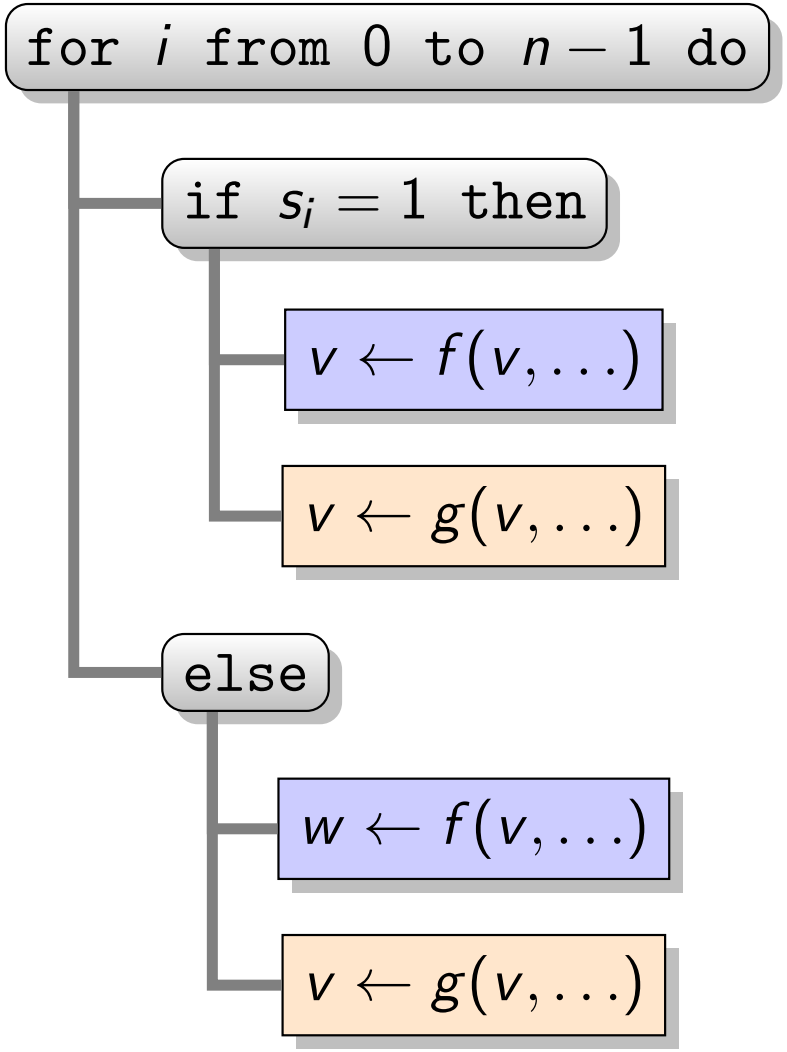

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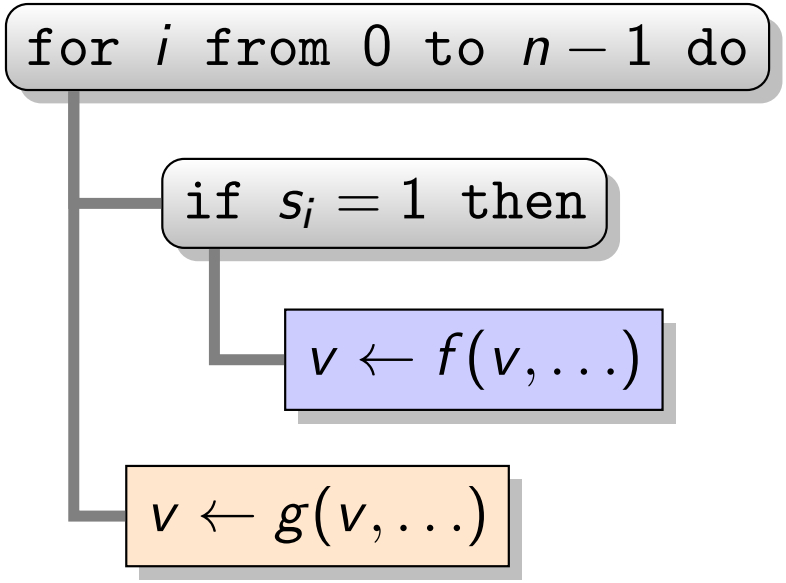
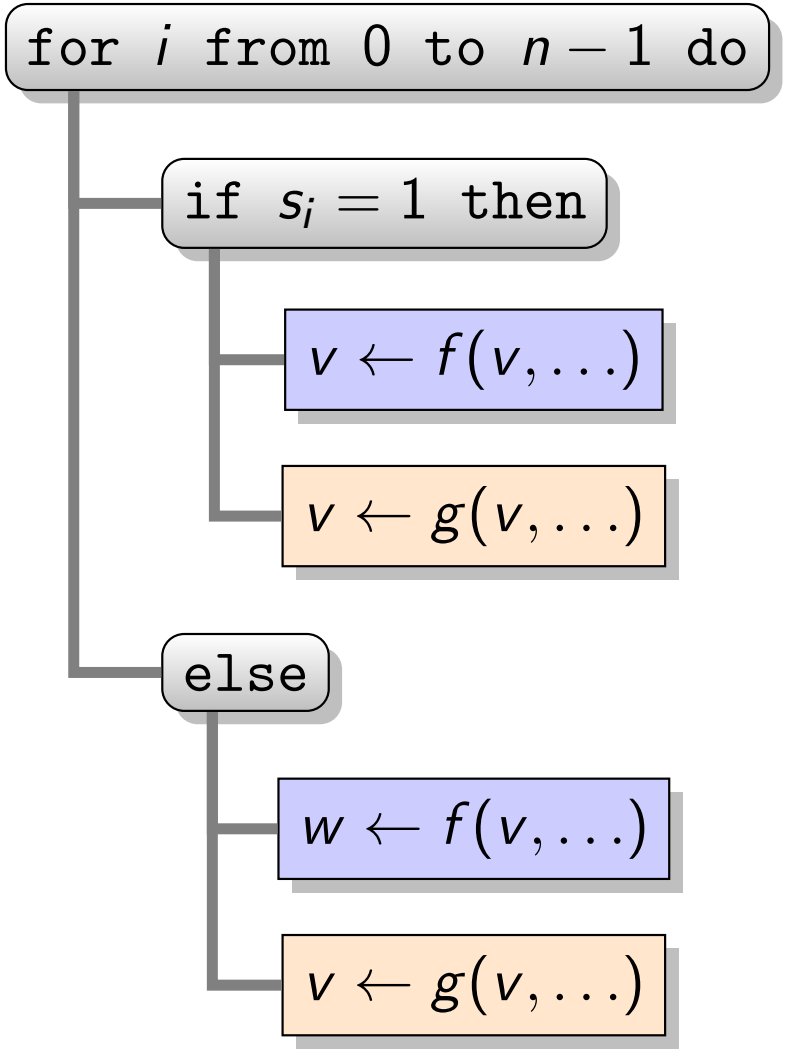


WEAK against SEA



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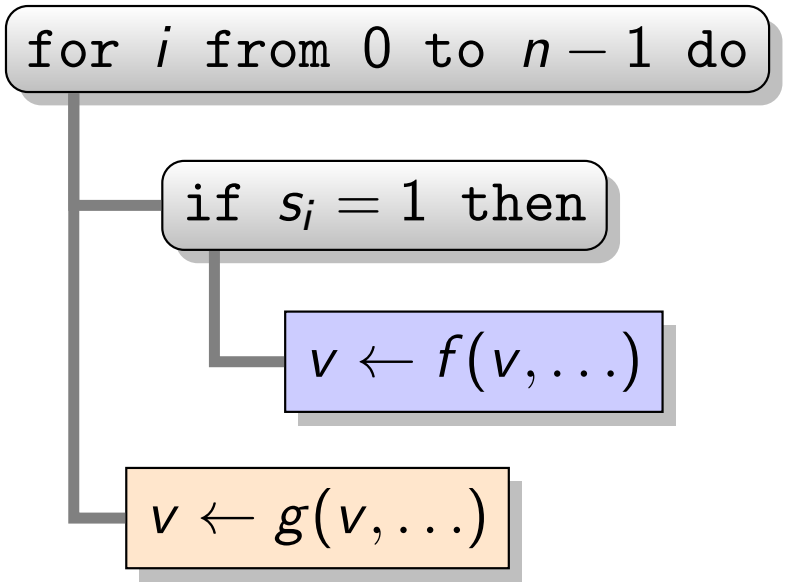

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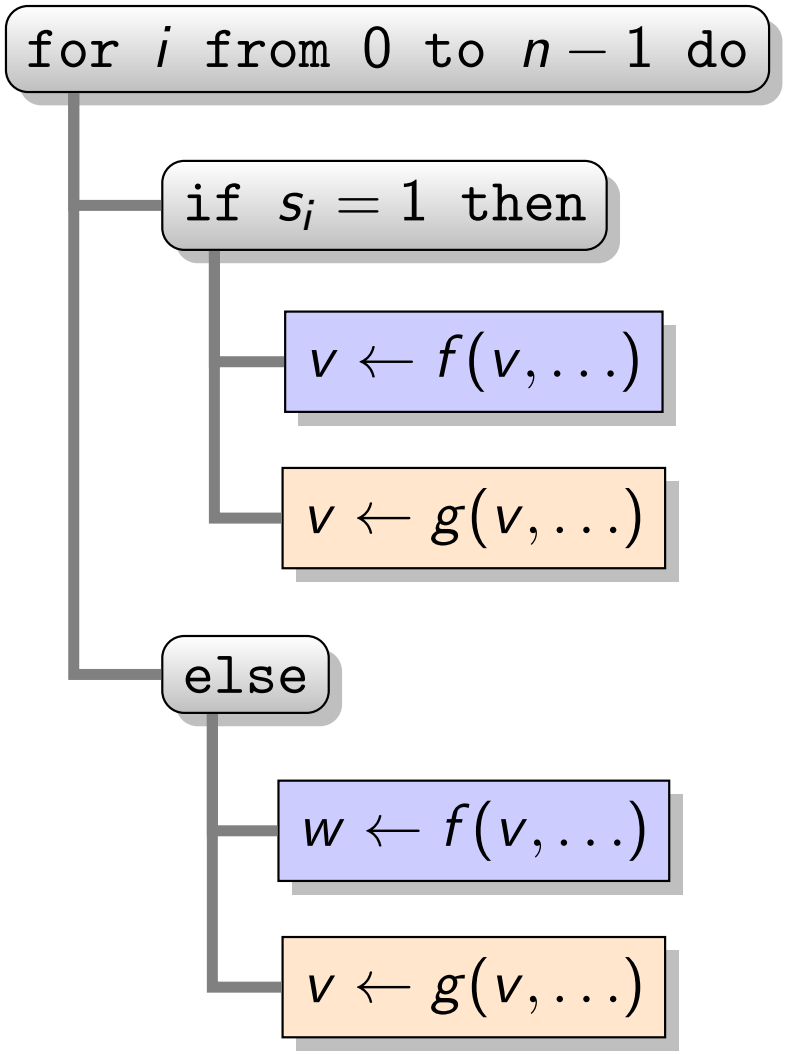

Useless or dummy operations are a bad idea

Fault Attack Example: Bit Flip on RSA Decryption

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- choose a plaintext message $\mathcal{M}$

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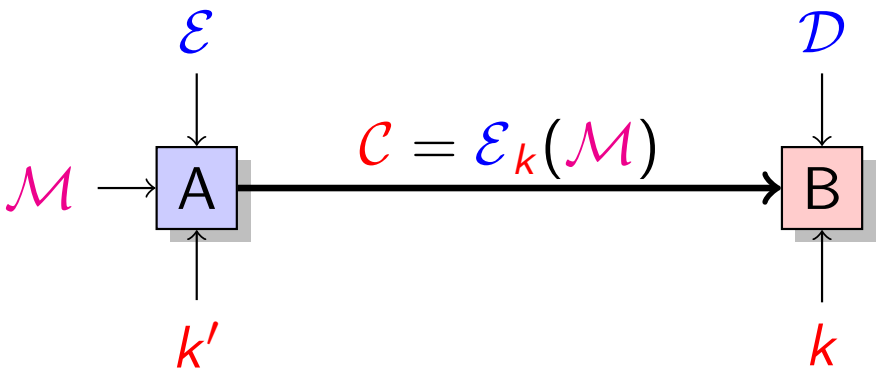

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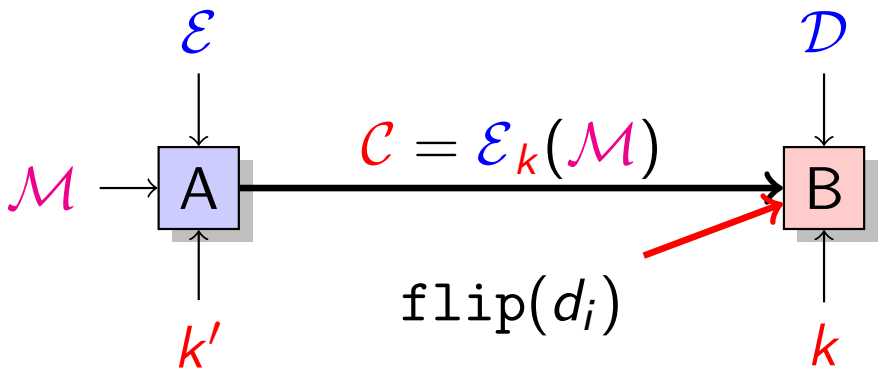

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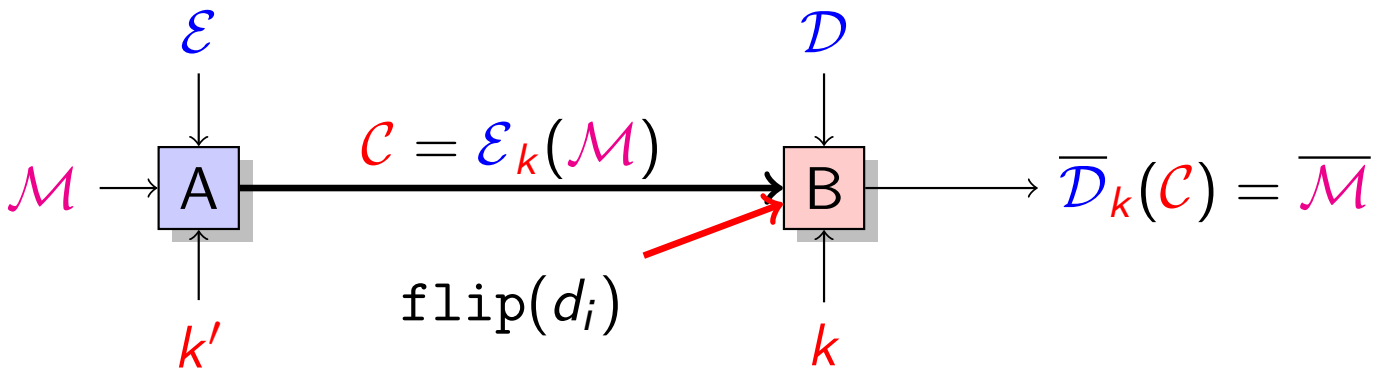

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- compute $\frac{\overline{\mathcal{M}}}{\mathcal{M}} = \frac{c^{2^i \overline{d_i}}}{c^{2^i d_i}}$

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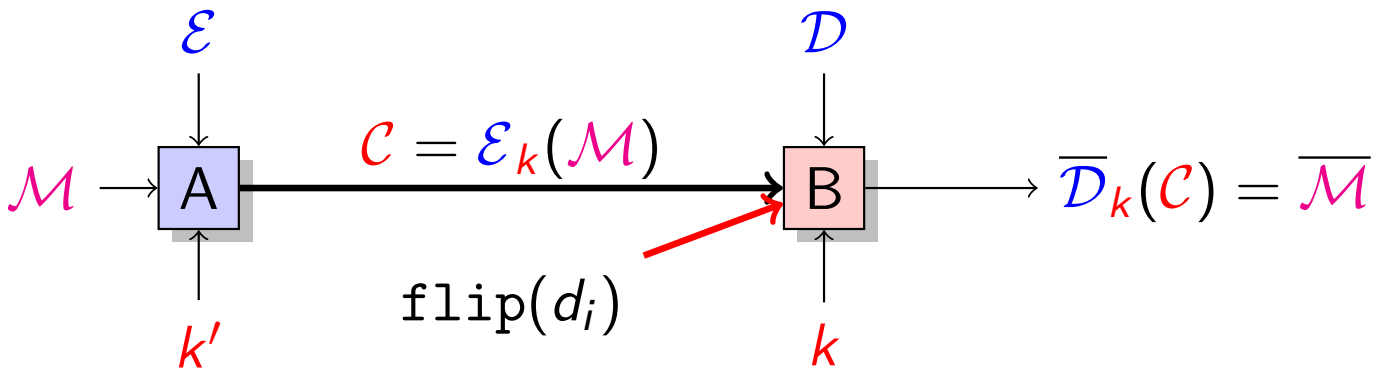

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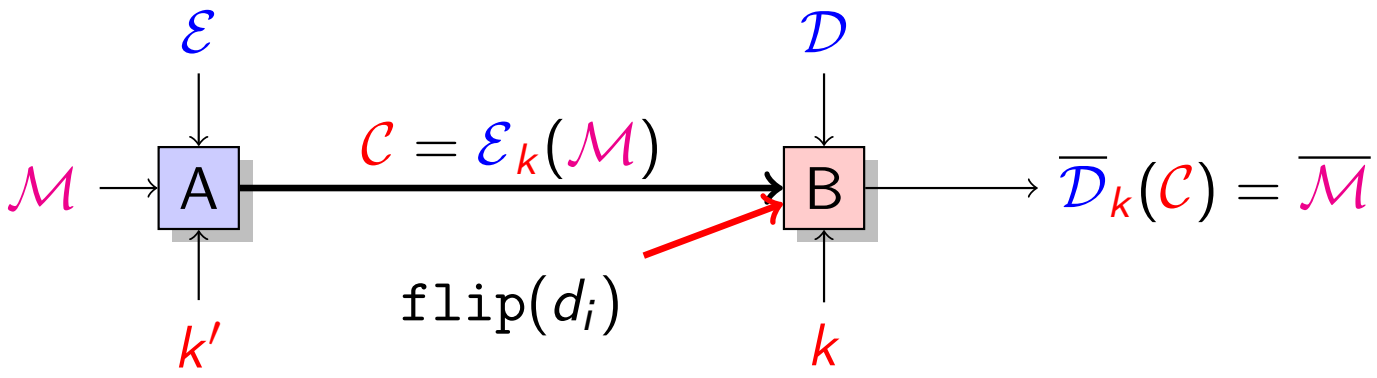

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- retry for several i ($\Longrightarrow$ get small parts of d, then mathematical attacks)

Many other fault attacks. . .

Countermeasures

Principles for preventing attacks:

- embed additional protection blocks
- modify the original circuit into a secured version
- application levels: circuit, architecture, algorithm, protocol...

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Countermeasures:

- electrical shielding
- detectors, estimators, decoupling
- use uniform computation durations and power consumption
- use detection/correction codes (for fault injection attacks)
- provide a random behavior (algorithms, representation, operations...)
- add noise (e.g. masking, useless instructions/computations)
- circuit reconfiguration (algorithms, block location, representation of values...)

Low-Level Coding and Circuit Activity

Assumptions:

- b is a bit (i.e. $b \in \{0, 1\}$, logical or mathematical value)
- electrical states for a wire ▬ : V_{DD} (logical 1) or GND (logical 0)

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Low-level codings of a bit:

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standard	GND	V_{DD}
dual rail	$r_0 = V_{\mathrm{DD}}$, $r_1 = \mathrm{GND}$ $(1, 0)_{\mathrm{DR}}$	$r_0 = \mathrm{GND}$, $r_1 = V_{\mathrm{DD}}$ $(0, 1)_{\mathrm{DR}}$

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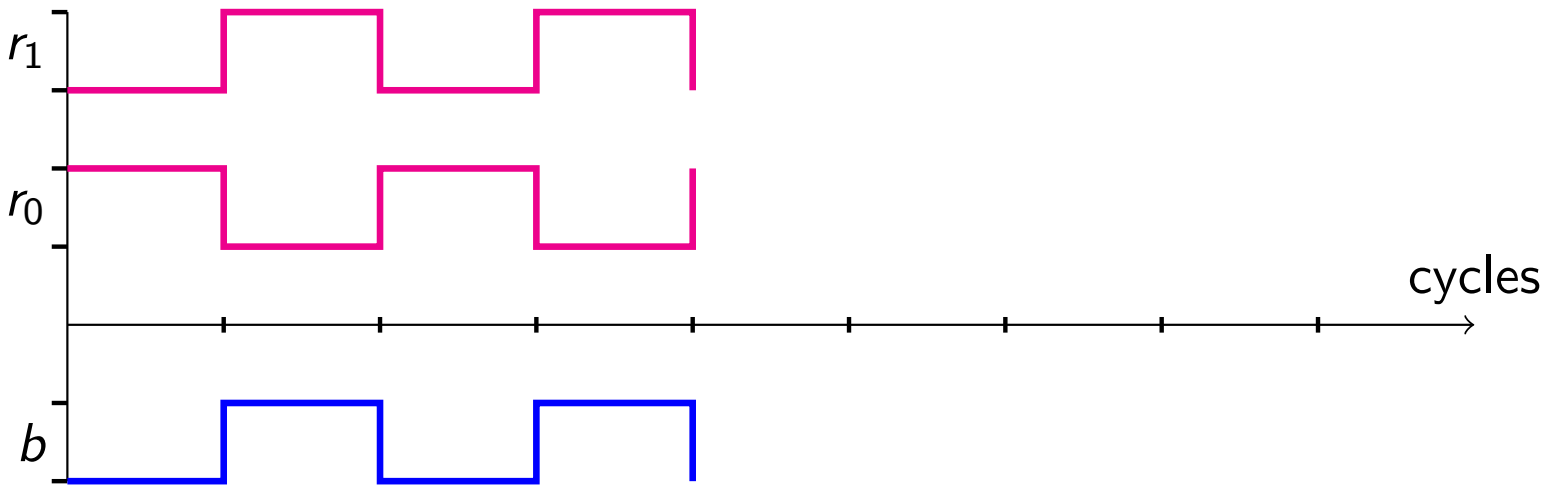

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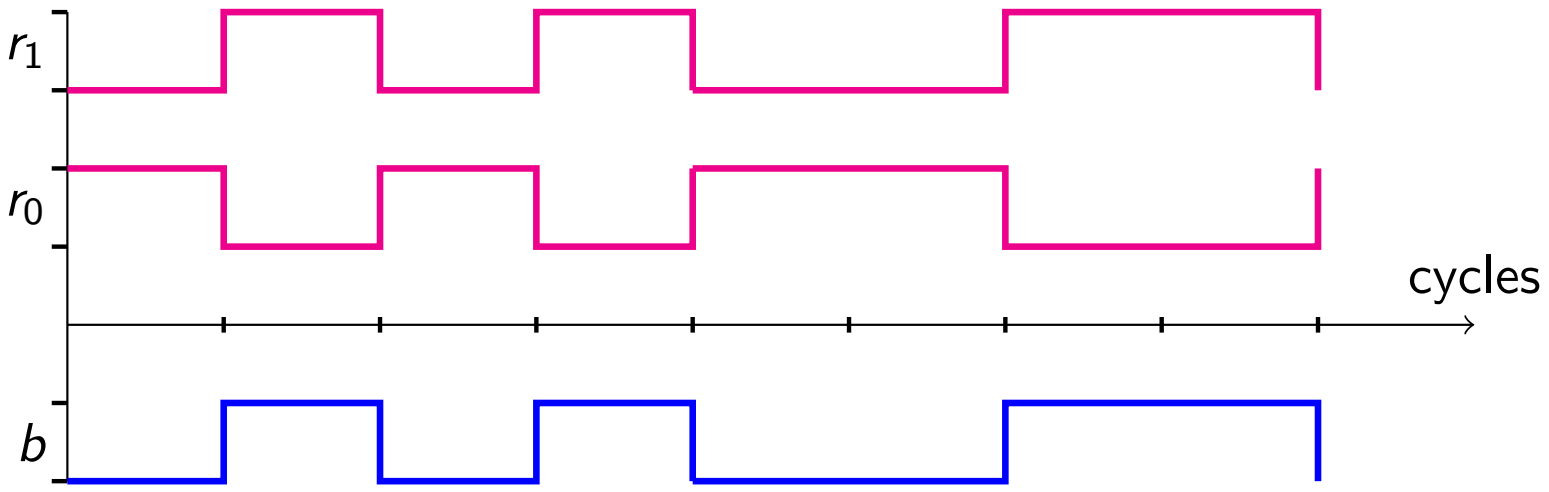

Circuit Logic Styles

Countermeasure principles: uniformize circuit activity and exclusive coding

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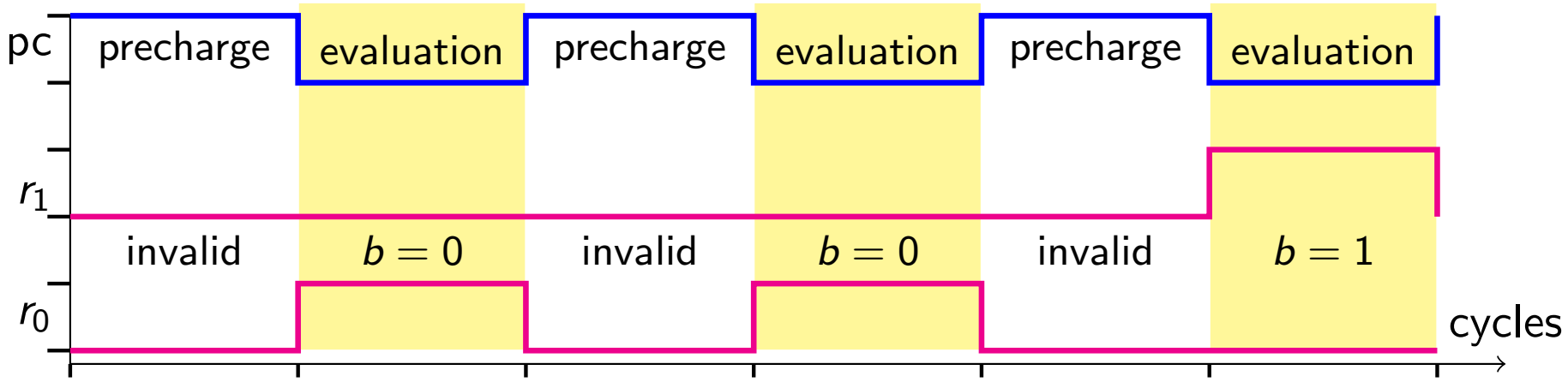
Solution based on precharge logic and dual-rail coding:



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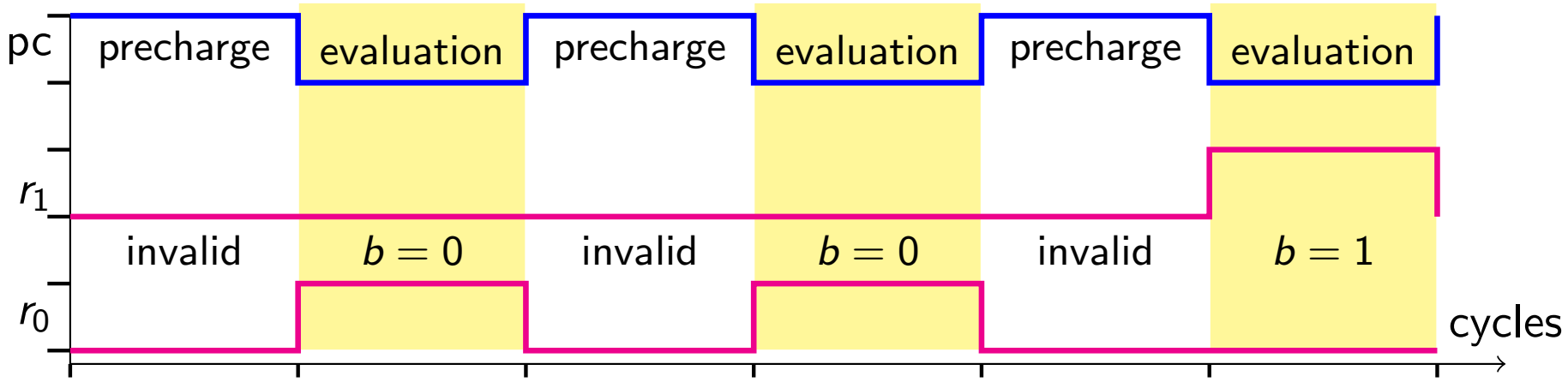
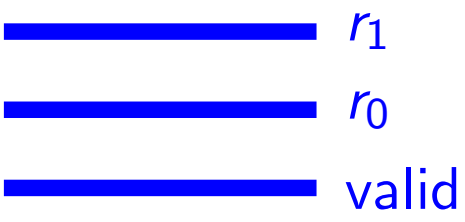
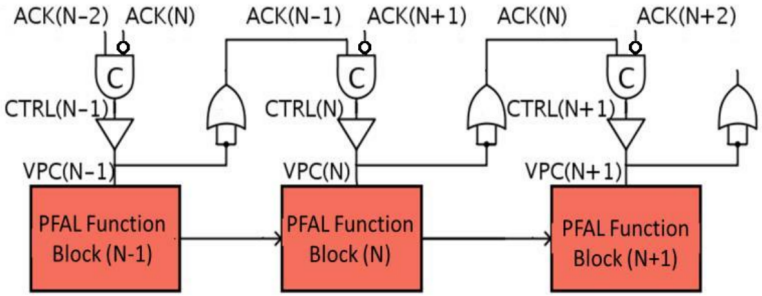


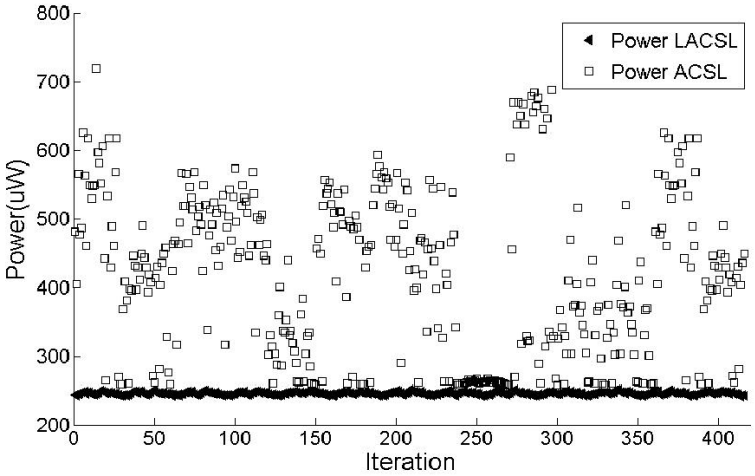
Solution based on validity line and dual-rail coding:

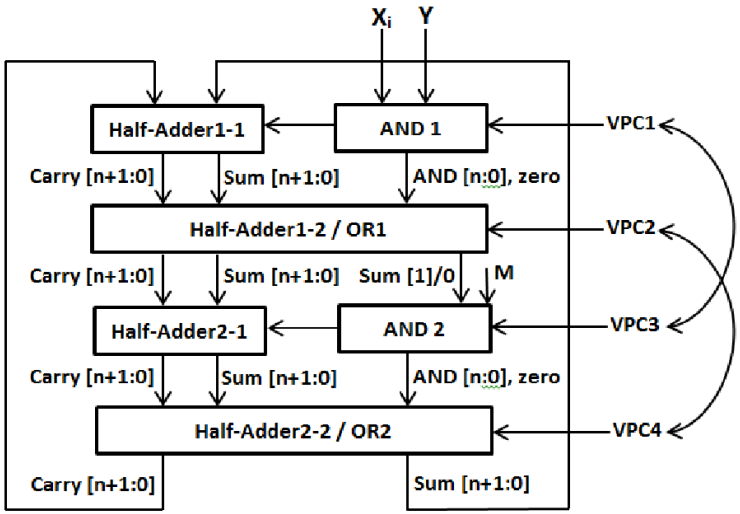


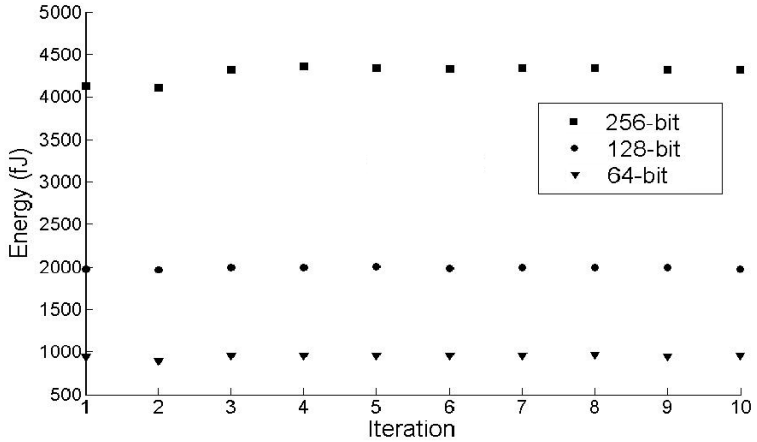
Important overhead: silicon area and local storage (registers)

Circuit-Level Protections for Arithmetic Operators







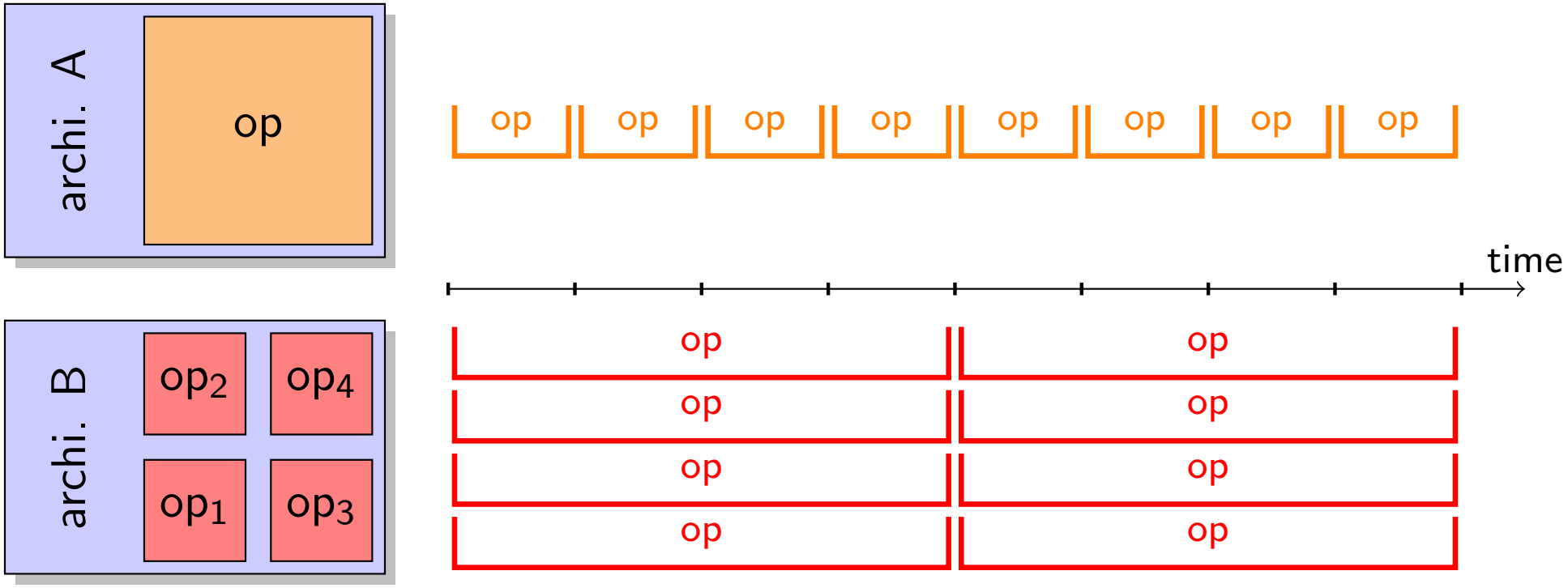


References: [8] and [9]

Countermeasure: Architecture

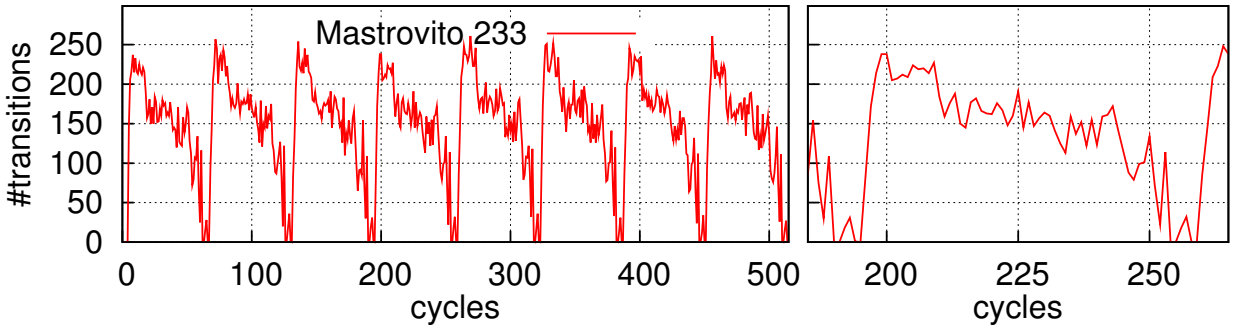
Increase internal parallelism:

- replace one fast but big operator
- by several instances of a small but slow one



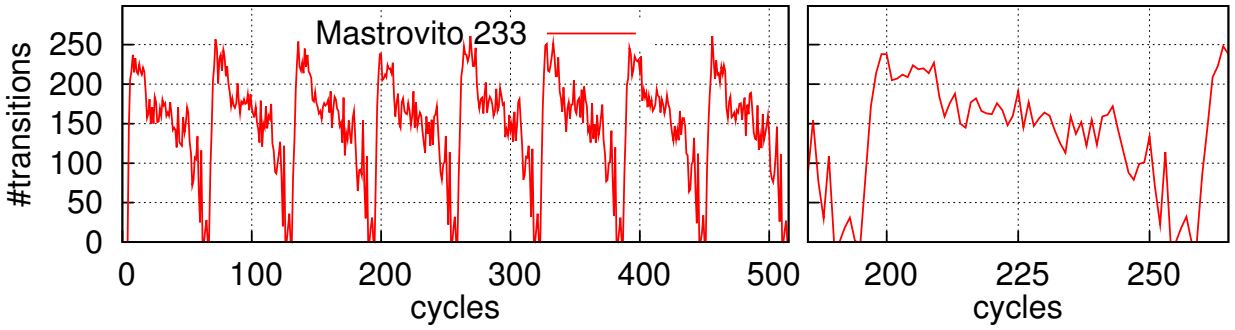
Protected Multipliers

Unprotected



Protected Multipliers

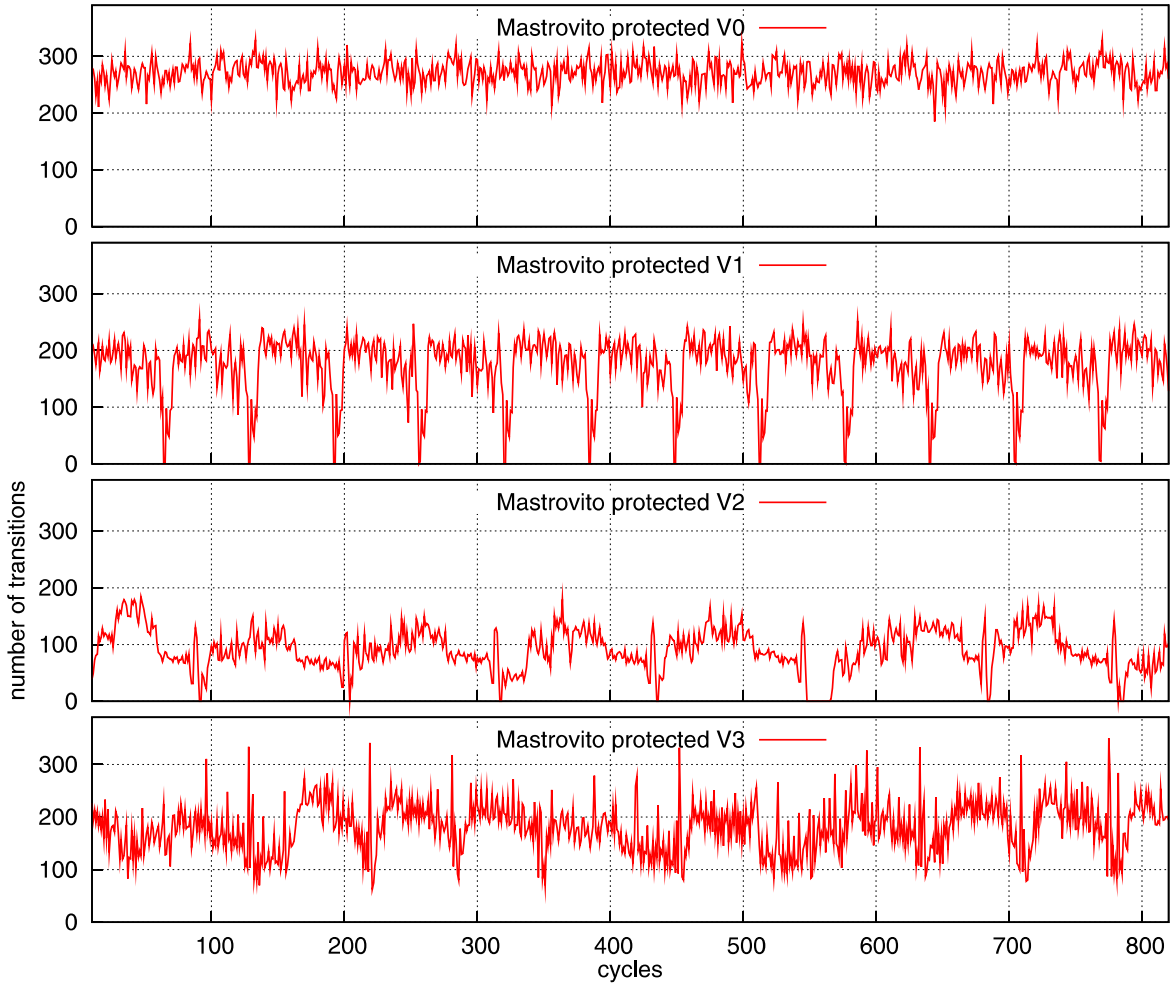
Unprotected



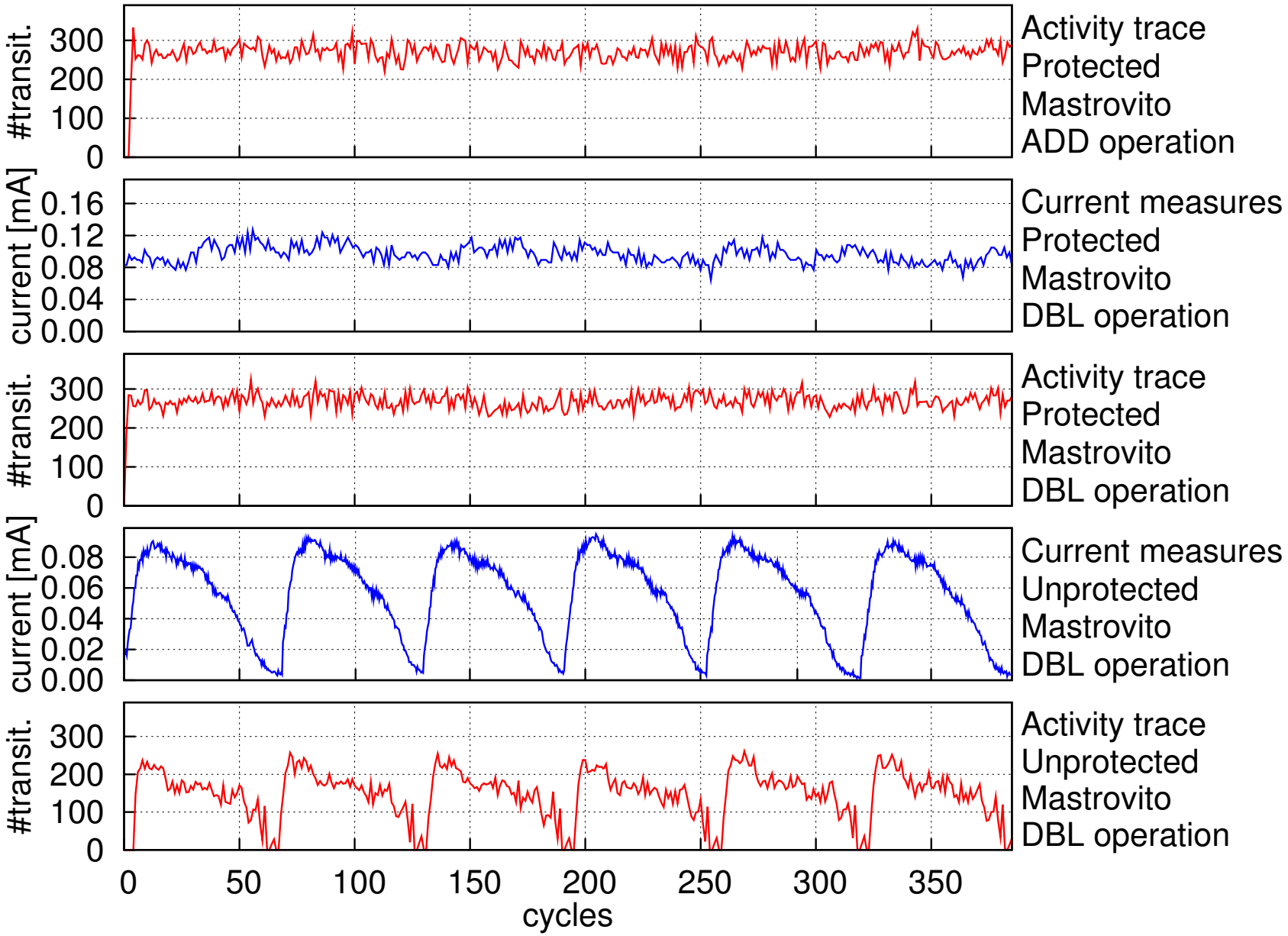
Protected

Overhead:
Area/time $< 10\,\%$

References:
PhD D. Pamula [13]
Articles: [16], [15], [14]



Protected ECC Accelerator

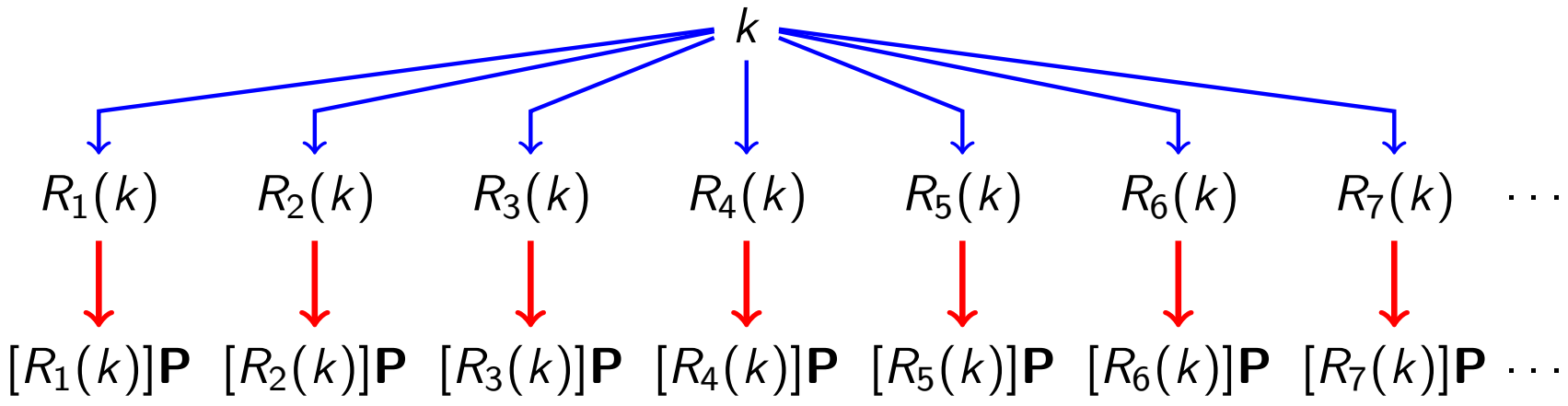


Warning: old dedicated accelerator (similar behavior is expected for our new one)

Arithmetic Level Countermeasures

Redundant number system =

- a way to improve the performance of some operations
- a way to represent a value with different representations



Important property: $\forall i \quad [R_i(k)]\mathbf{P} = [k]\mathbf{P}$

Proposed solution: use random redundant representations of k

Double-Base Number System

Standard radix-2 representation:

$$k = \sum_{i=0}^{t-1} k_i 2^i = \boxed{k_{t-1}}\boxed{k_{t-2}}\boxed{\cdots}\boxed{k_2}\boxed{k_1}\boxed{k_0} \quad t \text{ explicit digits}$$

Double-Base Number System

Standard radix-2 representation:

$$k = \sum_{i=0}^{t-1} k_i 2^i =$$

2^{t-1}	2^{t-2}	$\cdots$	2^2	2^1	2^0	implicit weights
k_{t-1}	k_{t-2}	$\cdots$	k_2	k_1	k_0	t explicit digits

Digits: $k_i \in \{0, 1\}$, typical size: $t \in \{160, \ldots, 600\}$

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Double-Base Number System (DBNS):

$$k = \sum_{j=0}^{n-1} k_j 2^{a_j} 3^{b_j} =$$

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Double-Base Number System (DBNS):

$$k = \sum_{j=0}^{n-1} k_j 2^{a_j} 3^{b_j} =$$

k_{n-1}	$\cdots$	k_1	k_0	n $(2,3)-$terms
a_{n-1}	$\cdots$	a_1	a_0	explicit "digits"
b_{n-1}	$\cdots$	b_1	b_0	explicit ranks

$a_j, b_j \in \mathbb{N}$, $k_j \in \{1\}$ or $k_j \in \{-1, 1\}$, size $n \approx \log t$

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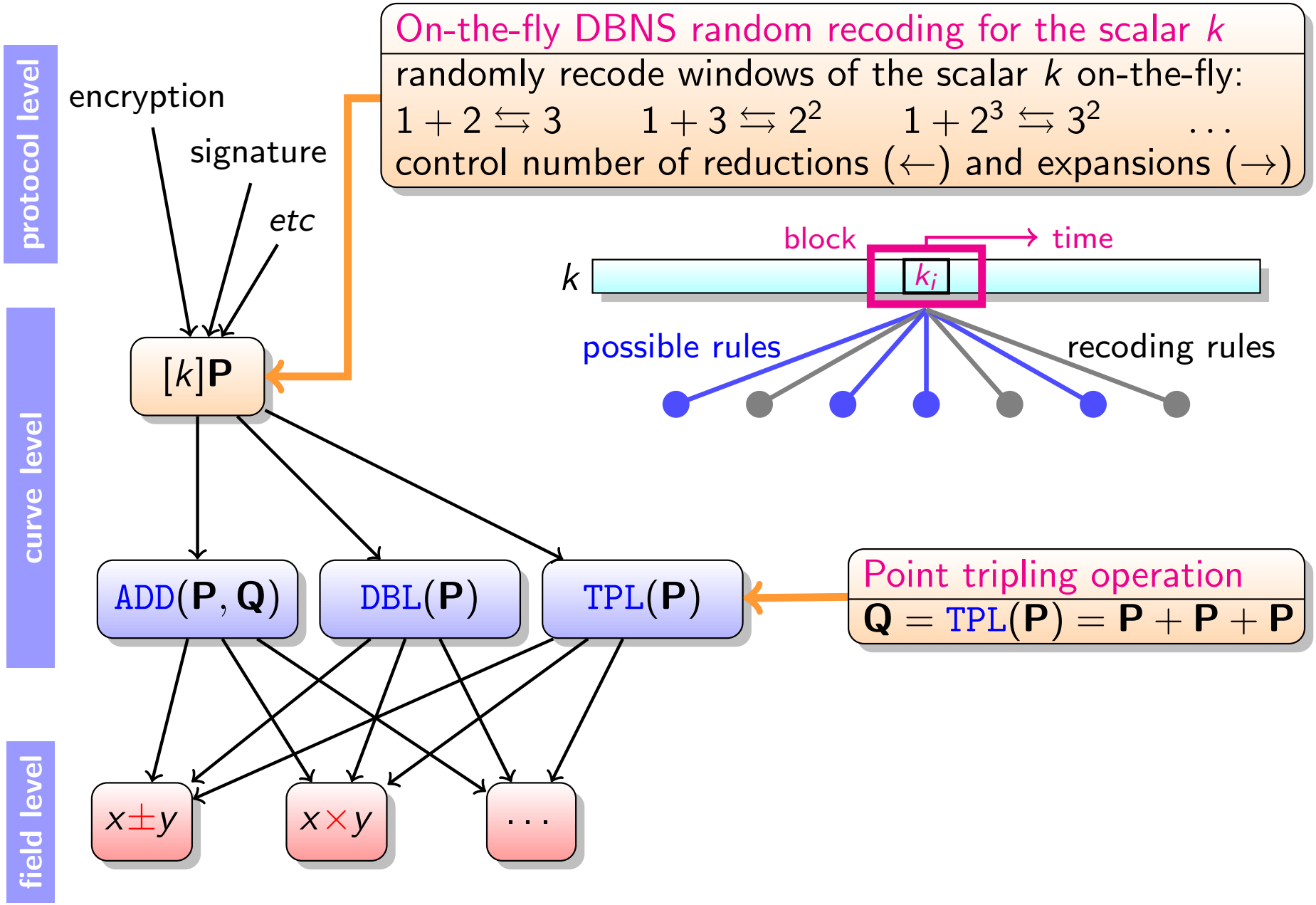
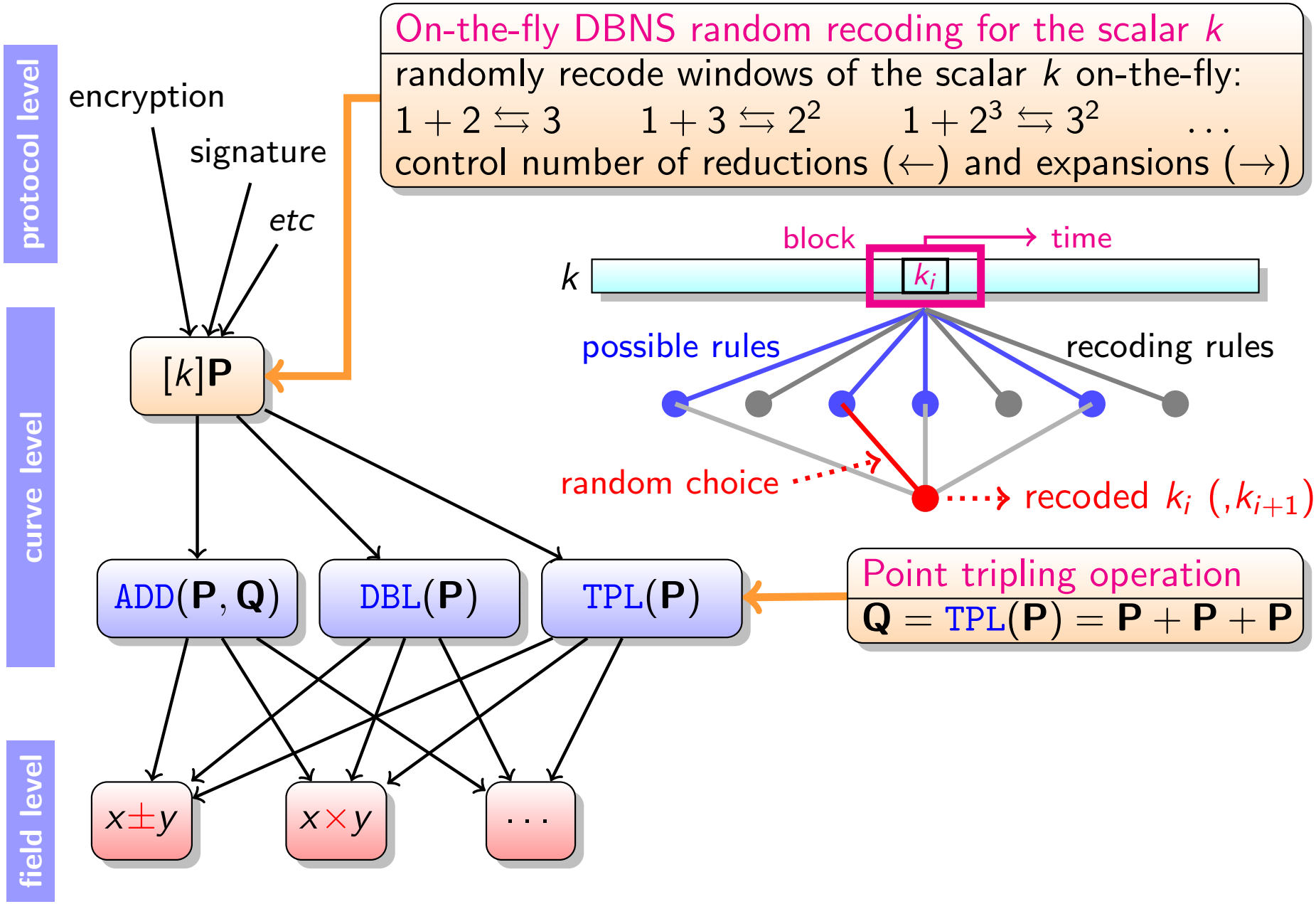
DBNS is a very redundant and sparse representation: $1701 = (11010100101)_2$

$$\begin{aligned}
1701 &= 243 + 1458 &= 2^0 3^5 + 2^1 3^6 &= (1, 0, 5), (1, 1, 6) \\
&= 1728 - 27 &= 2^6 3^3 - 2^0 3^3 &= (1, 6, 3), (-1, 0, 3) \\
&= 729 + 972 &= 2^0 3^6 + 2^2 3^5 &= (1, 0, 6), (1, 2, 5) \\
&\ldots
\end{aligned}$$

Randomized DBNS Recoding of the Scalar k



Randomized DBNS Recoding of the Scalar k



Randomized DBNS Recoding of the Scalar k

protocol level

encryption

signature

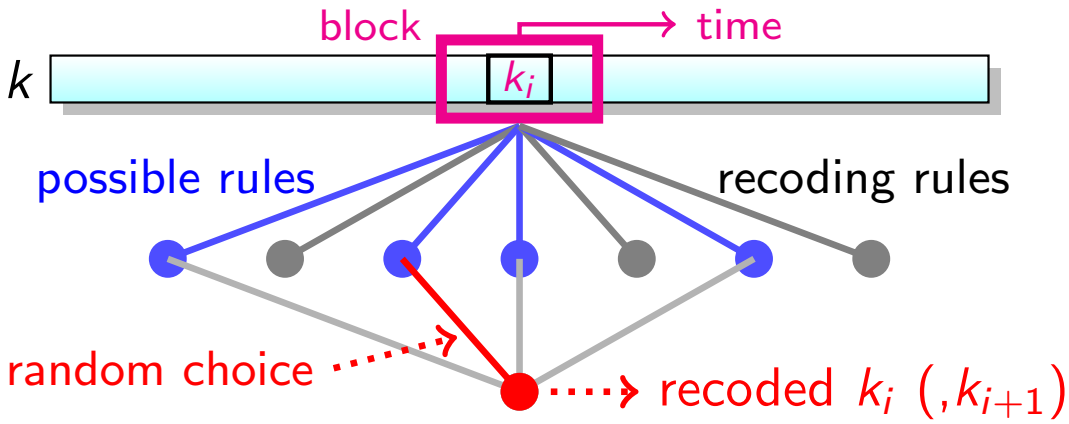
etc

On-the-fly DBNS random recoding for the scalar k

randomly recode windows of the scalar k on-the-fly:

$1+2 \leftrightarrows 3 \qquad 1+3 \leftrightarrows 2^2 \qquad 1+2^3 \leftrightarrows 3^2 \qquad \ldots$

control number of reductions ($\leftarrow$) and expansions ($\rightarrow$)



curve level

$[k]\mathbf{P}$

$\mathtt{ADD}(\mathbf{P},\mathbf{Q})$ $\mathtt{DBL}(\mathbf{P})$ $\mathtt{TPL}(\mathbf{P})$

Point tripling operation

$\mathbf{Q} = \mathtt{TPL}(\mathbf{P}) = \mathbf{P}+\mathbf{P}+\mathbf{P}$

field level

$x \pm y$ $x \times y$ $\ldots$

DBNS is redundant $\Rightarrow$ security $\nearrow$

DBNS is sparse $\Rightarrow$ 20–30 % speed $\nearrow$

Ref: [7] Chabrier, Pamula & Tisserand. Asilomar 2009

Hardware Implementation of RNS for ECC (1/2)

RNS: Residue Number System

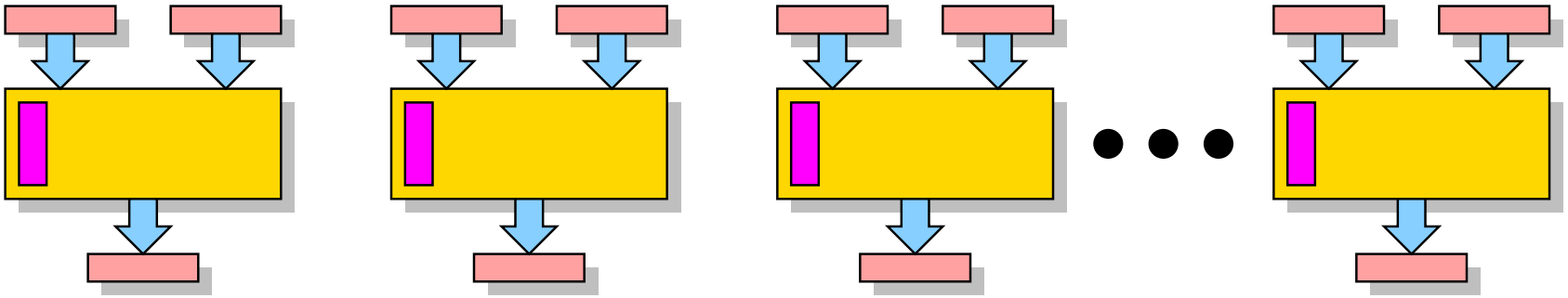
- Base $\mathcal{B} = (m_1, m_2, \ldots, m_k)$ of k relatively prime moduli
- Size of the base: k

$$A = \{a_1, a_2, \ldots, a_k\}, \quad \forall i \ a_i = A \bmod m_i$$

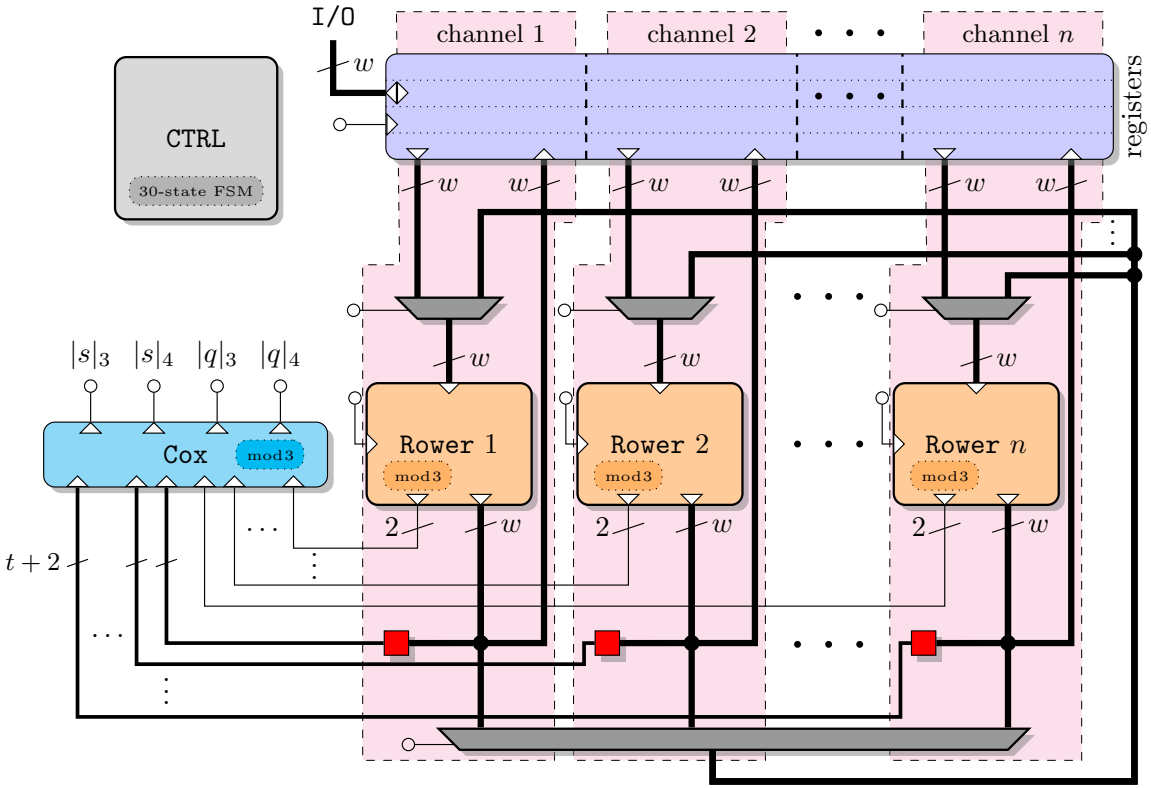
Operations:

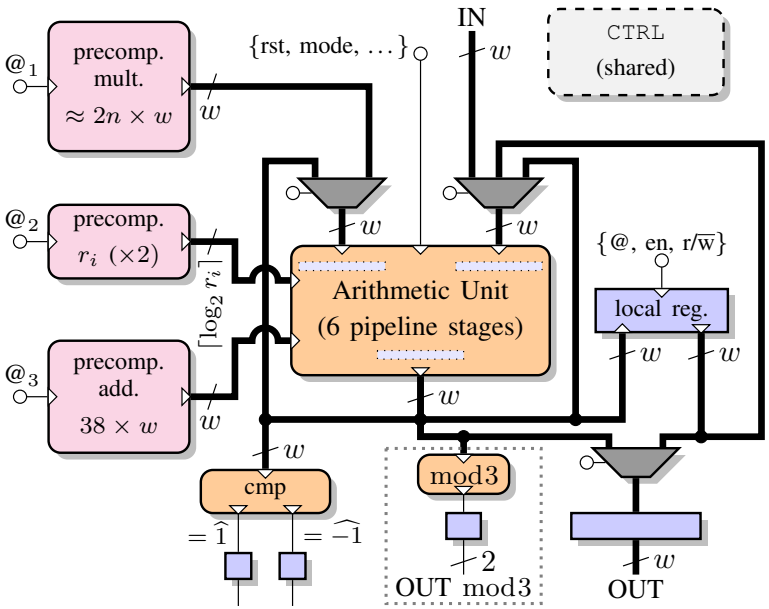
$$A \pm B = (|a_1 \pm b_1|_{m_1}, \ldots, |a_k \pm b_k|_{m_k})$$

$$A \times B = (|a_1 \times b_1|_{m_1}, \ldots, |a_k \times b_k|_{m_k})$$



Hardware Implementation of RNS for ECC (2/2)

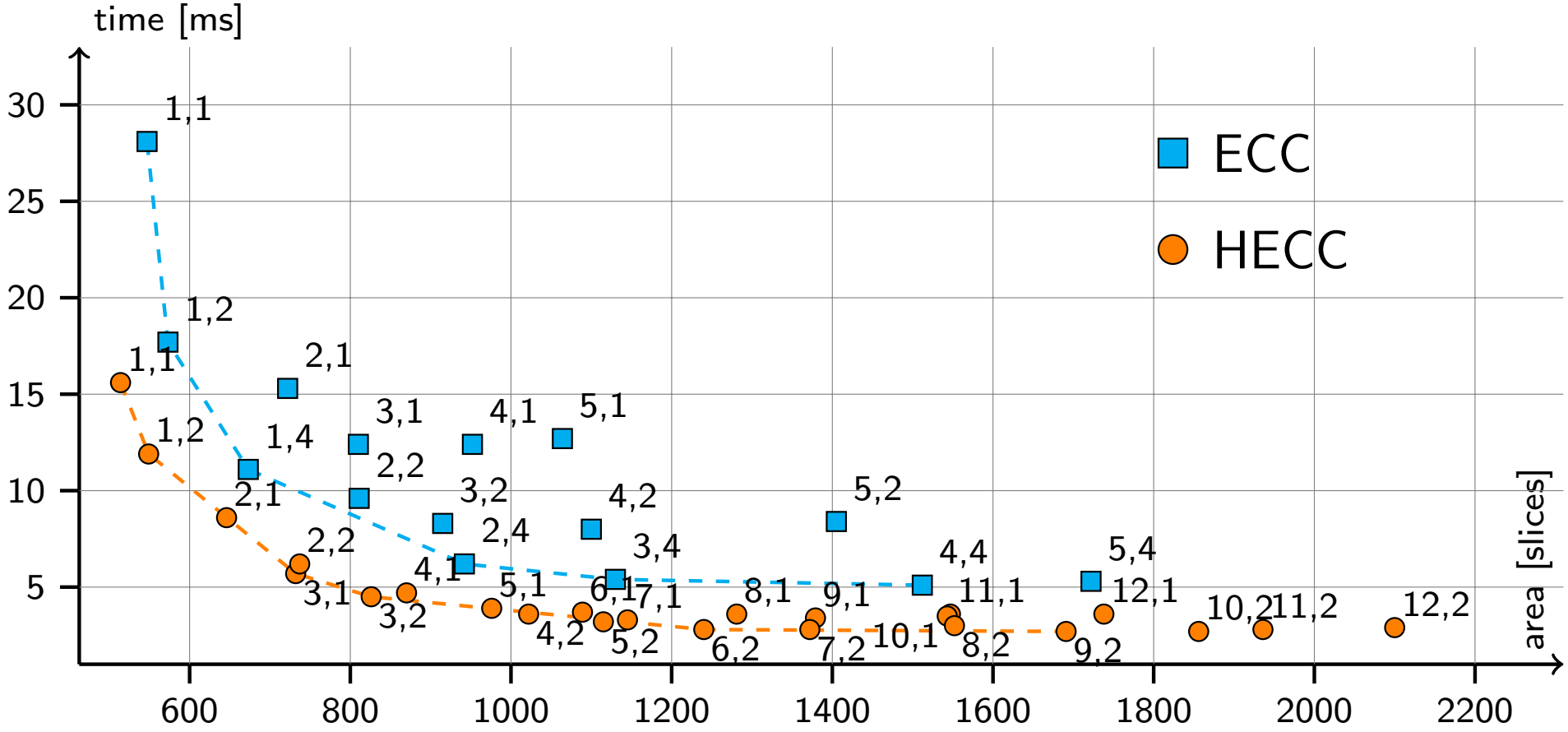




Optimized algorithms and implementations for $\mathrm{GF}(p)$ operations:

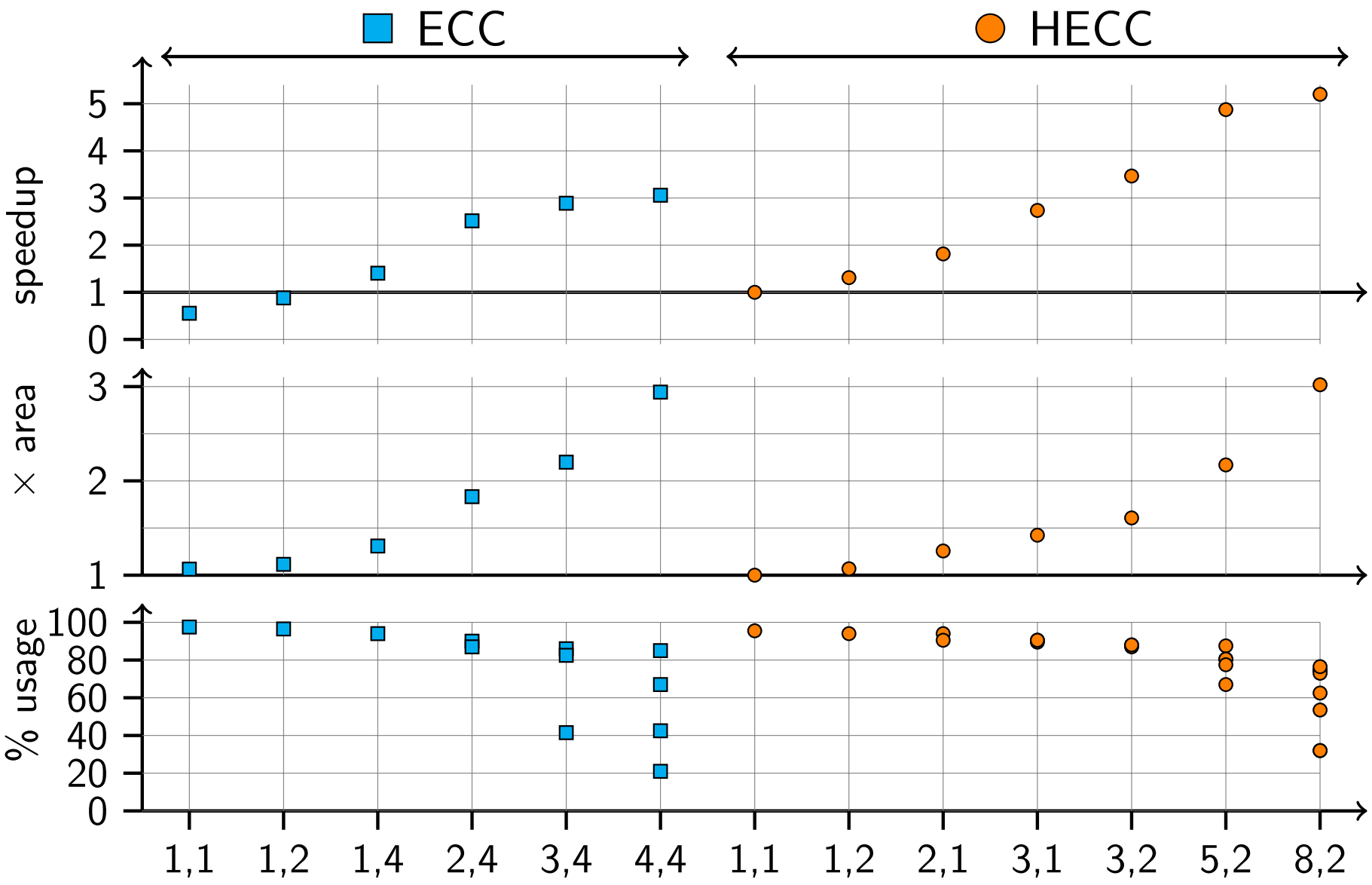
- fast operations: inversion [3], modular multiplication [5], patterns [4]
- PhD Thesis Karim Bigou [2]
- hybrid positio-residues (HPR) representation [6]

Comparison ECC 256 vs HECC 128 (1/2)



On average HECC is 40 % faster than ECC for a similar silicon cost

Comparison ECC 256 vs HECC 128 (2/2)



Conclusion

- Side channel and fault attacks are serious threats
- Attacks are more and more efficient (many variants)
- Security analysis is mandatory at all levels (specification, algorithm, operation, implementation)
- Security = trade-off between performances, robustness and cost
- Security = *func*(secret value, attacker capabilities)
- security = computer science + microelectronics + mathematics

Conclusion

- Side channel and fault attacks are serious threats
- Attacks are more and more efficient (many variants)
- Security analysis is mandatory at all levels (specification, algorithm, operation, implementation)
- Security = trade-off between performances, robustness and cost
- Security = *func*(secret value, attacker capabilities)
- security = computer science + microelectronics + mathematics

Current works examples:

- Methods/tools for automating security analysis
- Circuit reconfiguration (representations, algorithms)
- Circuits with reduced activity variations
- Representation of numbers with error detection/correction "codes"
- Design space exploration
- CAD tools with security improvement capabilities

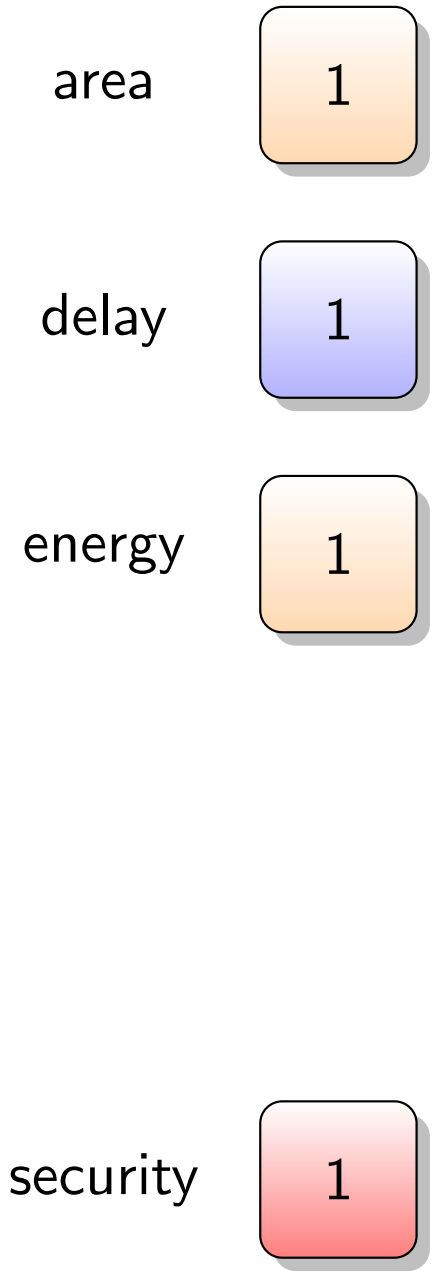
Our Long Term Objectives

Study the links between:

- cryptosystems
- arithmetic algorithms
- $\mathbb{F}_q$, pts representations
- architectures & units
- circuit optimisations

to ensure

- high security against
  - theoretical attacks
  - physical attacks
- low design cost
- low silicon cost
- low energy(/power)
- high performances
- high flexibility



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area $1 \longrightarrow 1 + a$

delay $1 \longrightarrow 1 + t$

energy $1 \longrightarrow 1 + e$

$a, t, e \in 0\%, 5\%, 10\%, \ldots, 100\%$

security 1

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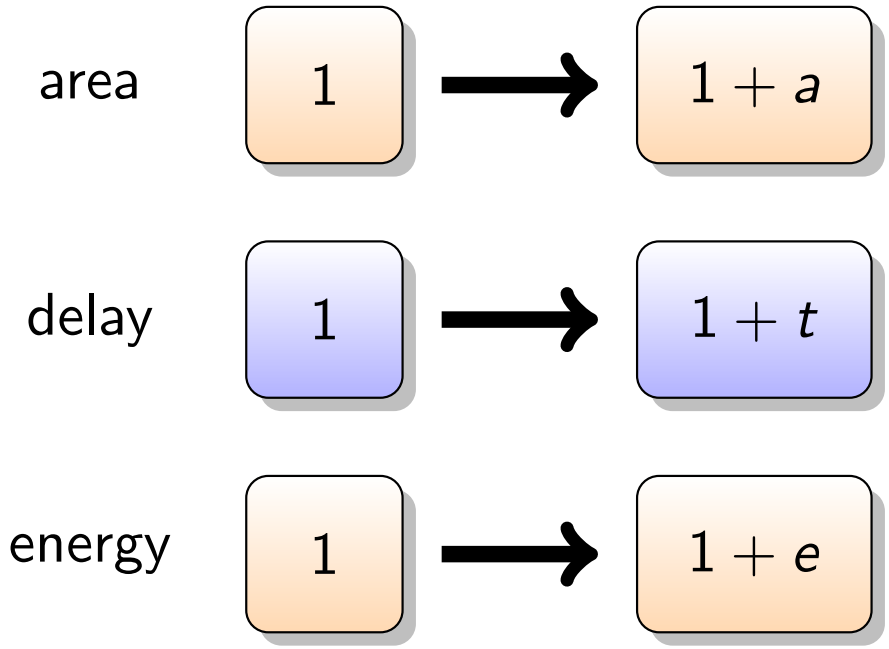
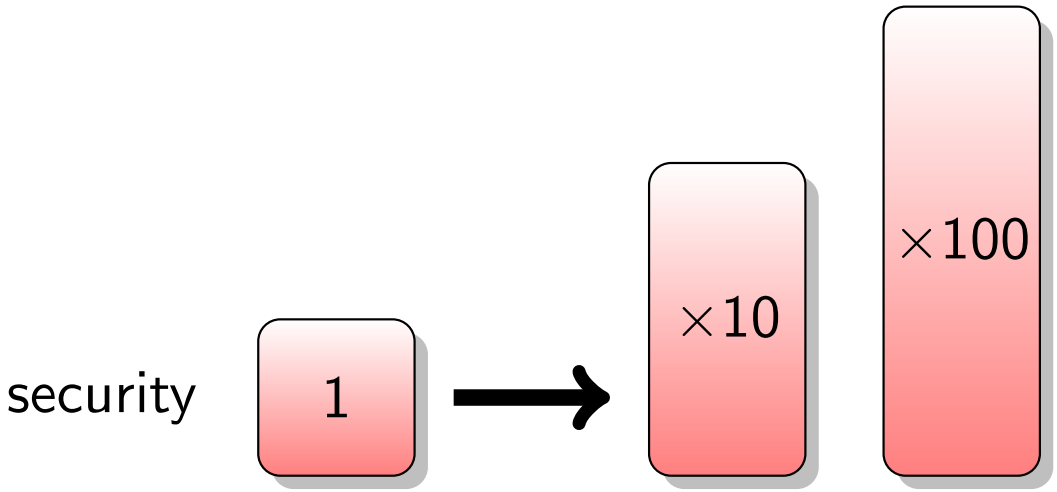


$a, t, e \in 0\%, 5\%, 10\%, \ldots, 100\%$



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The end, questions ?

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Thank you