Design and Simulation of Nano Wire FET

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DOI **10.2412/mmse.97.91.539** provided by Seo4U.link

Keywords: nanowire, FET, threshold voltage, SILVACO.

ABSTRACT. As the era of classical planar metal-oxide-semiconductor field-effect transistors (MOSFETs) comes to an end, the semiconductor industry is beginning to adopt 3D device architectures, such as FETs, starting at the 22 nm technology node. Since physical limits such as short channel effect (SCE) and self-heating may dominate, it may be difficult to scale Si FinFET below 10 nm. In this regard, transistors with different materials, geometries, or operating principles may help. For example, gate has excellent electrostatic control over 2D thin film channel with planar geometry and 1D nanowire (NW) channel with gate-all-around (GAA) geometry to reduce SCE. High carrier mobility of single wall carbon nanotube (SWNT) or III-V channels may reduce VDD to reduce power consumption. Therefore, as channel of transistor, 2D thin film of array SWNTs and 1D III-V multi NWs are promising for sub 10 nm technology nodes. To simulate these devices, accurate modelling and design based on gate-material are necessary to assess their performance limits, since cross-sections of the multi-gate NWFETs are expected to be a few nano-meters wide in their ultimate scaling. In this paper we have explored the use of SILVACO with different materials for simulating and studying the short channel behaviour of nanowire FETs.

Introduction. CMOS Technology is facing many problems over the last 30 years .In conventional MOSFET we have certain electrostatic limitations like source to drain tunnelling, carrier mobility, static leakages etc. [1-5]. As the size of nanomaterials is very small we can use a more number of transistors on a single chip so that size of the chip is reduced its additional features are robust against short channel effects and relatively simple steps of fabrication so device and circuit developers are using this type of devices and also can use different types of materials used to make these type of materials at low cost [2]. For an Ultra-small MOSFET we have to face several problems like electrostatic limits, source-to-drain tunneling, carrier mobility degradation, process variations and static leakage etc., all these problems can damage the MOSFET by reducing its performance [1-5].

In the VLSI industry it is critically necessary to have a device which has low power dissipation and has high performance along with long time durability. In order to achieve such characteristic features in a real time operation scenario it will be a hard tenacious task. The trend toward ultra-short gate length MOSFETs requires a more and more effective control of the channel by the gate leading to new device architecture [4]. It appears that non-classical device architectures can extend the CMOS lifetime and provide solutions to continue scaling. More in the present modern world the electronic device must have low response time along with low power consumption provided the cost of the device must be in a nominal range.

Using a conventional MOSFET device can no longer sustain such a modern day challenge. So if we use Nano-Materials we can meet the modern day challenge [3].

In this paper, we had replaced the Poly-Silicon material present on the Gate Terminal of the MOSFET device with different Nano-Materials like Si (Silicon Nano-Wires), ZnO (Zinc Oxide Nano-Wires), CSi (Carbon-Silicon or Silicon Carbide NanoWires).

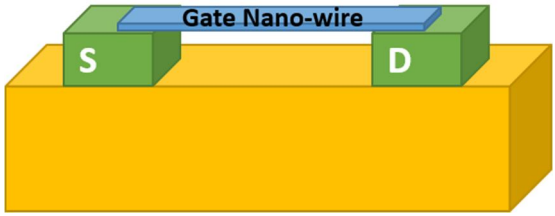

Fig. 1. Schematic of Nano Wire FET.

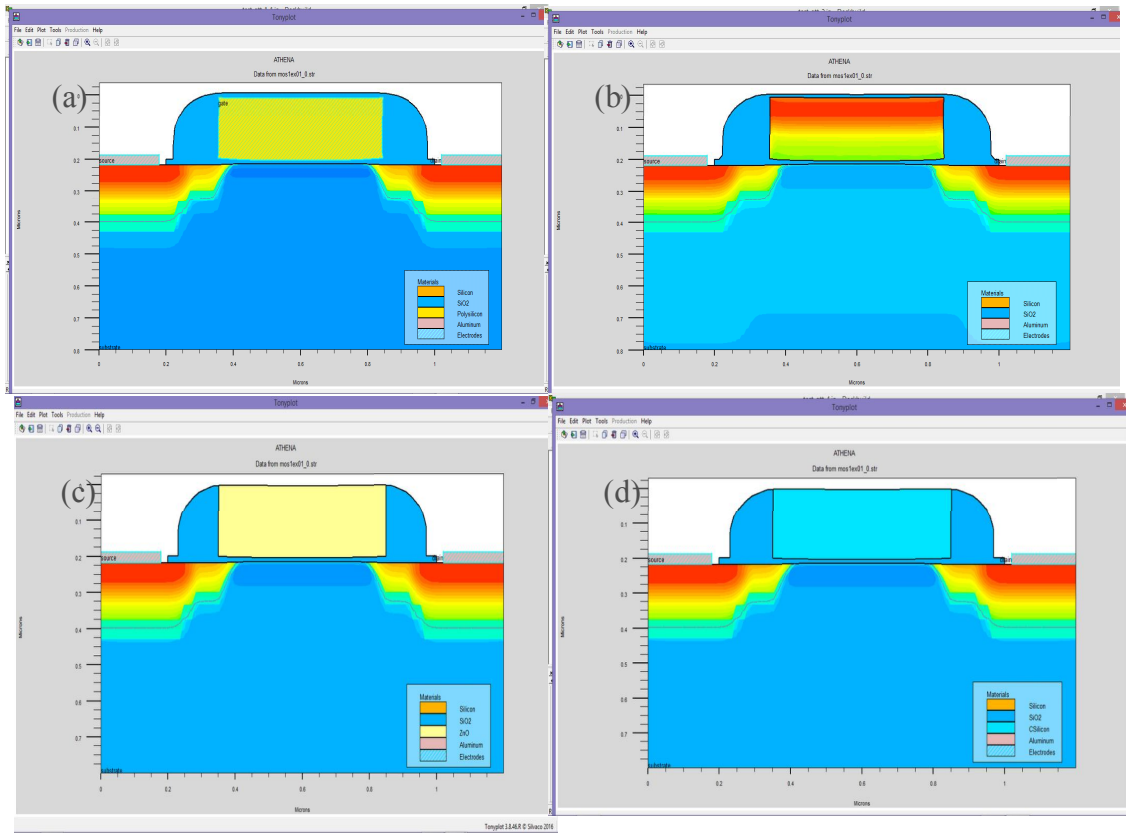

Fig. 2. Schematic of different Nano Wire MOSFETs: a) PolySilicon; b) Silicon Nano Wire; c) Zinc Oxide Nano Wire; d) Carbon Silicon materials in Silvaco Software.

Equations

Saturation region drain current:

$$I_d = (\mu c_{ox}\, \omega)/(2L)\,(V_{gs}-V_t)^2\,(1-V_{ds}/V_A)\ ;\ V_{ds} >= V_{gs}-V_t$$

Ohmic region drain current:

$$I_d = (\mu c_{ox}\omega)/(2L)[2\,(V_{gs}-V_t)V_{ds} - V_{ds}^2]\,(1-V_{ds}/V_A)\ ;\ V_{ds} < V_{gs}-V_t$$

Oxide capacitance:

$$c_{ox} > €_{ox}/t_{ox}$$

Transconductance:

$$g_m > (\mu c_{ox}\, \omega/L)\ (V_{gs}-V_t)$$

Output resistance:

$$R_o = |V_A|/I_{do}$$

Input capacitance:

$$C_{in} > C_{gs}+C_{gd} = C_{ox} L\omega$$

Transition frequency:

$$F_c > g_{m/}\ (2\ pi\ C_{in})$$

Surface mobility holes:

$$\mu > 200 cm^2/V\text{-}s$$

Surface mobility electrons:

$$\mu > 450 cm^2/V\text{-}s$$

Nomenclature:

drain current – I_d; oxide capacitance – c_{ox}; transconductance – g_m; output resistance – R_o; input capacitance – C_{in}; transition frequency – F_c; electronic field strength in oxide – $€_{ox}$; gate to source voltage – V_{gs}; drain to source voltage – V_{ds}; thickness of oxide layer – t_{ox}; threshold voltage – V_t.

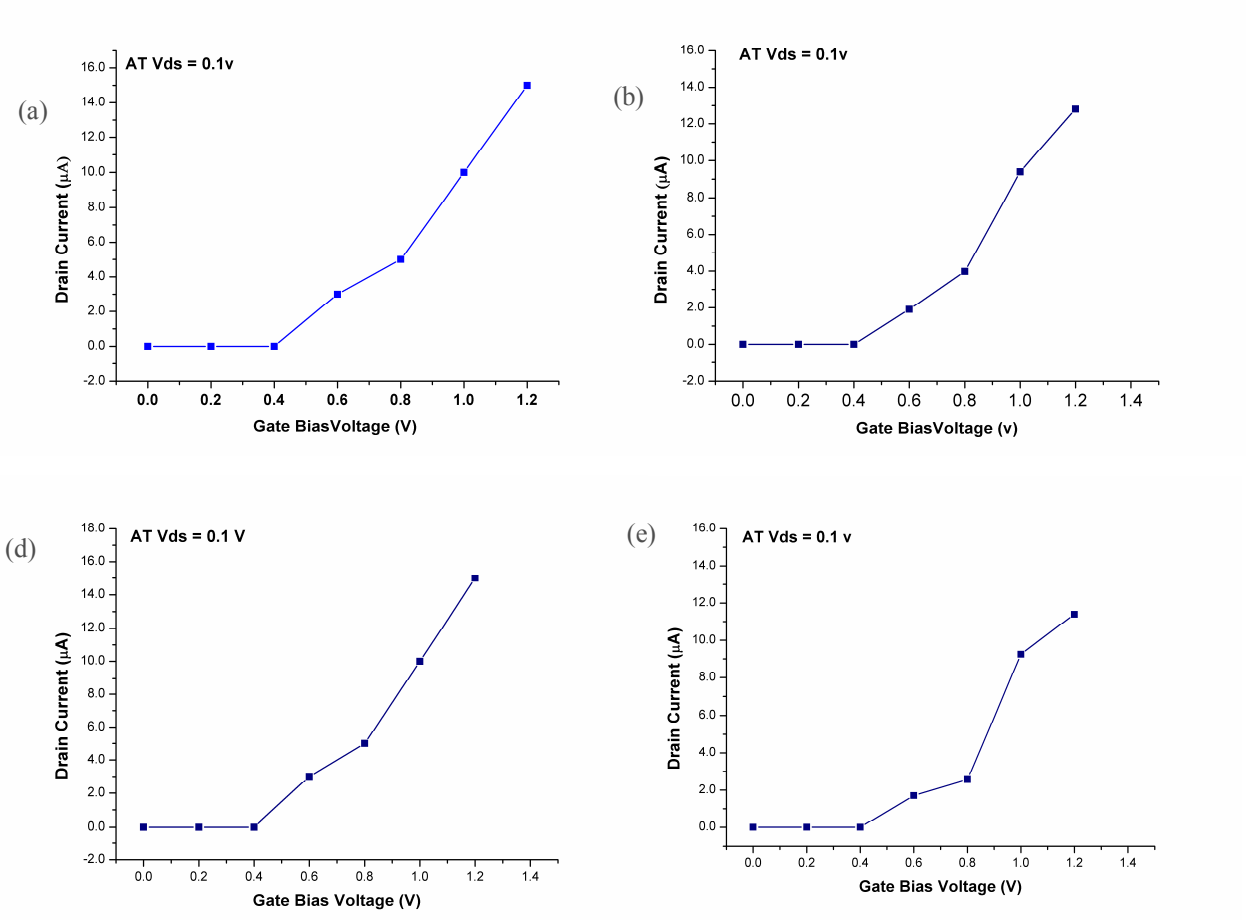

Fig. 3. I_{gs} vs V_{ds} sub threshold values for: a) PolySilicon ; b) Silicon Nano Wire ; c) Zinc Oxide Nano Wire ; d) Carbon Silicon Nano- Wire material FET in Silvaco Software.

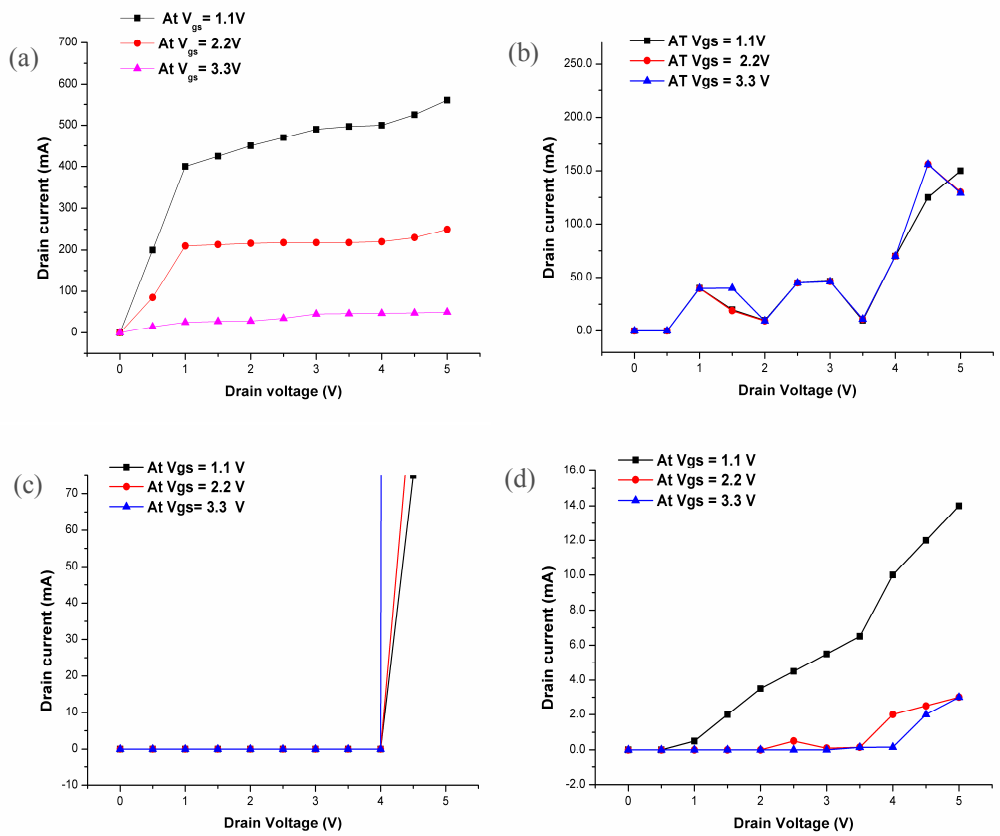

Fig. 4. Id_s vs V_{ds} Drain Current Values for : a)PolySilicon ; b) Silicon Nano Wire ; c) Zinc Oxide Nano Wire ; d) Carbon Silicon Nano- Wire FET in Silvaco Software.

Table 1. I_{gs} vs V_{ds} sub threshold values.

S.No	Nano-Wire Material (N.W.M.) NAME	THRESHOLD VOLTAGE (Volts)	RESPECTIVE CURRENT VALUE (Amperes)
1	Poly silicon	0.75	$3.989 \cdot 10^{-6}$
2	Silicon N.W.M.	0.749	$3.923 \cdot 10^{-6}$
3	Zinc-Oxide N.W.M.	0.743	$4.31 \cdot 10^{-6}$
4	Carbon silicon N.W.M.	0.75	$3.973 \cdot 10^{-6}$

Table 2. I_{ds} vs V_{ds} curve values.

Material Name	Respective Drain Current Value I_{ds} (Amperes) when V_{ds} (Volts)		
	At 1.1 V	At 2.2V	At 3.3V
Poly Silicon	$4.24 \cdot 10^{-4}$	$2.45 \cdot 10^{-4}$	$5.38 \cdot 10^{-5}$
Silicon Nano Wire	$3.62 \cdot 10^{-15}$	$3.35 \cdot 10^{-15}$	$3.02 \cdot 10^{-15}$
Zinc Oxide Nano Wire	$4.25 \cdot 10^{-15}$	$4.14 \cdot 10^{-15}$	$5.39 \cdot 10^{-15}$
Carbon Silicon Nano Wire	Respective Drain Current Value I_{ds} (Amperes) when V_{ds} (Volts)		
	At 3 V	At 3.5 V	At 4 V
	$2.28 \cdot 10^{-4}$	$8.73 \cdot 10^{-5}$	$5.44 \cdot 10^{-7}$

Summary. From I_{gs} vs V_{ds} sub threshold values I_{ds} vs V_{ds} curve values we can observe that the FET designed using the Nano-wire Materials has less drain current, drain voltage, low sub-threshold voltage. From this we can conclude that the drawbacks of the normal conventional FET has been covered upto certain level using the FET designed from using the Nano-Wire Materials.

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Cite the paper

M. Anil Kumar, Y.N.S. Sai Kiran, U. Jagadeesh, M. Durga Prakash (2017). Design and Simulation of Nano Wire FET. *Mechanics, Materials Science & Engineering,* Vol 9. doi:10.2412/mmse.97.91.539