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Hardware Implementation of Metric Algorithms for a Self-Mixing Laser Interferometric Sensor

Saqib Amin, Usman Zabit, Tassadaq Hussain, Olivier D. Bernal

Abstract—Self-mixing interferometry (SMI) has been widely used for sensing of diverse vibration, velocity, displacement, biomedical and flow applications. The simplicity of the SMI configuration enables the design of a low-cost, self-aligned and compact sensor with a small optical component count. SMI occurs when a small portion of emitted coherent optical beam is backscattered by the remote target and re-enters the laser cavity, causing interference. Under SMI, the employed laser diode simultaneously acts as a laser source, coherent detector, as well as micro-interferometer. This simple sensor design configuration, however, comes at a price of complex signal processing algorithms, because the SMI signals have rich characteristics as a function of optical feedback level. The purpose of this research work is to implement two of these algorithms, time-frequency signal processing (TFSP) and Consecutive samples based Unwrapping (CSU) in hardware so that real-time displacement and vibration measurements with nanometric precision can be retrieved from the SM sensor in an embedded, autonomous manner. We implemented and tested both algorithms on a Xilinx ZYNQ 7000 development board using VHDL. Results show that our design of CSU algorithm is capable of operating at 432 MHz minimum clock frequency and latency of 3 clock cycles. Our CSU design consumes 159 slice registers and 215 LUT's, and draws 0.70 watts of onboard power. While the design of TFSP algorithm is capable of operating at 363.3 MHz clock frequency and latency of 570k clock cycles. TFSP design consumes 5056 slice registers and 5192 LUT's, and draws 0.8 watts of onboard power.

Keywords—Self-mixing; interferometry; real-time; vibration measurement; signal processing

I. INTRODUCTION

Optical feedback (OF) interferometry [1] or Self-mixing (SM) interferometry [2] has been widely studied and used in many diverse applications involving measurements of displacement [3], velocity [4], biomedical signals [5], embedded sensing [6], and fluid flow rates [7]. Due to a high resolution of SM techniques involving very inexpensive and simple experimental optical setup, these techniques are being increasingly used for practical applications [8], [9].

A typical SM interferometric displacement sensor is shown in Fig.1. SM phenomenon, based on laser feedback, occurs when part of the laser beam is reflected back from moving target and re-enters active cavity of the laser diode (LD). This re-entered laser beam is mixed with the emitted light, producing variations in optical output power (OOP) which can be easily picked up through the monitor photo-diode (PD) enclosed in LD package [1]. The shape of OOP strongly depends on optical feedback coupling factor C . $C \leq 1$ corresponds to weak feedback regime while $1 < C < 4.3$ corresponds to moderate feedback regime [10], resulting in characteristic saw-tooth like SM fringes. Even if speckle occurs [11], SM operating regime can be made stable [12]. As each fringe corresponds to half wavelength ($\lambda/2$) target displacement so $\lambda/2$ sensor resolution can be easily achieved by using classical fringe counting [13].

In order to improve SM sensor resolution beyond $\lambda/2$, different phase unwrapping methods (PUMs) have been previously proposed [14-16]. The problem with these PUMs is their need of an iterative routine for joint estimation of C and

linewidth enhancement factor (α) parameters, making this approach slow and time-consuming for real-time applications.

In this context, for fast and time critical applications, a frequency domain analysis, proposed by [17], replaced the slow iterative process of conjoint C and α estimation resulting in a time-frequency signal processing (TFSP) approach. This approach not only allowed vibration extraction in a fast manner but also provided comparable sensor resolution as compared with previously proposed PUMs.

Likewise, a still better real-time natured algorithm was proposed in [18] based on consecutive sample based unwrapping (CSU). Just as in TFSP, CSU also doesn't require estimation of SM parameters or huge iterative routines, making it suitable for real-time, compact, low cost and self-aligned sensor design. Furthermore, CSU is even faster than TFSP because no FFT or IFFT or any computationally intensive transform is used by it. Thus, CSU is the fastest algorithm to process SM signals for displacement retrieval.

The main objective of this paper is the FPGA-based hardware implementation of these previously proposed CSU and TFSP algorithms. Such an implementation of these metric SMI algorithms paves the way towards a complete digital SM sensor integration on chip, capable of delivering real-time measurements for vibration and displacement applications in an embedded, autonomous manner.

The remainder of this paper is organized as follows: Section II and Section III describe the TFSP and CSU algorithms and their hardware implementation on FPGA respectively. Section IV presents the results and discussion. Finally, Section V provides the conclusions.

Figure 1. Schematic diagram of the embedded real-time self-mixing displacement sensor with an FPGA, requiring only a laser diode package with its built-in photodiode and a focusing lens. A piezoelectric transducer (PZT) is used as moving target. Optical output power variations $P(t)$ at laser diode are processed through FPGA to retrieve the target displacement $D(t)$.

II. TFSP AND ITS HARDWARE IMPLEMENTATION

TFSP [17] retrieves target vibration from rough laser feedback phase by means of a frequency domain analysis. TFSP can be divided into three major parts: fast Fourier transform (FFT), Noise Removal and Inverse fast Fourier transform (IFFT), as shown in Fig. 2.

By means of FFT, time domain roughly estimated feedback phase from SM signal is converted into frequency domain. Then, in Noise removal block, noise floor as well as frequency components making up the target motion are analyzed. Noise and unwanted frequency components are thus removed from main frequency tones. Finally, IFFT provides clean, noiseless retrieved target displacement with better resolution.

Fig. 3 (a) shows an SM interferometric signal for a vibrating target illuminated with a laser diode emitting at 785nm. Fig. 3 (b) shows roughly retrieved feedback phase, while Fig. 3 (c) shows the retrieved target vibration from our FPGA based hardware design after applying TFSP on roughly retrieved signal of Fig. 3 (b).

Figure 2. Block diagram of Time-Frequency Signal Processing of roughly retrieved phase from SM interferometric sensor signal.

FPGA-based hardware implementation of TFSP is done in Xilinx ISE tool using VHDL. FFT/IFFT IP Core is used for hardware implementation of the FFT and IFFT blocks. While Noise removal block is implemented by applying thresholding on the output of FFT block. Thresholding allowed only certain components to pass to next block, noise and unwanted signal are thus set to zero.

Figure 3. (a) SM interferometric signal composed of 10Hz-15Hz-25Hz-30Hz corresponding to a target vibration for a Laser emitting at 785nm, (b) roughly retrieved target vibration, (c) TFSP retrieved target vibration.

III. CSU AND ITS HARDWARE IMPLEMENTATION

CSU [16] algorithm retrieves target displacement from SM signal by means of a fast signal unwrapping approach. As the saw-tooth like shape of SM signal fringes belonging to a restricted moderate feedback regime [19] has a quasi-linear local relation to the target motion so precision beyond $\lambda/2$ can be achieved by utilizing this local linearity of SM fringes [19].

The task thus is simplified to unrolling or unwrapping of all SM fringes at all instances where the laser feedback phase crosses 0 or 2π . Such an unrolling can be achieved through fringe detection followed by fringe counting so as to increase the precision of displacement retrieval well beyond $\lambda/2$. Due to its simple and fast nature, CSU has been previously deployed on a micro-controller and used in conjunction with an adaptive-optics based SM displacement sensor prototype enabling robust optical feedback regime stabilization [19].

CSU algorithm can be divided into three major parts i.e. Fringe detection, Staircase signal formation, and fusion, as shown in Fig. 4.

Fringe detection block identifies all fringes contained within SM interferometric signal, while staircase signal formation block provides a staircase signal by counting all the positive and negative fringes in the SM signal. In fusion block, staircase signal is added with scaled version of SM signal to better retrieve the target displacement.

FPGA-based hardware implementation is done using VHDL in Xilinx ISE tool. On hardware, fringe detection block is made up of a subtractor taking derivative of SM signal, followed by thresh-holding on it to provide all the fringes present in SM signal, as shown in Fig. 5 (b).

Staircase signal block consists of a simple fringe counting to produce a staircase signal by continuous addition/subtracting of fringes according to their direction, as shown in Fig. 5 (c). The fusion block consists of an adder and multiplier, it takes SM signal and staircase signal as input, and add them in an appropriate manner after judiciously scaling SM signal to retrieve target displacement from SM signal, as shown in Fig. 5 (d).

Figure 4. Block diagram of Consecutive Sample Unwrapping of SM interferometric sensor signal for displacement retrieval.

Figure 5. Displacement retrieval through Consecutive-Samples based Unwrapping. (a) Normalized SM signal, (b) fringe detection, (c) stair-case signal formation by fringe counting, and (d) the retrieved displacement signal obtained by the fusion of signals (a) and (c).

Fig. 5 (a) shows normalized SM interferometric signal of moderate feedback regime produced due to target motion, used as input while implementing and testing CSU design on FPGA. Fig. 5 (b) shows the output of fringe detection block, while Fig. 5 (c) shows the staircase shaped signal achieved from the 2nd block of CSU involving fringe counting. Fig. 5 (d) shows the retrieved displacement using our hardware designed of CSU algorithm of FPGA.

IV. RESULTS AND DISCUSSION

ZYNQ 7000 series, 28 nm FPGA board is used for implementation and testing of both the algorithms. This section is further divided into two sections i.e.: TFSP Results and CSU Results.

A. TFSP Results

A total number of 16k samples of SM signal shown in Fig. 3 (a) are used in 32-bit fixed point format for the hardware design of TFSP on FPGA.

Table I shows the timing report of our TFSP design. Our TFSP hardware designed system can operate at a maximum frequency of 363.3MHz, with the latency of 570k cycles.

TABLE I. TIMING SUMMARY OF TFSP DESIGN

Speed Grade	-3
Minimum Period	2.752ns
Maximum Frequency	363.332MHz
Minimum input Arrival time after Clock	1.022ns
Maximum Output required time after Clock	0.672ns

Table II shows the device utilization summary. The design consumes 5056 slice registers, and 5192 LUTs on the FPGA, while it consumes 0.756 watts of onboard power.

TABLE II. DEVICE RESOURCES UTILIZATION SUMMARY FOR TFSP

Slice Logic	Used
Number of Slice Registers	5056
Number of slice LUTs	5192
Number of Occupied Slices	1724
Number of LUT Flip Flop pairs used	5229
Number of Bounded IOBs	212

Retrieved target vibration obtained from our FPGA based hardware design of TFSP can be seen in Fig. 3(c). From Fig. 3, it is clear that our designed hardware successfully retrieved the motion from the roughly estimated phase shown in Fig. 3 (b).

B. CSU Results

A total number of 1k samples of SM signal shown in Fig. 5 (a) are used in 16-bit fixed point format while testing the hardware design of CSU on FPGA.

Table III shows the timing report of our CSU design. Our CSU FPGA-based design can operate at a maximum frequency of 432MHz, with the latency of 3 clock cycles.

TABLE III. TIMING SUMMARY OF CSU DESIGN

Speed Grade	-3
Minimum Period	2.315ns
Maximum Frequency	432.021MHz
Minimum input Arrival time after Clock	1.205ns
Maximum Output required time after Clock	0.562ns

Table IV shows the device utilization summary. The design consumes 159 slice registers, and 215 LUTs on the FPGA while it consumes 0.7 watts of onboard power.

TABLE IV. DEVICE RESOURCES UTILIZATION SUMMARY FOR CSU

Slice Logic	Used
Number of Slice Registers	159
Number of slice LUTs	215
Number of Occupied Slices	55
Number of LUT Flip Flop pairs used	215
Number of Bounded IOBs	65

Fig. 5(d) shows the output displacement result obtained from our FPGA-based hardware design. It is clear that our designed hardware successfully retrieved displacement from the SM interferometric signal presented in Fig. 5 (a).

V. CONCLUSION

In this work, we performed FPGA-based hardware implementation of TFSP and CSU algorithms for self-mixing laser interferometric sensor. The designed hardware algorithms are tested and implemented on a Xilinx ZYBO Zynq 7000 development board. Results show that, our FPGA based hardware design of TFSP can operating at 363 MHz clock frequency. It consumes 5056 slice registers and 5192 Slice LUTs, and draws 0.8 Watt of static onboard power. Similarly, extracted results from CSU hardware implementation show that, it can operate at 432 MHz and consumes 159 slice registers and 215 LUT's, and draws 0.70 Watts of onboard power.

This successful FPGA based hardware implementation of these two metric algorithms for SMI is a significant step towards a complete digital SM sensor integration on a chip, which would be capable of delivering nanometric precision for real-time applications of vibration and displacement sensing in an embedded and autonomous manner.

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