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Abstract

This research aims to enhance the understanding on position and size effects on the electro thermal behaviour of low voltage power MOSFET transistors in forward bias condition. The numerical simulations is based on a fractional design of experiments (DoE). The performance of a finite elements model is discussed by comparing thermal and electrical measurements to results of finite elements simulation on a module of free void and voiding solder. The void in the model is afterwards parameterized in position and size, according to the fractional DoE of the study. The combined functions issued from the parametric simulations the DoE show the main impact of void size on temperature of the device and on the surface temperature of the bonding wires. From the numerical viewpoint, the most impacting position of void depends highly on the void size. The redistribution of current density and temperature on MOSFET chip and bonding wires due to solder void is also observed. A future experimental study in respect to the same DoE, is expected in prospect, in order to fulfil the complementarity for this approach.

1. Introduction

Power devices (MOSFET, JFET…) are expected to operate under harsh conditions (temperature, vibration, humidity, electrical constraints …). In particular, in automotive and avionic applications, the recent technologies tend to transport a large amount of power density through the power device (over 100W/cm²). Therefore, device packaging needs an efficient solution to remove heat from the active device to the cooling system.

In the conventional architecture of power assembly, the power device commonly is attached to the substrate by a solder material. This layer plays a critical role in the packaging because of high power density dissipated within the die and high current density which is flowing through. During the power module assembly process, voids can be formed due to poor finishing quality of the substrate surface, presence of residue or imperfection in reflowing process [1-3]. Unfortunately, voids prevent heat transfer to cooling system and lead to current redistribution which depends on the electro thermal characteristics of power device [4]. Consequently, local hot spots can be formed in the active device [5]. This local temperature rise is known at the main factor which affects the device performance and reliability [6]. Thus, voids must be controlled at an acceptable level. Void impact on power device performance and reliability had been investigated in different methods: analytical method [7], numerical method equipped with finite elements software such as ADINA [7], ANSYS[1], [8] or ICEPAK[9]. L. Chen [1] suggested a statistical approach by generating random rates of voids in a finite elements model. In this paper, we introduce another statistical approach based on fractional DoE. The DoE allows to evaluate the selective responses of a system in taking into account not only the main factors but also their interactions, by a minimum of experimental tests. At first, the conception of the fractional DoE will be presented. Later on, we present a numerical coupled field electro thermal model and evaluate its performance by correlating the simulation results to thermal and electrical measurement. The parametric simulations, based on the above DoE, extract the combined functions linking two selective responses to voids position and size. A brief description of a method for controlled void generation in solder joint will be introduced at the end of this paper.

2. Conception of fractional DoE

This chapter introduces our methodology for the conception of the fractional DoE based on three main factors: void position (X, Y) and size (T). The DoE is generated thanks to Design of Expert ™ software

after the definition of study field and the discretization of factors. This step asks for a compromise between the desired accuracy, which qualifies the number of tests to perform and the resource availability, especially materials and finance.

2.1. Hypothesis for the study

From the state of the art, solder voids effects depend mainly on their position [5], [9-10], their size [1], [5], [7-10] and their distribution [1], [5], [11] for a functional assembly and a given operating mode. In our framework, the void is supposed to be cylindrical form. Being limited by the number of equipped assembly prototypes and timing, we investigate effect of only on void on three independent factors: position (X, Y) and size (T). The DoE takes into account the effect due to the main factors (X, Y, T) and their secondary interactions (XY, XT, YT). The effect due to the triplet XYT is assumed negligible. Until now, the DoE is linked to a factorial model. Only information at the extremities from the field study can be directly accessible. In order to get more information inside the study field, we define supplementary levels for the factors X, Y, T, which requires to evaluate the frame curvature X^2, Y^2, T^2. The DoE relies on, from now on, a polynomial model. It requires 10 independent tests for the solving of the system of 10 variables:

$$\text{response} = \alpha_0 + \alpha_1 X + \alpha_2 Y + \alpha_3 T + \alpha_4 XY + \alpha_5 XT + \alpha_6 YT + \alpha_7 X^2 + \alpha_8 Y^2 + \alpha_9 T^2 \quad (1)$$

The DoE software generates the test configurations in respect to orthogonality principle, which represent the symmetry degree of the experimental points, and good conditioning of the system. Nevertheless, the solution of the system (1) is unique. In order to evaluate the responses accuracy, we add three randomized points into the study field.

2.2. Definition of the fractional DoE

The fractional DoE is built from the identification of the impacting factors, the parametric definition of the study field, and the selective responses that we need to analyse. A complementary numerical study showed the influence of the position of a 3mm–diameter void on the temperature distribution in the bonding wires. This phenomenon is observed on a MOSFET transistor in forward bias

conditions of 200A. The phenomenon, related to the relative position between the void and bonding pads, asks for test points placed inside and outside the bonding pads area. In the fig. 2, the bonding pads on the first line are named 1H, 2H, …, 8H et and those on the second line are named 1B, 2B, …, 8B. The MOSFET chip is characterized by its length L_p along vertical Y-axis, its width W_p along horizontal X-axis.
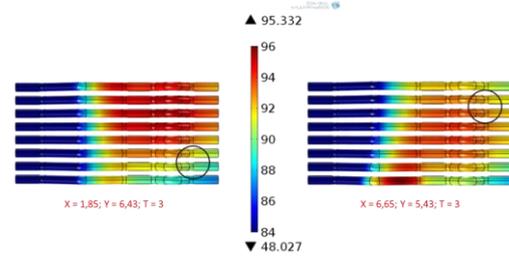

Fig.1: Temperature redistribution due to the change of void position (X, Y)

The pads are referred to the MOSFET chip by E_h (minimal distance between bonding wires and Y-axis), W_{bw} (bonding wires diameter), D_h (distance between 2 adjacent bonding wires), E_v (minimal distance between bonding wires and X-axis, L_{bw} (pads width) and D_v (distance between 2 pads of the same wire).
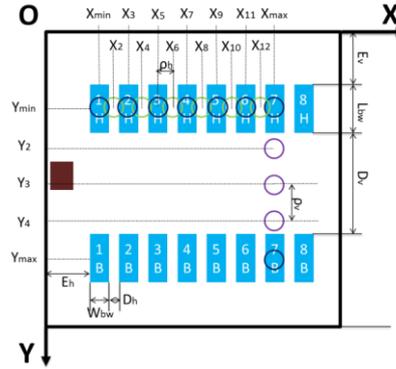
Fig.2: Position of bonding pads. Identification of possible positions of void to investigate

2.2.1 Identification of the levels of T

The study field of the factor T is deduced from the empirical acceptability criteria. The acceptability criterion applied to single void is related to 2mm–diameter void. We are interested in the voids whose diameter varies from 1mm to 3mm, corresponding to a voids rate varying from 1.2% to 11.2%. Moreover, the material constraint oblige to set the discretization step at 500μm.

2.2.2 Identification of the levels of X and Y

The positions of void center along X-axis is classified into two groups: the void center localizes at the middle of the bonding pads (group 1) and at the middle of two adjacent bonding wires (group 2). The possible horizontal positions of void are defined from (2):

$$X_m = E_h + \frac{m}{2}W_{bw} + \frac{m-1}{2}D_h \qquad (2)$$

where E_h, W_{bw}, D_h are 1.326mm, 0.5mm and 0.3mm respectively. As void geometry must be kept inside the solder under the MOSFET chip, m takes integer values from 1 to 13 (figure 2).

The positions of void center along Y-axis are also classified into two groups: the void center localizes inside (group 1) and outside (group 2) the bonding pads area. As the void geometry must be kept inside the solder under the MOSFET chip, the starting point of Y is placed at the centers of the bonding pads H and the ending point of Y is positioned at the centers of the bonding pads B. We add three supplementary levels which are uniformly distributed. Thus, one of these points is placed in the middle of the study field (figure 2):

$$Y_n = E_v + \frac{n+1}{4}L_{bw} + \frac{n-1}{4}D_v \qquad (3)$$

where n takes integer values from 1 to 5. E_v, L_{bw}, D_v are 1.47mm, 1.3375mm et 2.676mm respectively.

The levels of the influencing factors are summarized in the columns N°1, 2 and 3 of the table 1. The 13 test configurations given by the DoE software are shown in the columns N°4, 5 and 6 of the same table.

Table 1: The built fractional DoE

Discretization level (reference : MOSFET)			Conception of DoE (reference : Solder)			N° test
X-Level (mm)	Y-Level (mm)	Z-Level (mm)	X (mm)	Y (mm)	T (mm)	
1.85	2.42	1	4.65	4.42	1	1
2.25	3.42	1.5	5.45	4.42	2	2
2.65	4.42	2	1.85	4.42	2	3
3.05	5.43	2.5	3.45	2.42	3	4
3.45	6.43	3	3.05	3.42	1.5	5
3.85			6.65	5.43	3	6
4.25			6.65	6.43	1	7
4.65			1.85	6.43	1	8
5.05			1.85	2.42	1	9
5.45			3.05	5.43	1.5	10
5.85			1.85	6.43	3	11
6.25			6.65	2.42	2	12
6.65			4.25	6.43	2	13

The selective responses for voids impact evaluation are a compromise between the industrial exigencies on performance and the measurement accessibility. The maximal temperature on bonding wires surface and inside the chip are selected at the first time of this study.

3. Evaluation of void effects by numerical method

In order to validate numerical approach, a benchmark experiments for finite elements simulation will be carried out. The benchmark will be firstly set on the module in which the voiding solder is negligible, and secondly, on the module of realistic 1.26mm-diameter-void in the solder joint.

3.1. Description of finite elements model

A reference model is designed in COMSOL® Multiphysics in which we set an optimized meshing of about 80000 elements and direct solver for electro thermal coupling. This simplified model in presented in figure 3. The simplified model allows to reduce the calculating time in retaining analogue with the power module, which compose 4 embedded MOSFETs forming a converter leg. Three MOSFET transistors (orange crosses), are not functional. In fact, only one transistor is modelled among the 4 MOSFETs. The complex geometry elements are simplified (electrical connectors, lead frame, back plate) or removed (gel, encapsulation) from the model.
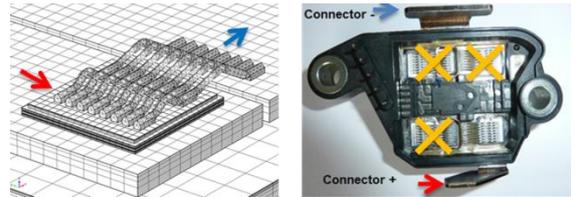

Fig.2: Meshing on simplified model and real MOSFET module

In the previous studies, the electro thermal coupling is mostly neglected. A nonlinear electro thermal model has been recently introduced by X. Chauffleur [12], in which the total dissipating power was discretized into two elementary dissipating areas. Thus the active layer of power MOSFET was dissociated from the highly doped N+ substrate layer. In the conventional structure of planar MOSFET, the ON-state resistance R_{dsON} is discretized into 4 elementary resistances, representing 4 resistive areas [13]. However, the selective indicator of performance (temperature in the profile across the void) is not sensitive to the modes of volume repartition of dissipating power in the active layer. As a result, the MOSFET device is modelled consequently in two layers: active layer of 10μm-thickness and substrate N+ layer of 225μm-thickness.

In our model, the aluminium-metallization layer and the MOSFET chip have the same surface (7.95mm x 7.96 mm). The semiconductor chip is brazed on the multilayer substrate: copper (50μm) – invar (150μm) – copper (50μm) thanks to a 130μm-thickness solder. The lower face of the substrate is brazed on the lead frame by the second solder layer having the same thickness (130μm). The lead frame is afterwards assembled to the aluminium-back plate by a thin layer of insulator material. The back plate is finally connected to the cooling system by a thermal grease.

The thermal and electrical properties of used materials in the model are issued from the supplier datasheets, and mostly temperature-independent, except for the electrical resistivity of aluminium, copper and doped silicon in the MOSFET chip. The electrical resistivity of copper (ρ_{Cu}) and one of aluminium (ρ_{Al}), in Ωcm, is defined as the function of temperature following the linearity laws (4) and (5):

$$\rho_{Cu} = 4.10^{-8} + 1.25.10^{-10}(T - 400) \qquad (4)$$

$$\rho_{Al} = 3.2.10^{-8} + 8.10^{-11}(T - 500) \qquad (5)$$

The electrical resistivity of highly doped silicon in substrate layer is estimated from [14]. For a doping rate of $10^{19} cm^{-3}$, the equivalent electrical resistivity is about 10^{-2} Ωcm. This one is quasi-constant from 20°C to 200°C. From the given information of R_{dsON} (datasheet), the electrical resistivity of the active layer can be deduced thanks to the formula (6):

$$R_{active} = \frac{\rho_{active} \times l_{active}}{S_{active}} \qquad (6)$$

where R_{active} is the resistance of active layer, ρ_{active}, l_{active}, et S_{active} are respectively its resistivity, length and area.

Table 2 : Equivalent resistivity of active and substrate N+ layer

T_{MOS} (°C)	-40	25	175	200
ρ_{N+} (Ωm)	10^{-4}	10^{-4}	10^{-4}	10^{-4}
ρ_{active} (Ωm)	$8.51.10^{-4}$	$1.66.10^{-3}$	$4.08.10^{-3}$	$4.67.10^{-3}$

The inlet current is applied to the lateral face (red arrow on plus connector). The outlet courant quits the module (blue arrow) at the lateral surface of the second lead frame (figure 2).

The boundary conditions for thermal model is supposed adiabatic except for the lower face of the assembly where the convection exchange is expressed by the convective heat transfer coefficient of 4000W/m²K at the reference temperature (23° C).

3.2. Validation du modèle numérique

The benchmark for the modules of free void and voiding solder is performed under pulse conduction 500A – 100ms. The current profile of current inlet for simulation is extracted from the measured current during the injection.

3.2.1 Evaluation of the performance of the model of free void solder

The results from finite elements simulations are compared to those obtained by electrical and thermal measurement on module of free void solder. The figure 3 depicts the evolution of drop voltage across the module terminals. We recognize a slight gap between the simulated and experimental curve at the beginning of the injection. This gap is no longer significant at the end of the injection (after 60ms). The finite element model seems to be performant for simulation in stationary mode.
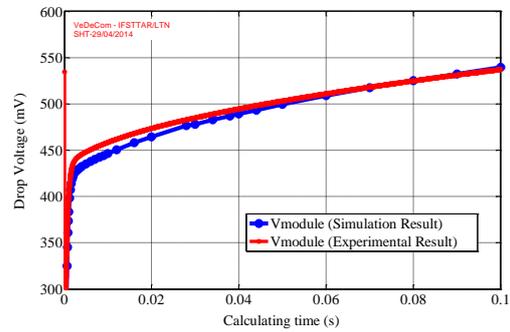

Fig.3: Evolution of drop voltage across the module terminals

The simulation results are also well-linked to experimental ones on thermal viewpoint. The figure 4 performs the evolution of the maximal temperature at the surface of bonding wires. The thermal measurement is performed by infrared camera CEPIP-FLIR SC7500.
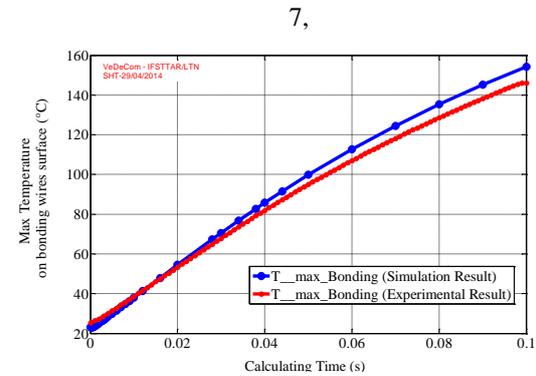

Fig.4 : Evolution of maximal temperature on the bonding wires surface

3.2.2 Evaluation of the performance of the model of voinding solder

In parallel, the benchmark is carried out on a module with voiding solder. The module for this study is selected from a great number of modules thanks to X-ray images. The 1.26mm-void positioning at X = 5.23mm and Y = 2.89mm, is "naturally" formed during the process (figure 5)
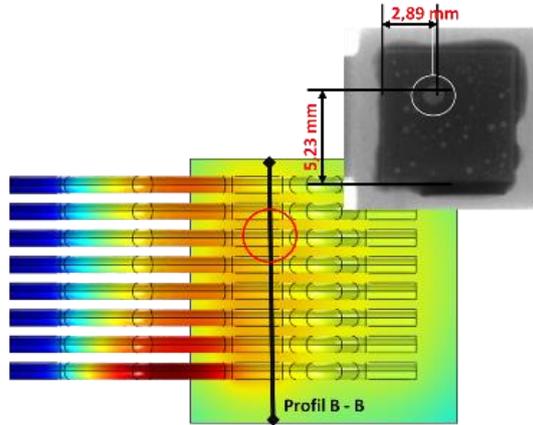
Fig.5: Single void in the used module

The simulation performs a slight temperature rise in void area, which is coherent to thermal response obtained by infrared measurement. Nevertheless, in quantitative and qualitative viewpoint, the benchmark needs to be improved. The benchmarks based on test prototypes with well-controlled voids are necessary for a robust validation of voids impact. However, the result presented above allows to enhance the degree of confidence on the numerical model.

3.3. Extraction of void effect by numerical approach

3.3.1. MOSFET Characterisations I(V, Tj) device

The characterizations I(V, Tj) provide more accurate information on the device behaviour for the finite elements model. The characterization test bench developed at LTN (Laboratory of New Technologies) allows to realize the electro thermal characterizations with forward current up to 250A and temperature up to 200°C. The table 3 depicts the electrical resistivity of the active and N+ substrate layer in relation to the temperature measured on the upper layer of the copper substrate. The calculation is deduced from the R_{dsON} given by I(V, Tj) characterization, the resistance of the substrate area according to its doping rate, thanks to the formula (6):

Table 3 : Equivalent electrical resistivity of the MOSFET layers

T(sub) - °C	37.8	91.6	114.0	135.9	157.4
RdsON - mΩ	0.98	1.12	1.19	1.26	1.33
R(N+) – mΩ	0.36	0.36	0.36	0.36	0.36
R(active layer) - mΩ	0.62	0.76	0.83	0.90	0.97
Ro_active - Ωm	$3.92.10^{-3}$	$4.87.10^{-3}$	$5.30.10^{-3}$	$5.70 10^{-3}$	$6.19.10^{-3}$

3.3.2. Responses surface analysis

The characterizations I(V. Tj) obtained in 3.3.1 fulfil the finite elements model. The parametric simulations, relying on the fractional DoE designed above, allow to perform the maximal temperature at bonding wires surface and inside the MOSFET device (table 4). The parametric simulations have been carried out under continuous forward current of 200A.

Table 4 : Responses from finite elements simulations

Factor X (mm)	Factor Y (mm)	Factor T (mm)	Tmax (wires)	Tmax (MOS)
4.65	4.42	1	116.4	116.3
5.45	4.42	2	118.8	119.2
1.85	4.42	2	119.6	119.1
3.45	2.42	3	127.1	127.0
3.05	3.42	1.5	117.7	117.4
6.65	5.43	3	124.9	125.1
6.65	6.43	1	116.4	116.0
1.85	6.43	1	116.5	116.2
1.85	2.42	1	116.5	116.2
3.05	5.43	1.5	117.6	117.2
1.85	6.43	3	127.8	126.6
6.65	2.42	2	119.9	119.6
4.25	6.43	2	119.3	119.1

The Design of Expert ™ software extrapoles two combined functions derived from the obtained reponses. These functions quantify void effects according to their position and size. In order to evaluate the contribution of each factor on global impact, all factors are expressed in standardized value. The maximal, minimal and average values applied to these factors are 1, -1 and 0 respectively. The combined functions given by the fractional DoE for numerical simulations are extracted in (7) and (8):

$$T_{max}(fils) = 119.24 - 0.42X - 0.29Y + 4.89T - 0.36XY - 0.66XT - 0.07\ YT - 0.02X^2 + 0.45Y^2 + 2.04T^2 \quad (7)$$

$$T_{max}(MOS) = 119.29 - 0.21X - 0.33Y + 4.94T - 0.23XY - 0.37XT - 0.11\ YT - 0.26X^2 + 0.21Y^2 + 0.98T^2 \quad (8)$$

As a référence, the finite elements simulation in module of free void solder provides T_{max} (fils) = 116.1°C and T_{max} (MOS) = 115.9°C. We notice that the coefficients linked to T are clearly higher than those linked to X and Y, which means the effect due to the size of void is predominant. The test N° 8 and 11 help to clarify this observation. The temperature rise in the chip and at the bonding wires surface due to a 3mm-diameter void is about 10°C. Meanwhile, the temperature elevation in case of 1mm-diameter void is just only 1°C. On the contrary. the effect due to 2 voids placed on different positions is practically similar.

Another remarkable observation is that. the most impacting position on selected responses is more difficult to identify. It depends on the void size. For example, the observation on the maximal temperature on bonding wires surface (R1) can illustrate this phenomenon. In case of small void (T < 2mm). the plus impacting position localizes near (X_{max}, Y_{min}) (red area on the left of the figure 6). Otherwise, this position tends to (X_{min}, Y_{max}) (red area on the right of the figure 6) when the void size increases. In fact, this phenomenon is due to many coupling effects: the initial current flow and thermal flow which depend mostly on the model geometry, the electro thermal coupling of used materials properties, the performance of the cooling system, and the characteristics of the void.

As another illustration of this pointview, the figure 7 depicts the variation of current level in the eight bonding wires (abscissa) caused by 2 voids, compared to free void module. The void A localizes at X = 5.45mm (under the pads 5B, 6B, 7B) and the void B one localizes at X = 1.85 mm (under the pads 1B, 2B, 3B). These voids possess the same size (2mm) and coordinate (4.42mm). We notice that the area in which the current drops in the bonding wires is related to the void area.

In fact, the current flow is deviated from the void area being poorly electrical conductor. In the local region, the direction of current flow is by preference lateral to vertical, which leads to a local drop of

current density in void area and the rise of current density in the remaining domain. The temperature on device replies to 2 opposite effects. On the one hand, it tends to increase due to the underneath thermal barrier. On the other hand, it tends to decrease due to the local density drop.
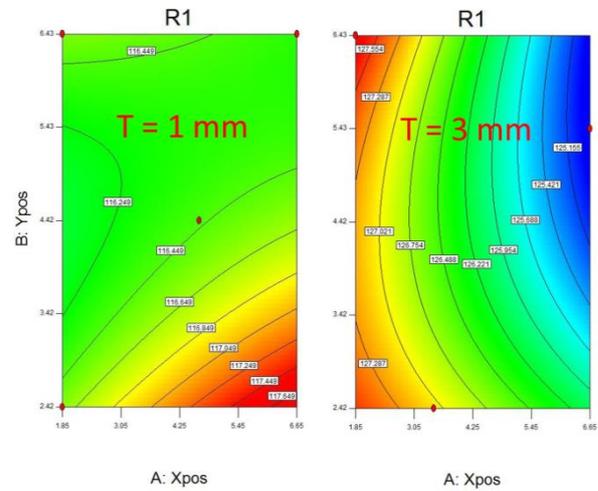

Fig.6 : Displacement of critical point from (Xmax, Ymin) towards (Xmin, Ymax) when the void size increases
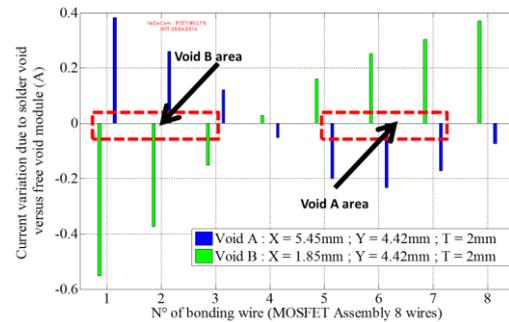

Fig.7 : Current variation in bonding wires due to two voids A and B versus free void

On our MOSFET assembly, the effect due to the variation of current density is not significant enough to overcome the effect the thermal barrier of void. The current variation in the bonding wires is only about 0.4A. As a result, the temperature is always higher in module with void than free void module.

4. Controlled void creation

The experimental benchmark for simulation study required 13 test vehicles. The voids must be created in these test vehicle in respect to the same fractional DoE, which requires to control the voids at the desired position and size. We introduced in this last chapter, a method allowing to generate void in

controlling its position and size. This method is based on two parameters: flux quantity and laser shot duration. In fact, the flux quantity must be little to create a site of preferential germination of voids. Furthermore, the laser shot duration must to be short enough to do not allow the flux to react completely. The residual flux, will form as a consequence, a source of gas (void).

A test prototype consists of a copper substrate, a MOSFET chip and SAC solder preform (SnAgCu). The preform is placed between the chip and the substrate. The solder is performed by DLS (Die Laser Soldering) technology. The laser shot is applied to the bottom surface of the substrate, and lead to the melting of the preform SAC. To generate a void at desired location and size, a 100µm-depth hole is drilled in the substrate at controlled position and size. The activation of the residual flux is ensured by trapped flux in the hole. The flux quantity is defined in relation to the hole volume. The laser shot duration is shorter than the duration by default. The figure 8 shows the creation of a 2mm-diameter void, and prove the performance of this method.
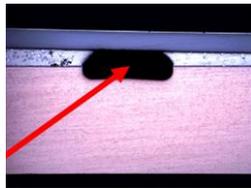

Fig.8 : A well-controlled 2mm-diameter void

5. Conclusion

The result issued from this framework shows a performant method allowing to evaluate the electro thermal behaviour of forward biased MOSFETs transistor due to solder void. The finite elements model allows to take into account the electro thermal coupling and to show it performance as far as accuracy and calculating time. The numerical results based on the conception of fractional DoE extract a priori the combined function for voids impact evaluation. Several remarkable phenomena have been observed and interpreted by numerical simulation viewpoints. The experimental tests. based on the same fractional DoE. will be performed in the next stage of this study . The experimental results will justify the accuracy of the combined function. A method for man-made void creation in solder will be presented shortly. This method will be used to build test vehicles in which the void in the solder is generated in respect to the DoE.

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