Preliminary Evaluation of Thermo-Sensitive Electrical Parameters Based on the Forward Voltage for Online Chip Temperature Measurements of IGBT Devices

Laurent Dupont, Yvan Avenas

Accepted by IEEE for publication in 2015 :
DUPONT, Laurent, AVENAS, Yvan, 2015, Preliminary Evaluation of Thermo-Sensitive Electrical Parameters Based on the Forward Voltage for Online Chip Temperature Measurements of IGBT Devices, IEEE Transactions on Industry Applications, 6, 51, IEEE PRESS, pp.4688-4698, DOI: 10.1109/TIA.2015.2458973

Preliminary Evaluation of Thermo-Sensitive Electrical Parameters Based on the Forward Voltage for On-line Chip Temperature Measurements of IGBT Devices

Laurent Dupont
IFSTTAR, COSYS-LTN
25 allée des Marronniers, F-78000 Versailles, France
Laurent.Dupont@ifsttar.fr

Yvan Avenas
Univ. Grenoble Alpes, G2Elab, F-38000 Grenoble, France
CNRS, G2Elab, F-38000 Grenoble, France
Yvan.Avenas@g2elab.grenoble-inp.fr

***Abstract*— The temperature of power semiconductor devices is one of the main issues affecting the performance, availability and reliability of power converters. The chip temperature is generally measured using Thermo-Sensitive Electrical Parameters (TSEPs). These parameters are well controlled for laboratory temperature measurements where the power devices are not used under functional conditions. However, the use of TSEPs for chip temperature measurements in on-line conditions has yet to be demonstrated. This paper presents an experimental evaluation of two new TSEPs based on measuring the forward voltage, which could be used during operation of the converter. It examines the accuracy of the chip temperature measurement and also discusses the results in terms of robustness to the aging of power devices.**

***Index Terms*—Power semiconductor, temperature, infrared measurement, IGBT, saturation voltage, thermo-sensitive electrical parameter.**

I. INTRODUCTION

The temperature of power semi-conductor devices is one of the main issues affecting the performance, availability and reliability of power converters. Knowing this temperature is of great interest for evaluating the thermal performance of power modules (thermal resistance and impedance measurements) and also for estimating the degradation levels of the devices during accelerated aging tests carried out in laboratory environments [1-2]. Several solutions exist for measuring the chip temperature [3]. Among them, Thermo-Sensitive Electrical Parameters (TSEPs) are currently the most used in industry and academia because they make possible high speed indirect chip temperature measurements without any physical modification of power modules.

In this context, the use of a TSEP is based on a physical relationship between an electrical parameter and the temperature of a power semiconductor. The calibration of a TSEP is therefore based on the measurement of an electrical parameter of a power device as a function of the temperature. This temperature is modified by an external system, the power chip being in its final environment, i.e. in the power module under examination. If the self-heating of the device is negligible during this calibration step, the chip temperature can be evaluated from the measurement of the electrical parameter. Two types of TSEPs can be distinguished. The first group consists of TSEPs which are used in non-functional (i.e. off-line) conditions. They are usually used in laboratory environments for measuring thermal resistances and impedances and also for carrying out damage evaluation during accelerated aging tests. The most used TSEP of this first group is the forward voltage under a low current. In the case of an IGBT or a MOSFET, the threshold voltage and saturation current are also possible candidates. These off-line TSEPs can also sometimes be employed for temperature measurements in functional systems, but the control and operation of the converter have to be modified [4]. The second group is made up of TSEPs which can be used in on-line conditions. In this case, the temperature measurements are carried out during real operation of the converter. For example, such measurements could be used to ensure health-monitoring of the converter during its life, or simply to act on the control strategy of the converter so as to protect the power semiconductors from over-heating. These TSEPs are generally based on measuring the forward voltage under a high current level [5] or on measuring switching times [6]. However, the scientific literature does not provide any demonstration of their effective use in functional power converters.

Nowadays, power module manufacturers offer the possibility of carrying out chip temperature measurements in on-line conditions by integrating temperature sensors into their products. With the help of precise thermal models, it is thus possible to estimate the temperature of active parts. However, the thermal performance of a power system varies with time (aging of the power module and of the cooling system), causing a discrepancy between the thermal modeling and the actual state of the system [7]. Another solution is the inclusion of

a temperature sensor inside the structure of the semiconductor part of the device [8]. Although it is very attractive, this solution generates certain practical problems, such as chips becoming excessively expensive and the structure of the power module becoming more complex. Furthermore, this temperature measurement is only local whereas the chip temperature is significantly non uniform [9]. By contrast, a TSEP gives an "average" value for the chip temperature, making its use more interesting for temperature monitoring.

This paper will seek to add to the not very plentiful literature on this topic by evaluating two new on-line TSEPs dedicated to IGBT devices. Two aspects will be studied: the accuracy of the indirect chip temperature measurements and the impact of power device aging on these measurements. The paper's first part will present the chosen TSEPs. Then the experimental setup will be outlined. Finally, calibration and validation tests will be discussed. This paper will confine itself to evaluating the suitability of the indirect temperature measurements obtained by using these TSEPs; implementation issues will therefore not be discussed.

II. CHOICE OF TSEPS DEDICATED TO ON-LINE MEASUREMENTS

A. Background

As detailed in [10], the scientific literature has so far chiefly examined three types of TSEP for on-line temperature measurements:
- classical (off-line) TSEPs,
- static characteristic I(V),
- dynamic characteristics.

As explained by the authors, all these TSEPs have advantages and drawbacks.

In the case of classical off-line TSEPs, the main advantage is their good accuracy. However, they necessitate the modification of the structure of the converter and/or its operation which can be seen as a serious drawback.

The use of the static characteristic is a natural way to estimate the junction temperature measuring simultaneously the forward voltage and the current crossing a device. The main advantages are the genericity of the method which can be used for all power devices and the possible measurements using the sensors dedicated to the control of the converter. However, several issues are pointed out: non accurate temperature measurements due to series resistances in the package, need of accurate sensors, synchronization of the measurements and noise during the measurements.

The dynamic characteristics can also be naturally used to estimate the junction temperature of switching devices in converters. The dynamic characteristics presented in [10] were: the turn-on delay, turn-of delay or current slope during turn-on. Two drawbacks of these TSEPs were their non-genericity (only transistors) and their low sensitivity (in the range of several nanoseconds or even picoseconds per °C). Other dynamic TSEPs were not presented in [10]. For example, the Miller plateau can also be used as TSEP [11] but it has the same problem of low sensitivity (several ns/°C). The voltage across the emitter-auxiliary emitter parasitic inductance can also be used to have an image of the turn-on [12] or turn-off times [13-14]. In 2014, Luo et al. [15] studied the junction temperature measurement of diodes using maximum recovery current rate di/dt. One major issue is the dependence of this parameter on the switching speed of the transistor in the same switching cell. In fact, because this switching speed depends of the transistor temperature, the knowledge of the diode temperature can only be made knowing the temperature of the transistor. To conclude, one drawback of all dynamic TSEPs is the influence of lots of operating conditions within a converter setup: the voltage, current, gate resistance, gate-emitter voltage, parasitic components… It also has to be noted that there is not any paper which verifies if the temperature estimation is accurate and which deals with the influence of the device aging on this accuracy.

Since the publication of [10], several papers propose to use the variation of the internal gate resistance with temperature to estimate the junction temperature of IGBT devices. Denk and Bakran [16] add a low voltage oscillation to the gate-emitter voltage when the device is in off-state. The voltage amplitude across the external gate resistance is then used as TSEP. The output of a demodulation circuit shows a very good sensitivity (20mV/°C). Baker et al. [17] propose to measure the voltage across the external gate resistance during turn-on. Thanks to the use of a specific electronic circuit including an integrator, a very large sensitivity is obtained (70mV/°C). One intrinsic issue of these methods is their non-genericity: they are not usable with diodes.

As a conclusion, no TSEP is ideal for on-line junction temperature measurements. Generally, authors measure the sensitivity of their TSEPs but do not propose any verification of the temperature estimation when the devices are submitted to dissipation or when they are aged. This work has to be carried out with all TSEPs in the future to obtain comparison elements.

This paper intends to make a contribution in this scientific field with a focus on the use of the static characteristic which is the most generic TSEP and which can be measured with sensors dedicated to the control of power converters. However, it has been demonstrated that temperature measurements using the forward voltage under high current can be very inaccurate [5]. The reason for this inaccuracy is quite simple. The forward voltage is the sum of the voltage across the semiconductor part and the voltage across the power electrical connections. After simplifying assumptions, it is therefore possible to write for an IGBT device:

$$V_{CE,mes} = V_{CE}(T_j, I_C, V_{GE}) + R_{con}(T_{con})I_C \qquad (1)$$

where $V_{CE,mes}$ is the measured forward voltage, I_C the collector current, V_{CE} the forward voltage across the semiconductor part, V_{GE} the gate-emitter voltage, R_{con} the resistance of the electrical connections, T_j the semiconductor temperature and T_{con} the temperature of the power connections. For a given T_j, the temperature T_{con} is not the same under calibration and operation conditions. For example, the temperature of wire-bonding is generally higher than the chip temperature during operation [9], which is not the case during the calibration

step (pulsed current in the device [7]). As a consequence, the collector-emitter voltages measured during the calibration and operation steps are not the same and large errors in temperature measurement can be observed.

Even if the forward voltage as a TSEP is not accurate, it remains attractive because it is relatively easy to measure; it can be used with all power devices; and its sensitivity is relatively high (several mV/°C). This paper will therefore study two TSEPs which are based on the forward voltage but which are less influenced by the resistance of the electrical connections.

B. TSEPs based on the forward voltage

The first TSEP is called $\Delta V_{CE\_\Delta VGE}$. It can be used with IGBT and MOSFET devices. In the case of an IGBT, the principle is to measure the forward voltage using sequentially two gate-emitter voltages V_{GE1} and V_{GE2} under the same collector current I_C. The delay between two measurements has to be low enough to be able to assume that T_j and T_{con} do not vary. Under these conditions, two collector-emitter voltages are measured:

$$V_{CE,mes1} = V_{CE}(T_j, I_C, V_{GE1}) + R_{con}(T_{con})I_C \quad (2)$$

$$V_{CE,mes2} = V_{CE}(T_j, I_C, V_{GE2}) + R_{con}(T_{con})I_C \quad (3)$$

The new TSEP can then be defined as:

$$\begin{aligned} \Delta V_{CE\ \Delta VGE} &= V_{CE,mes1} - V_{CE,mes2} \\ &= V_{CE}(T_j, I_C, V_{GE1}) - V_{CE}(T_j, I_C, V_{GE2}) \end{aligned} \quad (4)$$

where the influence of the electrical connection is cancelled under these hypotheses. Note that this equation is written with simplifying assumptions: the electrical potential of the electrode in the front side and the current in the active part of the die are assumed to be uniform.

Fig. 1a shows the basic principle of this TSEP in the case of an IGBT[3] (600V-200A – Infineon SIGC100T60R3), with a 60A current level and two voltage levels (12V and 15V). It can be observed that the difference between V_{CE}(15V) and V_{CE}(12V) depends on temperature and can therefore be used as a TSEP.

The second new TSEP is called V_0. It can be used with diodes and IGBT devices. Here, the forward voltage is measured under two different current levels I_{C1} and I_{C2}. For IGBT devices, the gate-emitter voltage remains constant. Two collector-emitter voltages are then measured:

$$V_{CE,mes1} = V_{CE}(T_j, I_{C1}, V_{GE}) + R_{con}(T_{con})I_{C1} \quad (5)$$

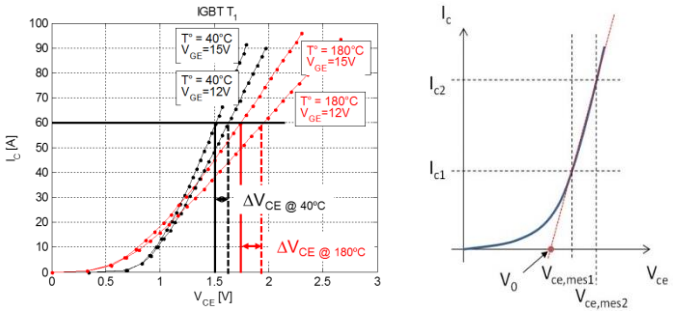
$$V_{ce,mes2} = V_{CE}(T_j, I_{C2}, V_{GE}) + R_{con}(T_{con})I_{C2} \quad (6)$$

As shown in Fig. 1b, V_0 is defined as the intersection between the line including the points (V_{CE1},I_{C1}) and (V_{CE2},I_{C2}), and the line I_C=0. It can be demonstrated that:

$$\begin{aligned} V_0 &= \frac{V_{CE,mes2}I_{C1} - V_{CE,mes1}I_{C2}}{I_{C1} - I_{C2}} \\ &= \frac{V_{CE}(T_j, I_{C2}, V_{GE})I_{C1} - V_{CE}(T_j, I_{C1}, V_{GE})I_{G2}}{I_{C1} - I_{C2}} \end{aligned} \quad (7)$$

As with the previous new TSEP, the influence of the resistance of the electrical connections is clearly cancelled with these hypotheses. This TSEP can be used in applications where the current varies periodically with time, for example in inverters. However, it has to be verified that the temperature of the connections varies only very slightly between two measurements, i.e. the period has to be short enough. Typically, temperature variations of only several °C are acceptable.

One important issue with both of these TSEPs is that they are the result of a subtraction between two voltage measurements which are close to each other. In the following sections, V_0 will therefore be calculated using more than two current values. A linear interpolation function will then be used to calculate this TSEP.



a. $\Delta V_{CE\_\Delta VGE}$ b. V_0

Figure 1. Basic principle of the new TSEPs

III. METHODS AND EXPERIMENTAL TOOLS

A. Experimental setup

An experimental setup was developed to evaluate the new TSEP in the case of a DC dissipated power. The device being tested is a power module (1200V-100A, FS100R12PT4, Infineon) containing IGBTs and diodes in order to create a three-phase inverter (Fig. 2).

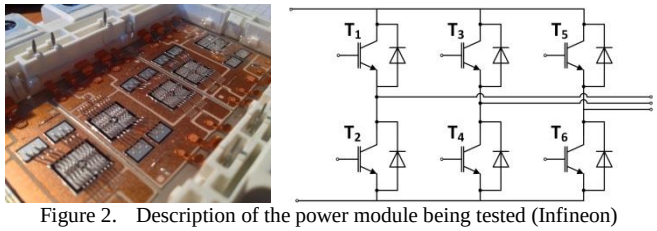


Figure 2. Description of the power module being tested (Infineon)

The IGBT device T_4 is characterized by making numerous I_C current injections and, at the same time, measuring the resulting V_{CE} voltages. The value of I_C being in the range 20 to 200A, it is necessary to produce short pulses to limit the self-heating of the dies during the characterization. Even though a curve tracer could be used to carry out these measurements, a dedicated electrical circuit was created in order to control the shape of the current pulses. Fig. 3 shows the power part of the circuit. The amplitude of the current pulse is controlled by the current supply I_{p1}. The inductor L_1 is used to limit the current variations in the power device during the current injection. The duration of the current pulse is set using a correct control of both MOSFET $Ta_{1,1}$ and $Ta_{1,2}$. The role of the right side of this circuit (I_{p2}, Da_2, $Ta_{2,1}$ and $Ta_{2,2}$) will be discussed later in the paper.

The temperature of the power module is controlled by a cold plate via a graphite thermal interface (thickness 100µm) in order to operate at high temperature up to 180°C in characterization condition and to recover the realistic thermal conditions in dissipation mode. The electrical measurements are carried out with a DEWETRON (DEWE800) acquisition system. The DAQP signal conditioning modules allow fast (sampling rate) and accurate measurements: the sampling rate is 500kHz and the accuracy is ±0.02% of reading + ±0.05% of range). The different elements are controlled with a CompactRio (National Instrument) real time system.

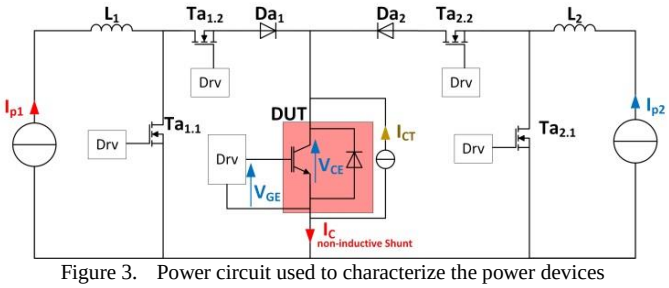


Figure 3. Power circuit used to characterize the power devices

B. Temperature measurements of the dies

Three complementary methods are used to evaluate the temperature of the semiconductor chips:

-one type K thermocouple with an open junction is placed as close as possible to the die, which makes it possible to measure the temperature of the substrate with an accuracy of ±1°C,

-one infrared (IR) camera is used to evaluate the surface temperature of the chips,

-a classical TSEP is compared with the new TSEP: the forward voltage under low current. In the following sections, it will be called $V_{CE\ Ict}$.It has been shown by various authors that this TSEP is robust and gives temperature measurements close to the mean temperature of the chip [18-20].

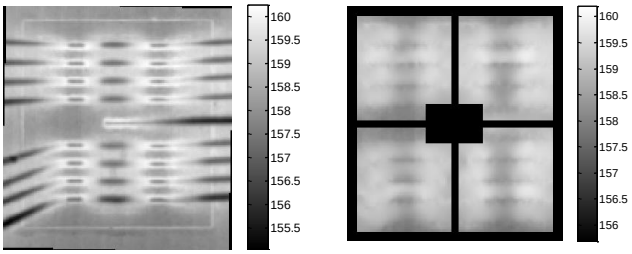
In a first step, the thermocouple and IR camera measurements will be used to characterize the different TSEPs as a function of temperature (Section IV). Then the IR camera and the TSEP $V_{CE\ Ict}$ will be used to estimate the temperature of the chip when it is submitted to stationary power dissipations (Sections V and VI). These measurements will then be compared with those provided by the new TSEPs.

The basic principle of the measurements carried out with the IR camera is described in the next paragraph.

C. Temperature measurements using the IR camera

The reference of the IR camera is CEDIP-FLIR SC7500. To take the measurements, the dielectric gel is removed from the power module. The power chips are then painted (PYROMARK 1200 high temperature paint). The paint is deposited by micro-spraying equipment that gives good control of its thickness. In the following tests, the paint thickness is 15µm. However, the emissivity of the coating was measured for two thicknesses (14µm and 45µm) and three temperatures (23°C, 100°C and 198°C) to validate the opacity of the paint layer for the proposed test conditions. The results of characterization demonstrate that this emissivity is very stable in the wavelength range 2µm to 10µm.

The main issue with using an IR camera to measure the temperature of semiconductor chips is the presence of wire bonding which generates optical artifacts (Fig. 4a). For the temperature evaluations, these artifacts are therefore masked using a digital post-process [20]. The surface temperature of the device is then reconstructed to obtain a more precise estimation of the temperature of the devices' active parts (Fig. 4b).



a. Unprocessed IR image b. IR image after reconstruction

Figure 4. Principle of the IR measurements

The IR measurements are validated by varying the temperature of the cold plate and then comparing the temperature measurements obtained by both the thermocouple and the IR camera. This temperature difference remains smaller than 1°C in the range 20°C to 160°C.

IV. CHARACTERIZATION OF THE TSEPS

A. Methodology

The goal of the characterization step is to obtain the evolution of each TSEP as a function of the chip temperature, gate emitter voltage and collector current. The self-heating of the device during the measurements has to be minimized and estimated to obtain an accurate value of the junction temperature during the V_{CE} measurement. In fact, apart from $V_{CE\ Ict}$, all other TSEPs are measured during a current pulse of high magnitude with a gate-emitter voltage V_{GE} in the range 11-15V. The test conditions therefore induce high power dissipation levels in the chip, meaning that the measurement has to be made within a short timeframe.

The methodology which is used for this characterization step is thus based on V_{CE} voltage measurements during short current injections (300µs) with an estimation of the junction temperature during these measurements. Each current injection sequence in the device consists of three successive steps, the time origin being defined as the beginning of the current pulse:

-Step 1 (-100µs to 0µs): only the current I_{CT}=50mA is injected in the device. This current and the resulting collector-emitter voltage ($V_{CE\ Ict}$) are measured between -100µs and 30µs. This step is therefore used to characterize the TSEP $V_{CE\ Ict}$. The reference temperature is given by the thermocouple.

-Step 2 (0µs to 300µs): a high current I_C is injected in the device. V_{CE}, V_{GE} and I_C are measured between 50 and 100µs.

-Step 3 (300µs to 700µs): only the current I_{CT} is injected in the device. Measuring the collector-emitter voltage between 500 and 700µs, it is possible to estimate the temperature at the end of the current pulse as it will be explained later.

Fig. 5 in the top shows the evolution of V_{CE}, I_C, V_{GE} and I_{CT} during the current pulse. Here, the current level is 180A, V_{GE}=12V and the chip temperature is 170°C. This electrical sequence is duplicated for different I_C levels (10-190A), V_{GE} levels (11-15V) and temperatures (20-170°C). For each temperature, 59 sequences are processed to extract the different characteristics.

This figure also summarizes the methodology which is carried out to estimate the self-heating of the device and therefore to obtain a more accurate evaluation of $V_{CE}(V_{GE},I_C,T_j)$. Because there is not any dissipation in the device before the current pulse, the temperature $T_j(0^-)$ is simply estimated using the thermocouple. As specified above, this measurement also allows for the characterization of the TSEP $V_{CE\ Ict}$. Having the relationship between $V_{CE\ Ict}$ and T_j, it is then possible to estimate the chip temperature at the end of the current pulse. To do that, $V_{CE\ Ict}$ is measured between 500µs and 700µs, then T_j is estimated within this timeframe and $T_j(300µs)$ is estimated using a linear regression of the junction temperature as a function of the square root of time [21]. It has to be noted that there is a 200µs delay between the end of the pulse and the beginning of the $V_{CE\ Ict}$ measurement to prevent the influence of non-thermal transients [21] and to insure an accurate temperature measurement after the current pulse [22]. Knowing $T(0^-)$ and T(300µs), a second linear regression of the

junction temperature as a function of the square root of time is used between 0 and 300µs. The chip temperature is then estimated between 50 and 100µs. At the end of the procedure, an averaging of V_{CE}, I_C, V_{GE} and T_j on this timeframe allows for an estimation of $V_{CE}(V_{GE},I_C,T_j)$ which will be used for the characterization of the new TSEPs.

For information, the estimated self-heating of the device is given for different test conditions:
- 5.0°C if V_{GE}=15V, I_C=180A, ambient temperature 40°C,
- 6.5°C if V_{GE}=12V, I_C=180A, ambient temperature 40°C,
- 6°C if V_{GE}=15V, I_C=180A, ambient temperature 160°C,
- 7.5°C if V_{GE}=12V, I_C=180A, ambient temperature 160°C.

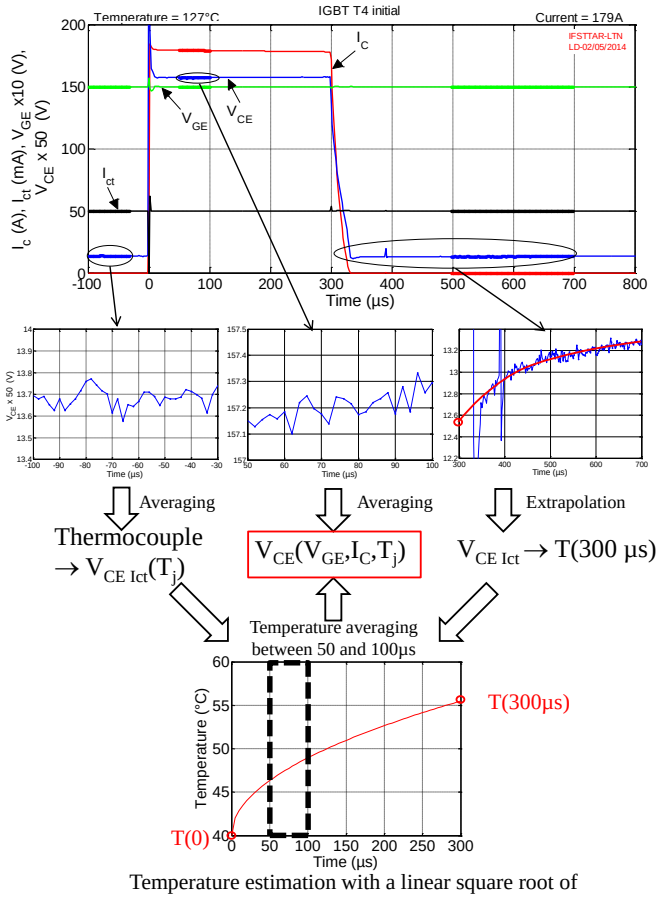


Figure 5. Principle of the the $V_{CE}(V_{GE},I_C,Tj)$ measurements to characterize the TSEPs

In the following paragraph, three TSEPs will be characterized: V_{CE_Ic} (the forward voltage) and those presented in section II ($\Delta V_{CE\_\Delta VGE}$ and V_0).

B. Characterization of V_{CE_Ic}

This first TSEP is directly obtained from the electrical measurements made during the current pulses. Its characterization consists of the measurement of the forward voltage V_{CE} for a given I_C and a given V_{GE}. Fig. 6 shows that its sensitivity is extremely dependent on the current value. When V_{GE}=15V, this sensitivity is in the range from -1mV/°C to +4mV/°C. It can be zero for intermediate current levels.

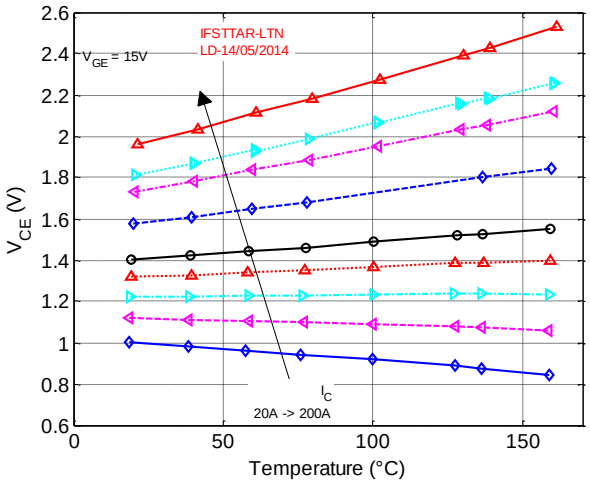


Figure 6. Characterization of V_{CE_Ic} with V_{GE}=15V

C. *Characterization of $\Delta V_{CE\_\Delta VGE}$*

The characterization results of $\Delta V_{CE\_\Delta VGE}$ are given for a V_{GE} voltage variation from 15V to 12V (Fig. 7). This result shows that the sensitivity of this TSEP increases with the current level. It is important to use this TSEP with V_{GE} levels higher than 12V to insure that the IGBT works in the saturation region for current levels up to 100A. However, the V_{GE} variation and the current have to be high enough to obtain sufficient sensitivities. When the current equals 90A and the V_{GE} variation is from 15V to 12V, the sensitivity is close to 2.5mV/°C for this IGBT chip.

D. *Characterization of V_0*

This TSEP is estimated using a linear regression of the forward characteristic of the semiconductor device. In the case of the power module presented here, the current level is in the range 30-120A (Fig. 8a). Fig. 8b shows the evolution of the TSEP as a function of temperature. In the temperature range, the sensitivity of V_0 is close to -1mV/°C when V_{GE}=15V.

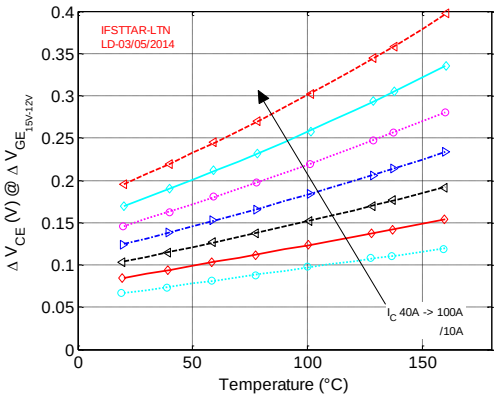
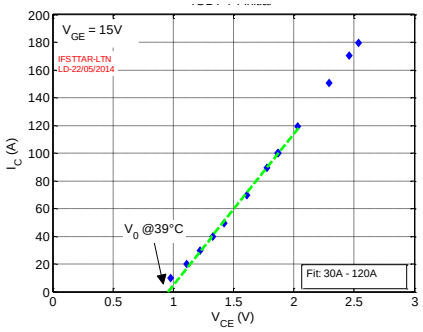
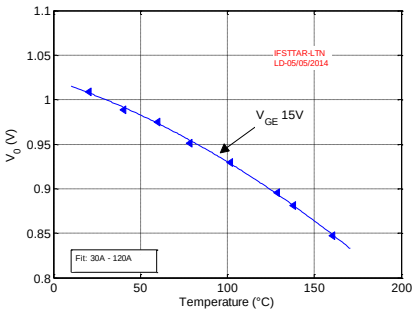


Figure 7. Characterization of $\Delta V_{CE\_\Delta VGE}$



a. Measurement principle



b. Characterization (V_{GE}=15V)

Figure 8. Evaluation of V_0

V. Temperature Measurements under Dissipation Conditions

A. Experimental conditions

Throughout the following tests, the input temperature of the fluid in the cold plate is 40°C. Five I_C values in the range 40-90A are used to change the stationary temperature of the chip. Three steps are made in sequence for each temperature measurement using the different TSEPs:

-Step #1: injection of the DC current to increase the temperature of the IGBT die being tested with V_{GE}=15V.

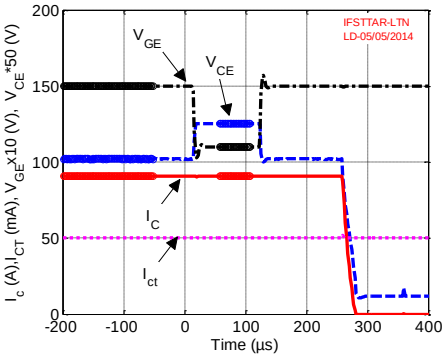
-Step #2: modification of the conduction conditions (variation of V_{GE} or of I_C) over a short period.

-Step #3: cancellation of the power current I_{p1} and estimation of the junction temperature T_{jv} using $V_{CE\ Ict}$ as TSEP.

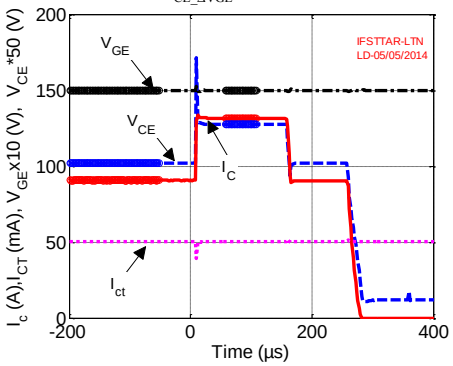
Fig. 9a and 9b respectively present the sequence which is carried out to measure the chip temperature using $\Delta V_{CE\_\Delta VGE}$ and V_0 as TSEPs. In the first case, V_{GE} varies from 15V to 11V during step #2 and, in the second, I_C increases from 90 to 130 A. The duration of the V_{CE} measurement is close to 100µs.

The chip temperature is also estimated using the IR camera with a numerical reconstruction as presented in Section III. The IR images are processed to extract the mean (T_{IR_mean}), minimum (T_{IR_min}) and maximum (T_{IR_max}) temperatures of the chip surface. It should be noted that the difference between the maximal and minimal values can reach 38°C when I_C equals 90A. All these values are compared to the junction temperature T_{vj} given by $V_{CE\ Ict}$ and by the other TSEP. As will be shown in the following paragraphs, and as was indeed expected, the temperature values obtained using $V_{CE\ Ict}$ are close to the mean temperatures of the chip surface. In fact, the difference remains smaller than 5°C.

Temperature measurements using the forward voltage as TSEP (V_{CE_Ic}) and using the new TSEP will now be presented.



a. $\Delta V_{CE\_\Delta VGE}$ 15V / 11V



c. V_0 90A / 130A

Figure 9. Electrical measurements to estimate the chip temperature using $\Delta V_{CE\_\Delta VGE}$ and V_0

B. Temperature measurements using V_{CE_Ic}

This TSEP is measured at the end of step #1, i.e. when the temperature of the device is stationary. Table I compares the temperature given by V_{CE_Ic} with the temperature given by $V_{CE\ Ict}$ and with the mean, minimal and maximal temperatures obtained by IR measurements. The gate-emitter voltage equals 15V for these measurements.

Table I shows that the TSEP gives chip temperature measurements which are always lower than the mean temperature. Using this TSEP to measure chip temperature is hazardous because the results are conform neither to the mean, nor to the minimal or maximal temperatures. As explained in Section II, this issue could be due to the resistive contribution of the electrical connections, including the bonded wires.

C. Temperature measurements using $\Delta V_{CE\_\Delta VGE}$

Table I presents the chip temperature measurements obtained using $\Delta V_{CE\_\Delta VGE}$ as a TSEP. A compromise is necessary so as to have both sufficient sensitivity and a high collector current for carrying out measurements. Here, this compromise consists of choosing a V_{GE} variation from 15V to 12V.

Excluding the measurement carried out with I_C=40A, this TSEP gives a temperature which is lower than the mean temperature of the chip with a difference between 1°C and 6°C in the used collector current range. It also shows a good correlation with the temperature obtained by using V_{CE_Ict}, with temperature differences being smaller than 10°C.

The results obtained with 40A could be explained by the device's low sensitivity to lower currents (Fig. 7).

D. Temperature measurements using V_0

Table I presents the chip temperature measurements obtained using V_0 as TSEP. For these measurements, the linear regression to obtain V_0 was carried out using 6 current values: I_C, I_C+10A, I_C+20A, I_C+30A, I_C+40A and I_C+50A.

Excluding the measurements carried out with I_C=40A, this TSEP gives temperature values very close to the maximum temperature of the chip with a maximum difference remains smaller than 4°C. The bad result obtained with 40A can be explained because the linear regression is not made in the linear part of the curve.

As a first conclusion, the TSEPs proposed in this paper provide accurate temperature measurements when the current level is sufficient. $\Delta V_{CE\_\Delta VGE}$ gives results close to the mean temperature of the chip, and V_0 provides results close to the maximal temperature. These results also show that the chip temperatures obtained with the forward voltage (V_{CE_Ic}) are hazardous. The following section will examine the influence of the damage of the wire bonding on the chip temperature estimation by TSEPs.

VI. Influence of the Power Module Ageing

A. Methodology

The principle retained to partially estimate the robustness of TSEPs is to operate a mechanical degradation of the wire bonding that ensures the electrical connections with the IGBT emitter surface. Fig. 10 presents a picture of this degradation, which was realized by cutting two wires in order to reproduce the impact of wire bonding damages that can occur in applicative conditions (I_C=90A).

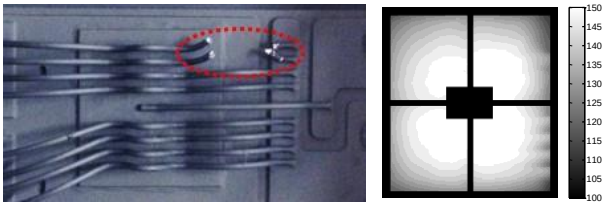


Figure 10. Electrical connections degradation of the IGBT by cutting 2 of 8 wire bondings, and infrared temperature measurement in dissipation mode (I_C=90A)

This degradation leads to a modification of the direct characteristics of the power IGBT component. The extraction of the characteristic I_C (V_{CE}, V_{GE}) is realized for a cooling temperature at 40°C. As shown in Fig. 11, the voltage drop V_{CE}, measured for the same current I_C and the voltage V_{GE}, is then increased by 2% for a current I_C=90A.

B. Temperature measurements in dissipation conditions

The modification of the number of electrical connections leads to a significant rise in the temperature of the wire bondings which have to conduct the currents from the corresponding active zones of the IGBT. Table II details the average of the results obtained for every current level I_C during the campaign in dissipation mode. It compares the measurements realized with the TSEP V_{CE_Ict} and the values calculated from the infrared measurements.

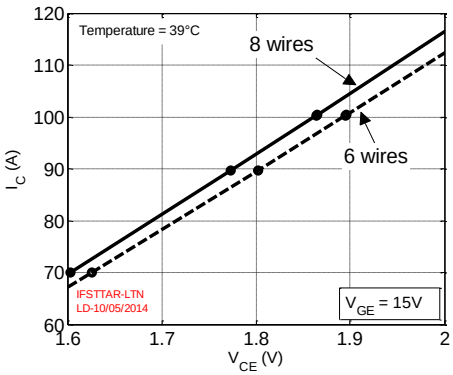


Figure 11. Impact of the electric connections degradation on the characteristics I_C (V_{CE}, V_{GE}) of the transistor IGBT T_4 at 40°C

To estimate the temperature of the degraded component, the TSEP V_{CE_Ic} is configured as previously, with V_{GE} equal to 15V. Table II presents a synthesis of the results by presenting a comparison between the measurements realized with TSEP $V_{CE\ Ict}$, the infrared values and those obtained with TSEP V_{CE_Ic}.

TABLE I.
COMPARATIVE EVALUATION OF V_{CE_Ic}, $\Delta V_{CE\ \Delta VGE}$, ΔV_0 AS TSEP

I_C (A)	T_{IR_mean} (°C)	T_{IR_min} (°C)	T_{IR_max} (°C)	$T_{jv\_Vce\_Ict}$ (°C)	V_{CE_Ic} (V)	$T_{jv\ VCE\_Ic}$ (°C)	$T_{jv\ VCE\_Ict}$ (°C)	$\Delta V_{CE\_\Delta VGE}$ (V)	$T_{jv\ \Delta VCE\ \Delta VGE\ 15V\text{-}12V}$ (°C)	$T_{jv\_Vce\_Ict}$ (°C)	V_0 (V)	$T_{jv\ V0}$ (°C)
	Common for all TSEPs											
40	66.8	59.3	70.2	69.7	1.328	32.5	68.1	0.082	58.9	67.9	0.932	64.9
60	88.4	74.9	94.4	90.5	1.573	71.7	91.4	0.143	87.4	90.9	0.940	98.3
70	102.1	84.6	109.8	105.1	1.711	88.7	104.9	0.184	99.5	105.7	0.936	107.7
80	118.3	96.3	127.8	121.7	1.864	106.7	121.8	0.235	113.7	122.1	0.927	129.6
90	137.8	111.1	149.6	141.6	2.039	127.2	141.8	0.302	132.0	142.3	0.898	151.3

The indirect measurements obtained with the TSEP V_{CE_Ic} are closer to the average value because of the increase of the voltage drop V_{CE} induced by the degradation of the electric connections. This understandable drift is due to this particular TSEP's characteristic. Considering this result, the TSEP V_{CE_Ic} does not satisfy the robustness requirement in the case of an electric connections degradation.

However, these results confirm the good correlation between the estimations of the temperature realized with TSEP V_{CE_Ict} and the extraction of the average value from the infrared measurements. The gaps remain strictly smaller than 3°C for all power dissipation conditions. These results demonstrate the robustness of this indicator, which makes it possible to estimate the average temperature in spite of a wire bonding degradation.

To estimate the component temperature with the degradation, the TSEP $\Delta V_{CE\_\Delta VGE}$ is configured as previously in §V.C, with a variation of V_{GE} from 15V to 12V. Table II presents a comparison between the measurements realized with TSEP V_{CE_Ict}, the infrared values and those obtained with the TSEP $\Delta V_{CE\_\Delta VGE}$ under the same conditions as previously detailed in §V.C.

As was the case with the temperature measurements taken on the component before degradation, a current of 40A does not allow satisfactory indirect measurements with the TSEP $\Delta V_{CE\_\Delta VGE}$. On the other hand, the results obtained for the higher current levels are also correct, both with and without degradation of the electric connections. The gaps between the average temperatures and the temperatures given by TSEP $\Delta V_{CE\_\Delta VGE}$ remain strictly smaller than 5°C. These results seem to confirm the robustness of this TSEP to the ohmic contribution which characterizes the voltage drop V_{CE}, including the electrical connections of the transistor (V_{CE}+2%).

Table II presents the results obtained with the TSEP V_0 extracted under the conditions previously detailed in §V.D. The differences between the temperature evaluation with the TSEP V_0 and the infrared measurements show a good correlation with the maximal temperature estimated by infrared measurements, as was the case without degradation. While this TSEP is of limited usefulness in the case of a low current level (I_C=40A), the results obtained for higher current levels I_C, between 60A and 90A, are satisfactory. A slight degradation of the relevance of this TSEP is observed. Nonetheless, the difference between the TSEP V_0 measurements and the maximal temperatures estimated with the infrared camera remains strictly smaller than 5.5°C.

VII. SYNTHESIS

To have a synthetic and qualitative view of the results presented in the tables, Fig. 12 presents the evolution of the estimated temperatures corresponding to each TSEP as a function of the collector current for safe and degraded devices. In each case, the temperature given by the TSEP is compared with the temperatures given by IR measurements.

This figure shows that V_{CE_Ict} gives temperature measurements between the mean and maximum temperatures as it was already demonstrated in [9,19-20]. This TSEP is weakly influenced by the degradation because the difference between mean and TSEP temperatures decreases slightly (<2°C) when two bond wires are cut. V_{CE_Ic} gives temperatures which are dependent on the degradation. On the contrary, temperatures given by $\Delta V_{CE\_\Delta VGE}$ and V_0 depend weakly and on the aging of the bondwires. They are therefore better

candidates for on-line chip temperature measurements than V_{CE_Ic}. However, the calibration and/or measurement of V_0 should be improved to obtain more accurate results.

TABLE II.
EVALUATION OF TSEP V_{CE_IC} (WITH DEGRADATION)

I_C (A)	T_{IR_mean} (°C)	T_{IR_min} (°C)	T_{IR_max} (°C)	$T_{jv\_Vce\_Ict}$ (°C)	V_{CE_Ic} (V)	$T_{jv\ VCE\_Ic}$ (°C)	$T_{jv\ VCE\_Ict}$ (°C)	$\Delta V_{CE\_\Delta VGE}$ (V)	$T_{jv\ \Delta VCE\ \Delta VGE\ 15V\text{-}12V}$ (°C)	$T_{jv\_Vce\_Ict}$ (°C)	V_0 (V)	$T_{jv\ V0}$ (°C)
	Common for all TSEPs											
40	67.6	59.7	70.8	67.7	1.340	50.8	67.1	0.083	60.3	68.0	0.931	65.9
60	90.2	76.1	96.0	90.8	1.593	84.8	91.2	0.145	89.7	92.0	0.938	100.5
70	104.4	86.3	111.8	106.1	1.736	101.3	105.7	0.186	103.1	106.6	0.932	111.3
80	121.2	97.4	130.7	122.7	1.896	119.4	124.4	0.239	117.8	123.5	0.919	136.2
90	141.3	111.1	153.1	144.1	2.079	140.9	143.9	0.308	137.2	144.1	0.893	155.2

VIII. CONCLUSION

This research evaluating new TSEPs adapted for use in functional conditions is based on an experimental confrontation with various means of temperature measurements. The means implemented made it possible to compare the temperature measurements obtained by the new TSEPs with an indirect measure (TSEP V_{CE_Ict}) and with infrared camera measurements, by integrating the phenomenon of self-heating during the phase of characterization. The results obtained for IGBTs show that both proposed TSEPs make it possible to follow the temperature of the power component with an error lower than 10°C in the worst case.

This article has shown that the use of the on bias voltage as TSEP was not ideal and remained influenced by the degradation of the wire bonding. In contrast, it seems that TSEP $\Delta V_{CE\_\Delta VGE}$ slightly underestimates the average temperature (difference lower than 6°C) and that TSEP V_0 gives a temperature value close to the maximal component temperature both without and after degradation of the electrical connections. A modeling approach will make it possible to understand more exactly the nature and the representativeness of the temperatures obtained with these various TSEPs. However, these TSEPs have not yet been definitively validated. It is important to improve the precision of the temperature estimations by increasing the number of test points during the TSEP characterization. It will also be necessary to complete this study on the influence that component damages have on the temperature measurements obtained by these new TSEPs. Our next research projects will focus on the effect of thermal assembly damages and the ageing of the gate oxide.

To confirm these first results, it will be necessary to carry out the same measurements using other devices: IGBT with the same reference to carry out statistical analyses and, then different ones to know if these TSEPs can be applied with all IGBT technologies. It will be also essential to set up a test mean that makes it possible to use components in functional conditions. We will then estimate more precisely how relevant these TSEPs are when confronted with the difficulties inherent in being used in this more complex environment. However, these first results are encouraging and allow us in particular to envisage the use of these TSEPs for estimating the integrity of the power modules in a converter. On this point, it is interesting to note that certain authors have already presented methods based on the direct on-bias to monitor the health of power converters [23]. We will be able to confront the results of our future projects with this body of research.

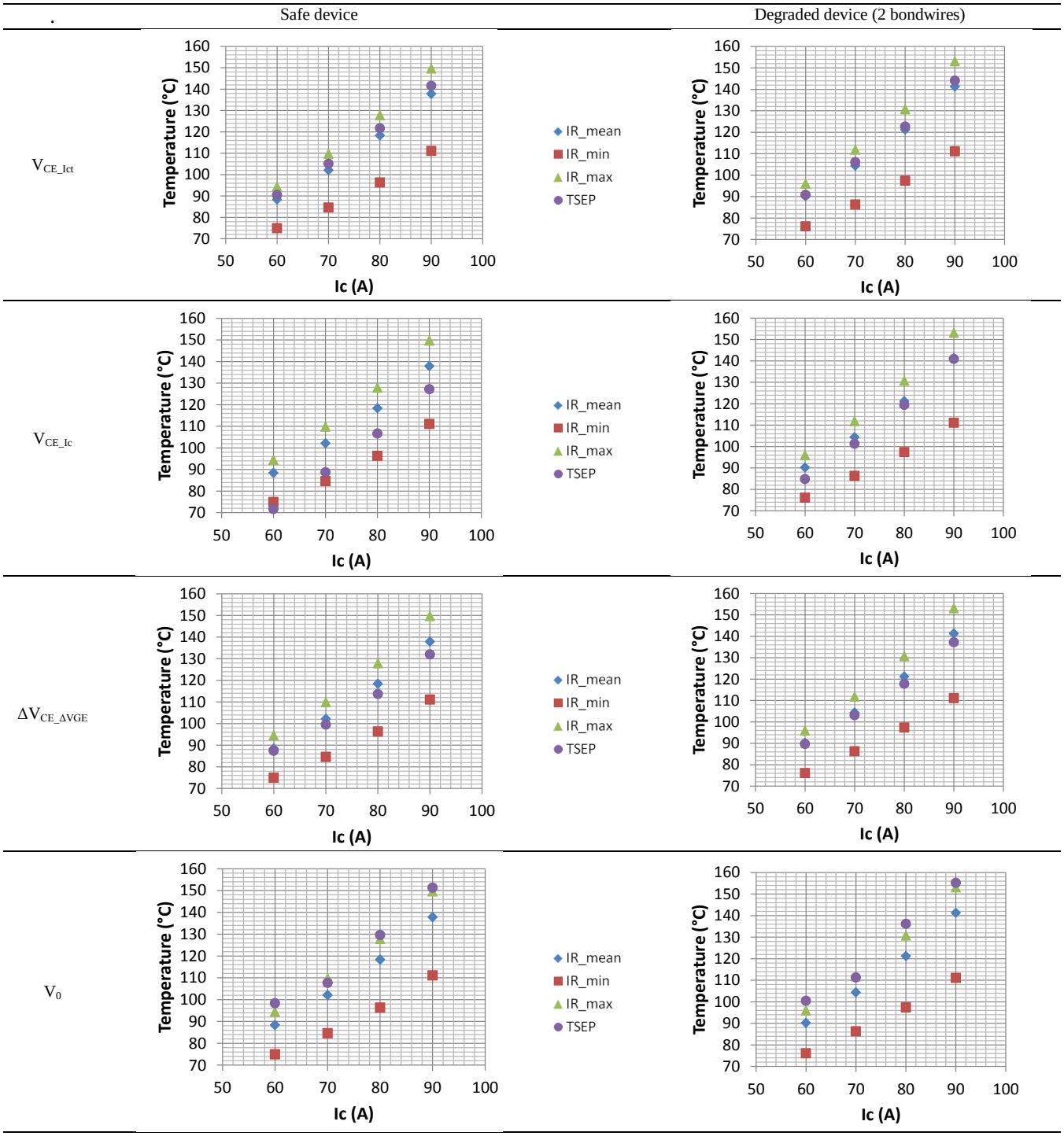


Figure 12. Evolution of the temperature for the different TSEPs as a function of the collector current

ACKNOWLEDGMENT

The authors thank the French National Research Agency (MEMPHIS ANR-13-PRGE-0005-01 PROGELEC project) and the GdR SEEDS for the grants allocated for this research topic.

REFERENCES

[1] M. Ciappa, "Selected failure mechanisms of modern power modules", Microelectronics Reliability, vol. 42, no. 4-5, pp. 653-667, 2002.

[2] M. P. Rodriguez, N. Y. A. Shammas, A. T. Plumpton, D. Newcombe, and D. E. Crees, "Static and dynamic finite element modelling of thermal fatigue effects in insulated gate bipolar transistor modules", Microelectronics Reliability , vol. 40, pp. 455-463, 2000.

[3] D-L. Blackburn, "Temperature measurements of semiconductor devices - A review", 20th Annual Semiconductor Thermal Measurement and Management Symposium, pp. 70-80, 2004.

[4] V. Smet, "Aging and failure modes of IGBT power modules undergoing power cycling in high temperature environments", PhD Thesis, Montpellier 2 University, France, 2010.

[5] X. Perpiñà, J.F. Serviere, J. Saiz, D. Barlini, M. Mermet-Guyennet, J. Millán, "Temperature measurement on series resistance and devices in power packs based on on-state voltage drop monitoring at high current", Microelectron. Reliabil., vol 46, pp. 1834-1839, 2006.

[6] H. Kuhn and A. Mertens, "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters," in Proc. 13th Eur. Conf. Power Electron. Appl., Barcelona, Spain, Sep. 8–10, 2009, pp. 1–10.

[7] D.C. Katsis, J.D. Van Wyk, "Void-induced thermal impedance in power semiconductor modules: some transient temperature effects", IEEE Trans. Ind. Appl., vol.39, no.5, pp. 1239- 1246, Sept/Oct 2003.

[8] E-R. Motto, J-F. Donlon, "IGBT module with user accessible on-chip current and temperature sensors", 2012 27th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1-6.

[9] R. Schmidt, U. Scheuermann, "Using the chip as a temperature sensor - The influence of steep lateral temperature gradients on the Vce(T)-measurement", 13th Europ. Conf. on Power Electronics and App., 2009.

[10] N. Baker, M. Liserre, L. Dupont, Y. Avenas, "Improved Reliability of Power Modules: A Review of Online Junction Temperature Measurement Methods," IEEE Industrial Electronics Magazine, vol.8, no.3, pp.17-27, 2014

[11] V. Sundaramoorthy, E. Bianda, R. Bloch, I. Nistor, G. Knapp, A. Heinemann, "Online estimation of IGBT junction temperature (Tj) using gate-emitter voltage (Vge) at turn-off," 15th European Conference on Power Electronics and Applications (EPE), pp.1-10, 2013.

[12] I. Bahun, N. Cˇobanov, Ž. Jakopovic, "Real-time measurement of IGBT's operating temperature", AUTOMATIKA, vol. 52, no 4, pp. 295–305, 2011.

[13] V. Sundaramoorthy, E. Bianda, R. Bloch, F. Zurfluh, "Simultaneous online estimation of junction temperature and current of IGBTs using emitter-auxiliary emitter parasitic inductance," PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp.1-8, 2014.

[14] P. Sun, H. Luo, D. Yufei, W. Li, X. He, G. Chen, E. Yang, Z. Dong, "Online junction temperature extraction with turn-off delay time for high power IGBTs", 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp.4016-4021, 14-18 Sept. 2014.

[15] H. Luo, P. Sun, Y. Dong, W. Li, X. He, G. Chen, E. Yang, Z. Dong, "P-i-N diode chip temperature extraction method by investigation into maximum recovery current rate di/dt", 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp.4022-4024, 14-18 Sept. 2014.

[16] M. Denk, M-M. Bakran, "An IGBT Driver Concept with Integrated Real-Time Junction Temperature Measurement," Proceedings of PCIM Europe 2014, pp.1,8, 20-22 May 2014.

[17] N. Baker, S. Munk-Nielsen, M. Liserre, F. Iannuzzo, "Online junction temperature measurement via internal gate resistance during turn-on", 2014 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe), pp.1-10, 26-28 Aug. 2014.

[18] M. Musallam, C-M. Johnson, "Real-Time Compact Thermal Models for Health Management of Power Electronics", IEEE Transactions on Power Electronics, vol.25, no.6, pp.1416-1425, 2010.

[19] Y. Avenas, L. Dupont, "Evaluation of IGBT thermo-sensitive electrical parameters under different dissipation conditions - Comparison with infrared measurements", Microelectronics Reliability, Vol. 52, no 11, pp. 2617–2626, 2012.

[20] L. Dupont, Y. Avenas, P-O Jannin, "Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermo-sensitive electrical parameters", IEEE Transactions on Industry Applications, Vol. 49, Issue 4, April 2013.

[21] D.L Blackburn, "A Review of Thermal Characterization of Power Transistors", 4th Annual IEEE Semiconductor Thermal and Temperature Measurement Symposium, Semi-Therm, 1988, p. 1-7.

[22] B. Thollin, L. Dupont, Z. Khatir, Y. Avenas, J-C. Crebier, P-O. Jeannin, "Partial thermal impedance measurement for die interconnection characterization by a microsecond "pulsed heating curve technique"," 15th European Conference on Power Electronics and Applications (EPE), pp.1-10, 2013

[23] M-A. Eleffendi, C-M. Johnson, "Thermal path integrity monitoring for IGBT power electronics modules", 8th International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg, Germany, pp.1-7, 2014.

.