

# Electrothermal evaluation of single and multiple solder void effects on low-voltage Si MOSFET behavior in forward bias conditions

Son Ha Tran, Laurent Dupont, Zoubir Khatir

▶ **To cite this version:**

Son Ha Tran, Laurent Dupont, Zoubir Khatir. Electrothermal evaluation of single and multiple solder void effects on low-voltage Si MOSFET behavior in forward bias conditions. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 99, 10.1109/TCPMT.2016.2633582 . hal-01466016

**HAL Id: hal-01466016**
**https://hal.science/hal-01466016**

Submitted on 13 Feb 2017

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

*Accepted by IEEE for publication in 2016 :*
*TRAN, Son Ha, DUPONT, Laurent, KHATIR, Zoubir, 2017, Electrothermal evaluation of single and multiple solder void effects on low-voltage Si MOSFET behavior in forward bias conditions, IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY, Institute of Electrical and Electronics Engineers - IEEE, 9p, DOI: 10.1109/TCPMT.2016.2633582*


# Electrothermal evaluation of single and multiple solder void effects on low-voltage Si MOSFET behavior in forward bias conditions

S.H. Tran, L. Dupont, Z. Khatir *IEEE Member*

***Abstract*—Solder void thermal effects on power module performance and reliability were investigated long time ago. The final goal is to determine void acceptability criteria or to remove them. Our approach is not to offer a more efficient method for neglecting void formation, but to suggest a method for optimizing void thresholding from multiphysical viewpoint. The major achievement is in the complete combination of modeling, experiments and optimization for void effect evaluation purpose. Especially, it has been introduced for the first time a real new highly coupled and detailed 3D-FEM electrothermal model of low-voltage silicon MOSFET and the bonding wires in steady state.**

**For single void case, the simulation results highlight local void effects on thermal performance of MOSFET in void area. However, no significant consequence on electrical performance is observed. Besides, the model shows a high dependence between void effects and back side metallization parameters. Electrical and thermal measurements performed on various single void configurations of experimental MOSFET prototypes offer a good agreement with numerical results. The study is then expanded to multi-voids case. The criticality of multi-voids corresponds to that of the most critical single void if the voids are not coalesced. These results offer an idea for a more optimized void inspection method in production line.**

***Index Terms*—Electrothermal modeling, low-voltage MOSFET, die attach, solder, void.**

## I. Introduction

In current applications, power module is required to operate under harsh conditions (high temperature, vibration, electrical stress…). Moreover, it is designed to meet performance, reliability and design-to-cost requirement. Especially in automotive applications, low-voltage MOSFETs are widely used due to the battery voltage level. In power module design, these devices are connected to a substrate by a solder layer. This die attach, undergoing high current densities and thermal fluxes, is one of the most crucial elements in power packaging [1]. During the assembly process, void can be formed due to trapped gas during the reaction of materials in the course of the die attachment, clean-up agent residues (fluxes), poor wettability at the joining interfaces [2] or the imperfections of the reflow process [3]. For short, we consider only solder voids in the die attach layer, whose impacts on electrothermal behavior are more important than those located in the layer between the baseplate and the leadframe as in conventional design. Void, existing under a form of bubble gas, reduces locally electrical and thermal performances. A well-known consequence of their disturbance is the formation of hot spots, causing degradation of device performance and others consequences (early ageing or destruction) [4]. Void concerns are intensified by the RoHS directive (Restriction of Hazardous Substances) which prohibits the use of lead (Pb) in some electronic and electric tools. Lead-free solders wettability is generally poorer than that of classical Pb-solders [5]. It can be noticed that it exists several methods allowing to reduce void rate such as vacuum soldering, sintering. Nevertheless, their slower process (about dozens of minutes) and high cost [6] are the most remarkable drawbacks in comparison to conventional soldering. In the present study, the power modules are issued from mass production line. The die attach is achieved from laser soldering due to cost-effective requirement in automotive applications. As a consequence, void rate has to be maintained under an acceptable level. In microelectronics field, the standards MIL-STD-883G and IPC-7095 [7-8] are recommended for void inspection. Nevertheless, no standard in power electronics field suggests void acceptability levels. For a given technology in power application, an empiric level of 5% is generally used [9-10]. In reality, the void criteria levels are much more complicated to determine because they vary with void characteristics such as geometry, position, distribution [11-16]. It becomes crucial to optimize void thresholding in taking into account the electrothermal couplings.

The previous studies introduced thermal modeling in which the power dissipated in the chip is defined by a homogenous surface or a volume heat source [11-16]. In reality, the device behavior in its surrounding environment is a complex thermal, electrical and mechanical coupling phenomena, and requires multi-physics modeling. Such an electrothermal model was introduced in [17-18]. To our knowledge, no distributed

S. H. Tran is with the Carbon-free, Communicating Vehicle and its Mobility Institute (VEDECOM), 77 rue des Chantiers, 78000 Versailles and the French Institute of Sciences and Technology for Transport, Development and Networks (IFSTTAR), 25 allée des Marronniers, 78000Versailles (phone: (+33) (0)1 30 84 39 85; e-mail: son-ha.tran@ ifsttar.fr).

L. Dupont and Z. Khatir are with the French Institute of Sciences and Technology for Transport, Development and Networks (IFSTTAR) in the laboratory of Systems & Applications of Information & Energy Technologies (SATIE), 25 allée des Marronniers, 78000 Versailles (e-mail: laurent.dupont@ifsttar.fr; zoubir.khatir@ifsttar.fr)

electrothermal model has been developed for void effects evaluation purpose, except for a simplified analytical model [19-20]. It is also noted that the electrical connections were mostly simplified. From electrothermal viewpoint, power bonding wires need to be taken into account especially in low-voltage applications. Indeed, their power loss can't be neglected in comparison with that of the component. In addition, bond-wire configuration plays a role on the current distribution in power device which is sensitive to the temperature.

This paper describes a finite element model allowing to take into account the electrothermal couplings at the active part layer of the low-voltage silicon MOSFET and the bonding wires in steady state. The major issue when attempting to obtain the finite elements modelling of the power module is the scale difference between the thickness of layers of the chip (micrometer) and its dimensions (centimeter). In our model, thin layers will be fine-meshed but for reasonable calculation time (approximately 20 minutes per simulation). Electrical and thermal disturbances due to void effects are observed at different layers of the system. The model validation is ensured by electrical and thermal measurements carried on experimental MOSFET prototypes in which intended single and double voids are generated at various positions and sizes in the die attach. The results will be used for discussing multiple voids case.

## II. Realization of Experimental Prototypes with Controlled Solder Voids

For validation purpose, we realized MOSFET prototypes so that position and size of solder voids are controlled. The operation process is illustrated in Fig. 1. We drill approximately 100µm-thick holes on a copper baseplate surface, corresponding to the intended voids (a), then drop a low quantity of gel beside (b). The solder area is delimited by laser where a SAC solder preform ($SnAg_{3.35}Cu_{0.7}Sb_{0.3}$) is placed before the MOSFET (24V–500A).

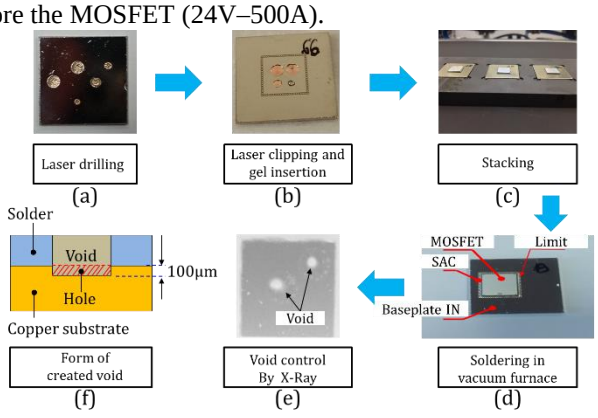



Fig. 1. Generation of controlled voids in the die attach

This method improves the homogeneity of solder thickness. Once the stacking is done (c), the soldering is activated in a vacuum furnace (d). Vacuum conditions ensure that only a negligible amount of parasitic voids will be formed. Void is then evaluated by 2D X-Ray tomography (e) before the final step of the assembly process begins. This method offers a good efficiency for both single and multiple voids creation, with a success rate higher than 90%. However, the created voids locate not only in die attach layer but also in the copper baseplate because of the holes (f – crosshatching area). This problem can provoke supplementary impacts beside those of solder voids and need to be checked. A simulation in which we compared solder void with and without hole in copper substrate, has confirmed that no significant effect arises from our method. This observation is consistent with the results of Chen [2].

To finish the assembly, the baseplate "IN" is pressed on an anodized aluminum lead-frame through a graphite thermal interface TIM1 (Fig.2 and Fig.3a). Eight bonding wires connect electrically the MOSFET source to the baseplate "OUT". This one is also attached to the lead-frame by using a high-temperature thermal paste. Once assembled, the prototype is fixed in the test bench. The lead-frame is attached to an aluminum plate by using a fiberglass thermal interface TIM2 (Fig.3b). Then the leadframe is itself placed on a cooling device by inserting another graphite thermal interface TIM3. Finally, for electrical control and measurement purpose, six 125µm-diameter-bonding-wires associate the source, gate and drain of the MOSFET to a connector fixed to the lead-frame by an isolated thermal paste. They ensure the gate-source control voltage and allow to access the drop voltage of MOSFET ($V_{DS1}$,$V_{DS2}$) and power bonding wires ($V_{S2S3}$) from which we extract electrical properties for electrothermal couplings.

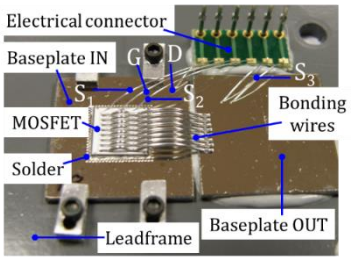



Fig. 2. Experimental MOSFET prototype

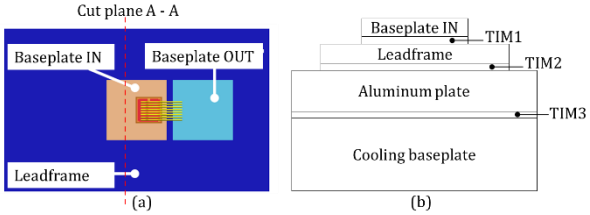



Fig. 3. Schema of the prototype assembly on the leadframe (a) and on the cooling baseplate (b)

## III. Electrothermal Modeling

### A. *Description of the finite element model*

The finite element analysis tool used to model the prototype is COMSOL Multiphysics™. It is representative to the experimental one. The different layers of the model respect the drawing shown in Fig. 3.

The low-voltage MOSFET is modeled as a rectangular parallelepiped of 8mm x 8mm x 249µm. The area of the MOSFET is divided into two main parts for a more realistic representation of the physical phenomena in different subdomains (Fig. 4):

- An active area (in red) in which heat is dissipated, occupies 89% of the total surface of the die

- An inactive area (in orange) in which no current flows, gathering the MOSFET gate, four reference sights, guard rings, fills 11% of the total surface of the die

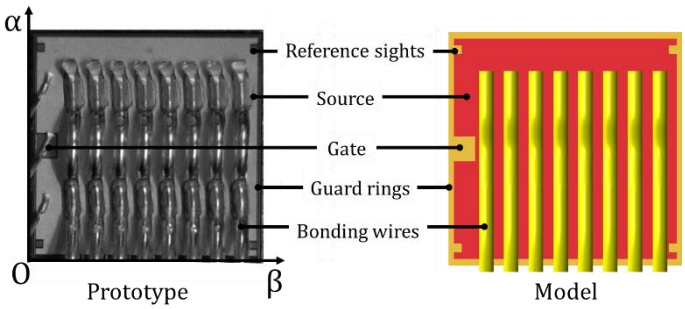



Fig. 4. Active and inactive areas of the MOSFET

The active domain of the MOSFET is discretized into four layers, based on the distribution of the on-state resistance $R_{DS}(on)$ (Fig. 5):

- Two Al-metallized layers corresponding to the MOSFET source and drain, they are 10µm and 1µm-thick respectively
- An active layer, gathering the channel, accumulation, JFET, N- epitaxy regions. This 10µm-thick volume is surrounded by guard rings
- A 228µm-thick layer, corresponding to the highly doped N+ substrate ($10^{19}cm^{-3}$)

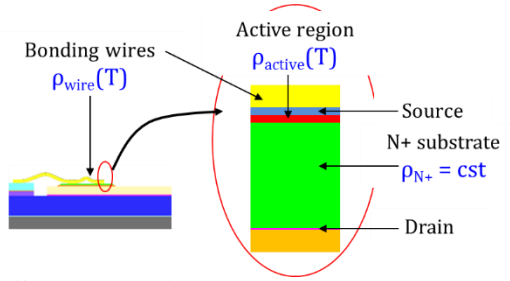



Fig. 5. Different domains of the used MOSFET

To evaluate void effects, two models are similarly built, except the presence or not of the void. In the void-model, each intended void is modeled as a cylindrical cavity over the entire height ($E_v$) of the solder layer. An example of a void with a diameter $T_v$ at position ($X_v$, $Y_v$) is shown in Fig. 6:

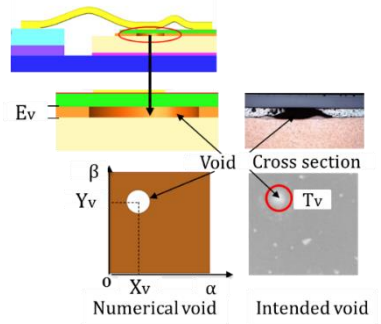



Fig. 6. Modeling of void

The dimensions of our model elements are summarized in Table I. The discretization of the MOSFET allows to consider a high chip–to–packaging scale factor, from micrometer scale of the MOSFET to decimeter scale of the cooling device.

TABLE I
DETAIL OF MODEL GEOMETRY

| **Constitutive layers** | **Dimensions** |
|---|---|
| MOSFET | 8mm x 8mm x 249µm |
| Solder | 8.7mm x 8.7mm x $E_v$ |
| Substrate IN | 20mm x 20mm x 1.2mm |
| TIM1 | 20mm x 20mm x 200µm |
| Lead-frame | 88mm x 54mm x 3mm |
| TIM2 | 88mm x 54mm x 130µm |
| Plate | 161mm x 110mm x 12mm |
| TIM3 | 161mm x 110mm x 130µm |
| Cooling device | 161mm x 110mm x 20mm |
| Thermal paste | 20mm x 20mm x 680µm |
| Substrate OUT | 20mm x 20mm x 1.2mm |

The material properties are issued from the literature or characterized by electrothermal measurements. The thermal properties of the model elements are constant while the electrical ones are determined from the following expression:

$$\rho = \rho_0 \times (1 + \alpha_T \times (T - T_0)) \quad (1)$$

Where $T$ is the temperature, $T_0$ is the reference temperature, $\rho$ and $\rho_0$ are the electrical resistivity at $T$ and $T_0$ respectively, $\alpha_T$ is the temperature-dependence coefficient. The temperatures are expressed in Kelvin. The material properties of the model elements are summarized in Table II:

TABLE II
MATERIAL PROPERTIES [21]

| **Packaging elements** | **Material** | **Density (kg/m³)** | **Specific heat (J/kg.K)** | **Thermal conductivity (W/mK)** | **Electrical Resistivity (Ωm)** | | |
|---|---|---|---|---|---|---|---|
| | | | | | **Reference resistivity (Ωm)** | **Temperature coefficient ($K^{-1}$)** | **Reference temperature (K)** |
| **Bonding wires** | Al | 2710 | 913 | 230 | **Characterizations I(V, Tj)** | | |
| **Source Gate MOSFET** | Al | 2700 | 910 | 200 | 4E-8 | 3.1E-3 | 400 |
| **Active Domain MOSFET** | Si | 2330 | 710 | 148 | **Characterizations I(V, Tj)** | | |
| **N+ area MOSFET** | Doped Si ($10^{19}cm^{-3}$) | 2330 | 710 | 148 | 1E-4 | 0 | 273 |
| **Solder** $SnAg_{3.35}Cu_{0.7}Sb_{0.3}$ | | 2320 | 7390 | 58.7 | 1.3E-7 | 0 | 273 |
| **Substrate IN + OUT** | Cu | 8960 | 380 | 390 | 3.2E-8 | 2.5E-3 | 500 |
| **TIM1** | Graphite | 1650 | 846 | $\lambda x = \lambda y = 400$ $\lambda z = 5/k_1$ | 7.8E-6 | 0 | 273 |
| **Lead frame** | Al | 2700 | 870 | 148 | 4E-8 | 3.1E-3 | 400 |
| **TIM2** | Fiberglass | 2500 | 736 | $1.6/k_2$ | 1E10 | 0 | 273 |
| **Plate** | Al | 2700 | 870 | 148 | 4E-8 | 0 | 273 |
| **TIM3** | Graphite | 1650 | 846 | $\lambda_x = \lambda_y = 400$ $\lambda_z = 20$ | 7.8E-6 | 0 | 273 |
| **Cooling device** | Al | 2700 | 1300 | 120 | 4E-8 | 0 | 273 |
| **Thermal paste** | Silicone polymer | 2710 | 700 | 1.9 | 1.9E-7 | 0 | 273 |
| **Drain MOSFET** | Ag | 1E4 | 232 | 429 | 1.47E-8 | 0 | 273 |
| **Guard rings** | Polyimide | 1420 | 1090 | 0,12 | 1.5E17 | 0 | 273 |

The Z-axis thermal conductivity of the thermal interfaces TIM1 and TIM2 may vary from one module to another depending on the surface geometries and contact conditions. They are respectively determined by the coefficients $k_1$ and $k_2$. The electrical resistivity of the N+ layer of the MOSFET is constant at its doping level and for temperature between 20°C and 200°C [22]. The electrical resistivity of the bonding wires as well as the active layer of the MOSFET are extracted from a static electrothermal characterizations I(V, $T_j$) performed on a dedicated test bench [23]. Each measurement of the MOSFET and power bonding drop voltage is done under pulse conditions during 200µs, for seven current levels between 5A and 200A, at seven temperature levels between 40°C and 160°C and for a gate-source voltage fixed at 15V.

At a fixed temperature, each characterization offers a linear I(V) curve from which we calculate the global on-state resistance $R_{DS}(on)$ of the MOSFET and the resistance $R_{wires}$ of the eight wires. These information allow to determine the resistivity of active layer of the MOSFET $\rho_{active}$ and that of the bonding wires $\rho_{wire}$ from Ohm's law at this temperature:

$$\rho_{active} = \frac{(R_{DS}(on) - R_{N+}) \times S_{active}}{e_{active}} \quad (2)$$

$$\rho_{wire} = \frac{8 \times R_{wires} \times S_{wire}}{l_{wire}} \quad (3)$$

where $R_{N+}$ is the resistance of the N+ substrate, $S_{active}$ the active area, $e_{active}$ the thickness of the active layer *and* $S_{wire}$, $l_{wire}$, the area cross-section and the length of the bonding wires respectively. The temperature-dependence of the MOSFET active layer resistivity and that of the bonding wires are expressed by linearized relationship similarly to (1). The measured resistivity relationship of the aluminum wires is compared to that issued from the literature [24] (Fig 7). These two laws of resistivity represent the electrothermal couplings that we take into account in our model.

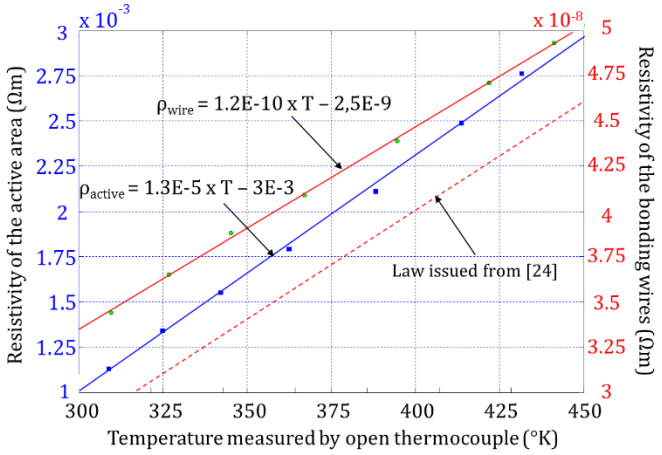



Fig. 7. Temperature-dependence of the resistivity of MOSFET active layer and this of the bonding wires

In the model, all solid volumes subjected to the current flow are considered as heat sources. The heat exchange by natural convection with ambient air (20°C) is represented by a heat transfer coefficient of 10 W/m²K applied to all outside surfaces. The convection at cooling face is taken into account by a heat transfer coefficient of 1000 W/m²K at the reference temperature of 80°C, applied to its lower surface. This convection represents the performances of the cooling system. For electric isolation boundaries, electrical discontinuities are applied at the following interfaces:

- Interface lead-frame - TIM1
- Interface lead-frame – thermal glue
- Interface active layer and inactive layer
- Interface substrate N+ and inactive layer

To represent forward bias conditions, a current level of 200A is applied to the lateral face of the baseplate IN and a ground is defined at the lateral face of the baseplate OUT (Fig. 8a).

Structured mesh is used for most of the domains except for the bonding wires where tetrahedral mesh is defined. In the void-model, the presence of void requires a hexahedral mesh, generated from quadrangle mesh at solder upper surface. For convergence problem, the fineness of this mesh is controlled by the number of elements ($M_{_void}$) at the void periphery (Fig. 8b). The model contains approximately 80000 mesh elements. Direct solver is chosen for calculation time and convergence reason. The model solves the electrothermal problem in about 20 minutes in a PC workstation.

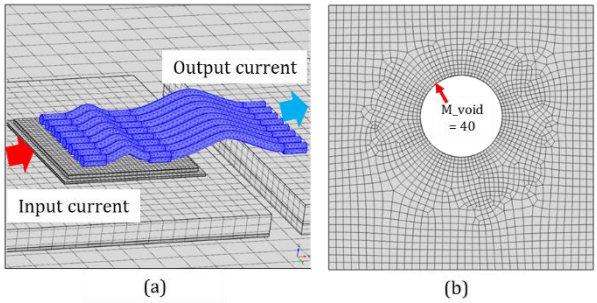



Fig. 8. Global mesh including bonding wires mesh (a) and solder mesh when $M_{_void}$ = 40 (b)

### B. *Simulation results*

The following section introduces the results obtained by both free-void and single-void models. Concerning the free-void one, the global temperature map is shown in Fig. 9, where it can be seen an inhomogeneous temperature distribution at MOSFET source and bonding wires level.

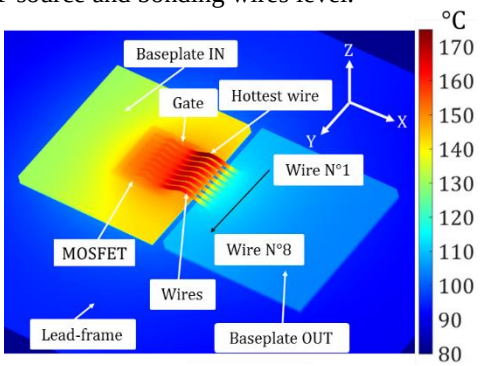



Fig. 9. Global temperature given by the free-void model

The temperature map obtained from numerical results at the top surface of the source metallization is illustrated in Fig. 10. In this figure, we can see the impact on the temperature distribution over the chip area of the Joule effect in the

wirebonds (10b) relatively to the configuration in which it is not taken into account (10c). The area near the chip center (Fig. 10b,c) is hotter because of the global electrothermal coupling. The cartography is slightly asymmetric because of the geometry of the MOSFET source. It is remarkable that the area underneath the bonding pads B (starting point of the big loop) is particularly hotter than that underneath the pads A (beginning of the small loop) (Fig. 10b). This observation can be explained by two phenomena. Firstly, it is a result of the current distribution in the source metallization which is higher under pads B than under pads A (Fig. 10a). Indeed, path B is shorter thus less resistive than path A. The resistivity of the area under the pads B is more important due to higher temperature but insufficient to modify the trend of the current distribution in top source metallization level. A second reason stems from the thermal diffusion from the hottest point C of the bonding wire towards the pad B. This is argued by an additional similar simulation in which self-heating of the bonding wires isn't taken into account (Fig. 10c). Obviously, the global temperature decreases. Moreover, we find out that the hottest area on the source metallization is no longer underneath the bonding pads but shifted to the chip centre. These results show that for power devices operating on steady state conditions, the bondwires may provide overheat to the power chip rather than cooling it. Furthermore, these phenomena can affect the impact of void due to the relative position between void and the hottest areas.

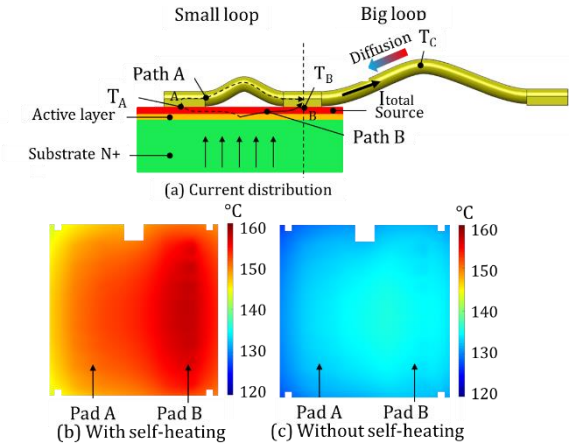



Fig. 10. Explanation of the temperature distribution at top source metallization of the MOSFET

Besides, we can see an inhomogeneous temperature distribution in the bonding wires (Fig. 11) as a result of a non-uniform current distribution (Table III). The first wire near the gate pad carries the largest part of the current and becomes the hottest wire. This observation can be mostly explained by the asymmetric location of the bonding wires on the MOSFET active surface.

TABLE III
CURRENT DISTRIBUTION IN BONDING WIRES

| Wire N° | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| $\frac{I_{fil}}{I_{total}}$ (%) $I_{wire}/I_{total}$ (%) | 13.7 | 12.9 | 12.5 | 12.2 | 12.1 | 12.1 | 12.2 | 12.5 |

We evaluate now the impact of single void positioned near the chip center by numerical simulation. The considered void is characterized by its spatial position in the chip ($X_v$, $Y_v$) = (3.8mm, 4.0mm), its diameter ($T_v$ =2.5mm) and solder thickness ($E_v$ = 246µm). The thermal conductivity of TIM1 and TIM2 is characterized by ($k_1$, $k_2$) = (8, 17.5). Figure 11 shows the impact of such a single void on the temperature map on the model relatively to the free-void case. Respectively to this figure, the thermal impact is clearly limited to void location.

For quantification purpose, void thermal effect (Fig 11c) is assessed by taking the MOSFET source surface temperature along the profile V-V crossing the void centre compared to the same profile in free-void model. We can see that a hot spot appears locally above the void area while little temperature change is observed elsewhere. The highest difference due to this 2.5mm-diameter void is approximately 7°C. The creation of this hot spot is explained by a thermal resistance rise issued from the poor thermal conductivity of the void. The same phenomenon is observed for the void effect on wire bonding temperature. However from quantitative viewpoint, void impact on bonding wires is clearly less significant than that on the MOSFET temperature.

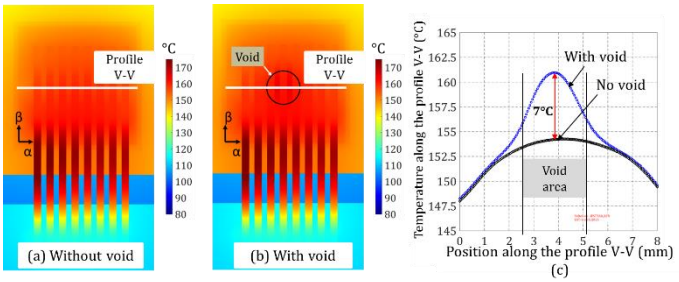



Fig. 11. Void effect on the temperature at MOSFET source metallization

The effect of void on current distribution is analysed at the different layers of the MOSFET. After reaching the area underneath the void, the current is forced to flow in lateral direction in the solder close to the void. Then, the current tends to concentrate in the region above the void after achieving the drain layer (Fig. 12).

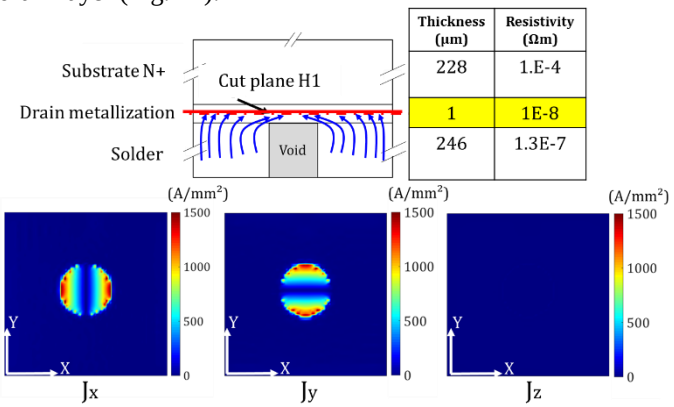



Fig. 12. Current distribution in the MOSFET drain in single-void model

The current density components ($J_x$, $J_y$, $J_z$) are observed in the cut plane H1 crossing the drain metallization layer, parallel to the die surface. This current redistribution is verified by the high current density area on the outskirts of the circles representative to the void in the $J_x$, $J_y$ mappings (Fig. 12). In

contrast, Z-axis current density $J_z$ is negligible. This phenomenon depends on the ratio between the resistance of the portion of the drain metallization above the void and that of the lateral N+ substrate domains, thus void's thickness and resistivity.

After passing through the drain metallization, the current reaches the N+ substrate and tends to redistribute homogeneously in this layer as shown in Fig.13. A similar current density map is visible in the cut plane H2 crossing the substrate N+ layer close to the drain metallization. The current densities $J_x$ and $J_y$ become negligible compared to $J_z$. In addition, $J_z$ is relatively uniform in the cut plane H2. The current tends to return to its vertical distribution as if it hadn't been affected by the void (Fig. 13c,d). It decreases and rises slightly inside and outside the region above the void. The impact of void on electrical behavior of the MOSFET seems to be negligible. Similar phenomena are reproduced for various configurations of single void (corner void, center void, small void, big void …).

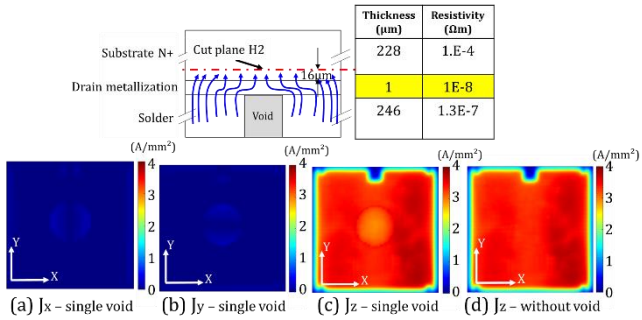



Fig. 13. Current distribution in MOSFET N+ area in single-void model

## IV. Experimental Validation

The validation of the model is done on the same test bench [23] but pulsed conditions are replaced by steady on-state conditions. The current flows in the device under test until thermal equilibrium is reached. The base plate temperature is maintained at 80°C by a temperature control system. The surface temperature of the prototype is measured by an infrared camera CEPIP-FLIR and a K-type open thermocouple placed at a corner of the leadframe. For infrared measurement, we deposit a 10µm-thick paint on the entire upper surface of the prototype which offers an emissivity of 0.93 in the functional wave length interval of the infrared camera [25]. Here we introduce only the validation of single-void simulation consisting in electrical and thermal comparisons. The validation process of void-free model is similar. Furthermore, in order to evaluate the single-void model robustness, 3 configurations of single void have been studied: center void, void located at colder bonding pads (A) side and void under hotter bonding pads (B) side. We will introduce the most critical conditions corresponding to the last one. This configuration is characterized by the following parameter values ($X_v$, $Y_v$, $T_v$, $E_v$, $k_1$, $k_2$) = (5.8mm, 2.2mm, 2.5mm, 197µm, 3.5, 47) (see Fig. 14).

Electrical validation of the finite elements model consists to compare the drop voltages $V_{DS1}$ and $V_{DS2}$ of the MOSFET and that of the bonding wires $V_{S2S3}$ (see Fig. 2) given by simulation and by measurement (Table IV). The small differences, less than 7% between numerical and experimental results demonstrate a good representativeness of the model which is defined by efficient electrothermal characterizations.

TABLE IV
Electrical Validation

| | $V_{DS1}$ (mV) | $V_{DS2}$ (mV) | $V_{S2S3}$ (mV) |
|---|---|---|---|
| Simulation | 154 | 163 | 78 |
| Measurements | 155 | 168 | 73 |
| Difference (%) | 0.6% | 3.1% | -6.4% |

Thermal validation consists to compare the experimental temperature map to the calculated one. Firstly, we evaluate the correlation of the global temperature of prototype issued from both numerical and experimental approaches (see Fig.14). From a qualitative viewpoint, the temperature mappings seem to demonstrate a good agreement at the MOSFET, baseplates, wires and lead-frame level. We can observe a hot spot in the area related to the single void position.

In quantitative terms, the performance of the single-void model is judged by comparing the temperature of both the MOSFET source and the bonding wires especially in the void region. Fig. 15 presents the temperature variation of the MOSFET source along the profile V-V crossing the void centre. We noted that experimental mapping is neither accessible in the areas under the bonding pads nor at the border of the wires due to optical difficulties. The simulation curve passes near the experimental points, especially in the void area where a hot spot is formed.

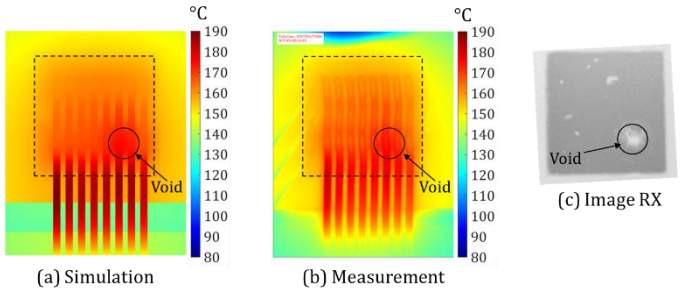



Fig. 14. Thermal validation of single-void model

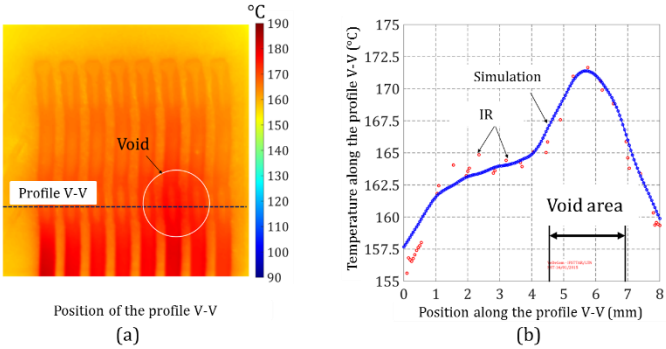



Fig. 15. MOSFET source temperature (b) along the profile V-V (a)

Moreover, a thermal comparison is also carried out at bonding wires level, along the profiles F1 and F6 (Fig. 16). The simulation results and the corresponding experimental ones are similar. The differences are relatively low, about 5%. We remark a soft offset of the position of the maximal temperature probably due to an error in the measurement of bonding wires geometry. In addition, we find out that the temperature of the sixth wire located above the void area, at small loop level is sharply higher than the temperature of the first one. This

observation is the result of the local modification of the current distribution due to the electrothermal behavior discussed in the numerical investigation presented in section III. However, an identical simulation given by the void-free model shows that the maximal temperature of the whole sixth wire at the big loop is not affected by the void because of the low impact of void on the current distribution.

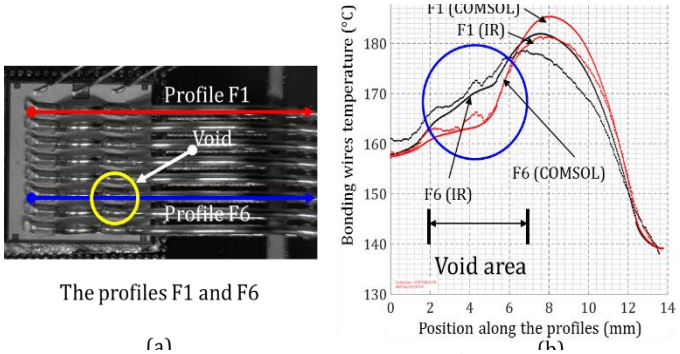



Fig. 16. Bonding wires temperature (b) along the profiles F1 and F6 (a)

Thermal agreement of numerical and experimental results is equally confirmed at the lead-frame and the aluminum plate where the temperature is performed by an open thermocouple and a PT100 probe respectively.

## V. Discussion

### A. *Interest of single-void effects investigation*

According to the simulation results, one void in the chip solder affects the local thermal response of the MOSFET without significant effect on its electrical behavior. In fact, these results seem mainly be dependent on the MOSFET drain metallization properties. The design of this element can be optimized to improve the thermal performance of the power module and limit the hot spot effects. If the drain metallization is thicker and more resistive, its resistance can force the current to flow mainly outside the void area. The power density in this area will be diminished due to the reduction of current density. As a result, the hotspot is less severe and the maximal temperature of the MOSFET will be decreased. An experimental validation is necessary to confirm this observation.

### B. *Multi-voids effects investigation highlight*

In multiple voids case, it is traditionally considered that their effects rise with the void rate. Previous works highlighted that in case of great number of homogenous distributed voids, their effects, due to the overall thermal impedance rise, are less critical [2, 12-13] and allow consequently a more flexible thresholding. In other cases, our results demonstrate that multi-voids effects are quite overestimated. We have pointed out that the criticality of a set of voids can be clearly reduced to only the one having the greatest impact. So, for quality screening purpose in a manufacturing process, criteria based on rate of voids are not sufficiently relevant, multiple-voids effects can be reduced to characteristics of the most critical void only.

In order to illustrate this, we introduce only double-voids model in this paper. We investigate the effect of two voids: void A located under the colder pads and void B positioned under the hotter pads (Fig. 17). The electrical validation process of double-voids model is similar to that of single-void one. For thermal aspect, Fig. 17 shows a good agreement between the double-voids model and IR measurement in term of thermal distribution. We can observe two hotspots.

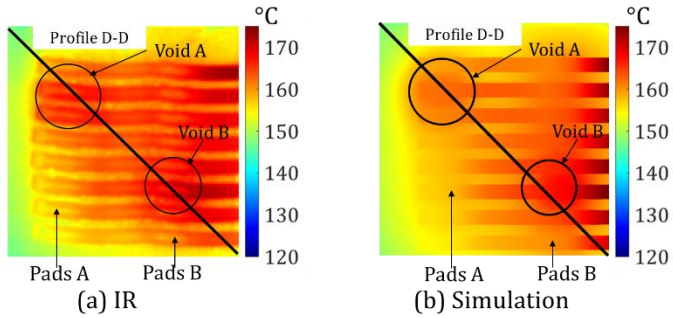



Fig. 17. Case double-voids: Temperature of the MOSFET source and the bonding wires given by IR measurement (a) and simulation (b)

From quantitative viewpoint, the impact of the double-voids is displayed by the temperature distribution along the diagonal profile D-D crossing near the center of the voids at the top surface metallization from IR measurement and simulation (Fig. 18). In order to understand the interactive effect between these voids, we draw the impact of the two voids separately using two simulations with single-void model. So, two curves representing simulation results obtained by single void A and single void B and a third one representing free-void model in the same conditions are added to Fig. 18. We can see that the hot spots issued from double-voids simulation are equivalent to hot spots given by two single voids A and B. On the other hand, the remaining area is almost unchanged and close to the case of without void. These observations shows that the interaction of two distant single voids is not significant and a superposition method can be used as long as voids are sufficiently separated and no thermal coupling occurs between them.

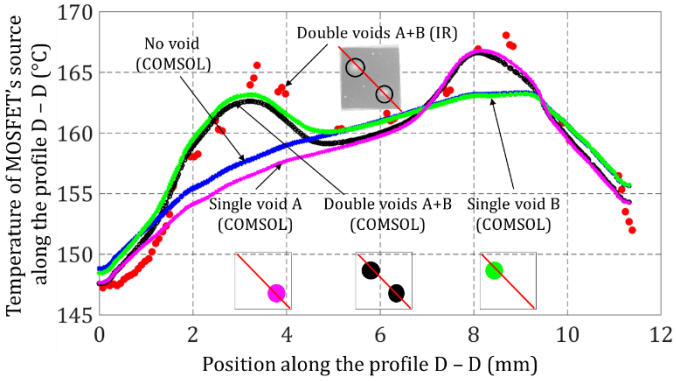



Fig. 18. Evaluation of the interactive effects between void A and B

In order to highlight the voids coupling effects, Fig. 19 performs the interaction of single void C on void D versus their distance. Void D position remain unchanged and void C is “mobile”. We note that the magnitude of the hot spot of void C rises rapidly while void C comes closer to void D. It can be explained firstly by the change of void C position, which is nearer to the hotter bonding pads (pads B) and then the interaction of the two voids. On the contrary, the magnitude change of the hot spot of void D, is less significant. This more critical void seems to be more inert versus the less severe one. The interaction of void C on void D tends to maximize when

their distance is close to zero, correspond to the coalescence of two voids to form a single but larger one.

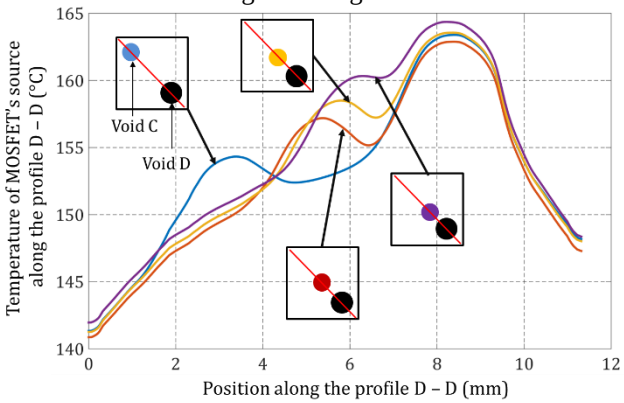



Fig. 19. Evaluation of the interactive effects between void C and D when void C comes closer to void D

The absence of interaction between two distant hot spots offers a cost-effective method for void inspection. Indeed, the severity of a given rate of non-coalesced voids can be deduced from that of the most critical void that we must identify. This observation allows to suggest a more flexible threshold. Void rate is probably no longer a good criterion but the identification of the most critical single void becomes crucial in the investigated operating conditions.

## VI. Conclusion

The electrothermal modelling of low voltage Si MOSFET module in forward bias condition, validated by experimental campaign, is performant and robust to evaluate not only the phenomena from chip scale to packaging level but also the disturbances due to solder void. The simulation results demonstrated the local thermal effect but no significant electrical effect of single and multi-voids on the electrical connections and device behaviour. Their impact seems to depend strongly on the drain metallization properties. The design of this last one can be optimized to reduce void effects.

The extended study on multi-voids showed that their criticality corresponds to that of the most critical single void if the voids are not coalesced. This fact allows a more flexible threshold for void inspection on production line, which avoids mistaken reject. Besides, the identification of the most critical single void becomes crucial in order to fulfil the inspection criteria of solder void.

## VII. Acknowledgement

We would like to extend our grateful thanks to Mr. Jean-Michel MORELLE, Mr. Laurent VIVET, Mr. Ky-Lim TAN and Mr. Serge LAVRENTIEFF, engineers and technicians of the VALEO group for their contribution during the realization of the test prototypes. We would like to express our appreciation to VEDECOM institute members for useful technical and financial supports.

## References

[1] A. Yerman, J. Burgess, R. Carlson, C. Neugebauer, “Hot Spots Caused by Voids and Cracks in the Chip Mountdown Medium in Power Semiconductor Packaging”, *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 6, pp. 473–479, 1983.

[2] L. Chen, M. Paulasto-Kröckel, U. Fröhler, D. Schweitzer, H. Pape, “Thermal impact of randomly distributed solder voids on Rth-JC of MOSFETs”, *2nd Electronics System-Integration Technology Conference (ESTC '08)*, Greenwich, UK, pp. 237–243, 2008.

[3] V.R. Manikam, “Die Attach Materials for High Temperature Applications: A Review”, IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 1, pp. 457–478, 2011.

[4] D.C. Katsis, J.D. Van-Wyk, “Void-induced thermal impedance in power semiconductor modules: Some transient temperature effects”, *IEEE Industry Applications Society*, vol. 39, pp. 1239–1246, 2003.

[5] M. Abtew, G. Selvaduray, “Lead-free solders in microelectronics”, *Materials Science and Engineering Reports*, vol. 27, pp. 95–141, 2000.

[6] R. Diehm, “Reduction of Voids in Solder Joints an Alternative to Vacuum Soldering”, *IPC APEX EXPO Proceedings*, San Diego, USA, 2012.

[7] “Standard MIL – STD – 883G – Method – Ultrasonic Inspection of Die attach,” pp. 1–4, 1987

[8] “Standard IPC-7095C - Design and Assembly Process Implementation for BGAs”, *IPC Ball Grid Array Task Group of the Assembly and Joining Processes Committee of IPC*, 2013

[9] J. Chang, L. Wang, J. Dirk, X. Xie, “Finite element modeling predicts the effects of voids on thermal shock reliability and thermal resistance of power device”, *Welding Journal*, vol. 85, p. 63S–70S, 2006.

[10] M. Thomas, “A Lead-free Solution for Power and High-power Applications”, Advanced Packaging, ISBN-13: 978-9057681448, 2007.

[11] A. S. Fleischer, L. H. Chang, B. C. Johnson, “The effect of die attach voiding on the thermal resistance of chip level packages”, *Microelectroics Reliability*, vol. 46, pp. 794–804, 2006.

[12] K.C. Otiaba, R.S. Bhatti, N.N. Ekere, S. Mallik, M.O. Alam, E.H. Amalu, M. Ekpu, “Numerical study on thermal impacts of different void patterns on performance of chip-scale packaged power device”, *Microelectronics Reliability*, vol. 52, no. 7, pp. 1409–1419, 2012.

[13] N. Zhu, “Thermal impact of solder voids in the electronic packaging of power devices”, *15th IEEE on Semiconductor Thermal Measurement and Management Symposium*, Bedford, U.K, pp. 22–29, 1999.

[14] H. Li, C. Wang, M. Yang, N. Wang, R. An, Y, Xu, “The effect of Voids on Thermal Conductivity of Solder Joints”, *Electronic Packaging Technology and High Density Packaging*, pp. 1061–1064, 2012.

[15] L. Ciampolini, M. Ciappa, P. Malberti, P. Regli, W. Fichtner, “Modelling thermal effects of large contiguous voids in solder joints”, *Microelectronics Journal*, vol. 30, pp. 1115–1123, 1999.

[16] L. Biswal, A. Krishna, D. Sprunger, “Effect of solder voids on thermal performance of a high power electronic module”, *Proceedings of 7th Electronic Packaging Technology Conference*, Singapore, vol. 2, 2005.

[17] R. Bonyadi, O. Alatise, J. Hu, Z. Davletzhanova, Y. Bonyadi, J. Ortiz-Gonzalez, L. Ran, P. Mawby, “Compact electrothermal models for unbalanced parallel conducting Si-IGBTs”, *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 253–260, 2016.

[18] J. B. Sauveplane, P. Tounsi, E. Scheid, “3D electro-thermal investigations for reliability of ultra low ON state resistance power MOSFET”, *Microelectronics Reliability*, vol. 48, pp. 1464–1467, 2008.

[19] G. Calabrese, F. Gualdi, S. Baricordi, “Numerical simulation of the temperature distortions in InGaP/GaAs/Ge solar cells working under high concentrating conditions due to voids presence in the solder joint”, *Solar Energy*, vol. 103, pp. 1–11, 2014.

[20] S. Baricordi, G. Calabrese, F. Gualdi, V. Guidi, M. Pasquini, L. Pozzetti, D. Vincenzi, “A joint thermal-electrical analysis of void formation effects on concentrator silicon solar cells solder layer”, *Solar Energy Materials and Solar Cells*, vol. 111, pp. 133–140, 2013.

[21] L. Dupont, J. L. Blanchard, R. Lallemand, G. Coquery, J.M. Morelle, G. Blondel, , “Experimental and numerical results correlation during extreme use of power MOSFET designed for avalanche functional mode”, *Microelectronics Reliability*, vol. 50, no. 9–11, pp. 1804–1809, 2010.

[22] S. S. Li and W. R. Thurder, “The dopant density and temperature dependence of electron mobility and resistivity in n-type silicon”, *Solid-State Electronics*, vol. 20, pp. 609–616, 1977.

[23] N. Baker, S. Munk-Nielsen, F. Iannuzzo, L. Dupont and M. Liserre, “Experimental evaluation of IGBT junction temperature measurement via peak gate current”, *17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1-11, 2015.

[24] P.D. Desai, H.M. James, C.Y. Ho, “Electrical Resistivity of Aluminum and Manganese”, *Journal of Physical and Chemical*, vol 13, n°4, 1984.

[25] Y. Avenas, L. Dupont, “Evaluation of IGBT thermo-sensitive electrical parameters under different dissipation conditions - Comparison with infrared measurements”, *Microelectronics Reliability*, vol. 52, no. 11, pp. 2617–2626, 2012



**Son Ha TRAN** received th Ph.D degree from the Electrical, Optical, Bio - Physics and Engineering (EOBE), Paris-Saclay University in 2015. His thesis work involved an evaluation of the effects of void in the die attach on the electrothermal behavior of power module. This thesis was a result of a cooperation between the French Institute of Sciences and Technology for Transport, Development and Networks (IFSTTAR) and the Carbon-free, Communicating Vehicle and its Mobility Institute (VEDECOM). He is presently in a post-doc position at IFSTTAR Institute where he focuses his researches on the estimation of power module lifetime based on an analysis of coupling failure modes.



**Laurent DUPONT** received the Electrical Engineer in 2002, and the Ph.D. degree in electrical engineering from the Ecole Normale Supérieure de Cachan (ENS-Cachan), France, in 2006. After ten years of experiences in industry, he works as researcher scientist in the SATIE Laboratory, French Institute of Science and Technology for Transport, Development and Networks, Versailles, France since 2007. His research interests are geared towards the robustness evaluation of power semiconductor modules. The research activities are especially focused about parameters which allow estimations of the temperatures and the ageing indicators of power components in functional conditions.



**Zoubir KHATIR** received the Dipl.-Ing. degree in solid-state physics and the Ph.D. degree from the Institut National des Sciences Appliquées de Toulouse, Toulouse, France, in 1984 and 1988, respectively. He has been with the Laboratory of New Technology, French National Institute for Transport and Safety Research, Versailles, France, since 1988, where he was in charge of high-power semiconductor device modeling and computer-aided design tool development. He is currently a Senior Scientist with the SATIE Laboratory, French Institute of Science and Technology for Transport, Development and Networks, Versailles, France. His current research interests include the reliability in high-temperature environments of silicon and wide band gap high-power electronic devices in the field of transport applications.