High-Density 3-D Capacitors for Power Systems On-Chip: Evaluation of a Technology Based on Silicon Submicrometer Pore Arrays Formed by Electrochemical Etching

Magali Brunet, Pascal Kleimann

High-density 3D capacitors for Power Systems on-Chip: evaluation of a technology based on silicon submicrometer pore arrays formed by electrochemical etching.

Magali Brunet[1,2], Pascal Kleimann[3]
[1] CNRS, LAAS, 7 avenue du colonel Roche, F-31400 Toulouse, France
[2] Univ de Toulouse, LAAS, F-31400 Toulouse, France
[3.] INL, Institut des Nanotechologies de Lyon, Univ Claude Bernard-Lyon 1, F-69622 Villeurbanne, France

Abstract. This paper presents the state of the art technologies currently used to produce high density integrated capacitors for power systems on-chip applications. The use of high-*k* dielectrics and 3D patterning of silicon for reaching high specific capacitance is reviewed. Integrating capacitors monolithically on the active chip or in package of power systems is discussed and solutions are proposed for minimising series resistance and achieving a high level of integration. A technology based on nanolithography and silicon electrochemical etching is then detailed. It is shown that capacitance densities of up to 700 nF/mm² can be obtained with a submicrometer pores array in a relatively limited thickness. The advantages and disadvantages of further decreasing the pore size to nanosize pores (below 100 nm) are discussed.

I. INTRODUCTION:

The recent boom in multifunctional portable electronics has imposed a drastic size reduction in power systems. Within the device, multiple functions working at different voltage/current levels coexist and impose several converters to step-up or step-down the battery voltage. Typical specifications for conversion in portable equipment are a power of 1W, input voltages lower than 5 V and an output current between 100 mA and 1 A. Types of voltage converters include switched-mode converters (inductive or capacitive) or linear regulators. Inductive type switched-mode DC-DC converters can present the highest power efficiency and require the lowest number of passive components: one inductor and two capacitors, but their value should be relatively high for efficient filtering. For example, current commercial miniaturized low power DC-DC converters (buck type) that operate in the MHz range frequency (such as Texas Instruments LM8801), require the use of an output inductor and capacitors with a typical inductance value of 0.47 µH and capacitance values between 2.2 µF and 4.7 µF. Up to now, Multi Layered Ceramic Capacitors (MLCCs) and inductors (MLCIs) have been mostly used because they have the highest density, However, they are relatively thick (typically over 500 µm) and their manufacturing is not compatible for integration on-chip in particular because of high temperature sintering steps.

To realize the objective of high performance power systems on-chip (SoC) with high power density (above 1W/mm²) and high efficiency (above 90%), increasing the switching frequency is unavoidable. This enables the reduction of passive components and therefore, their integration on-chip. This integration requires adapted technologies and materials. Research and development has been pursued for many years in this field. A successful integration of passive components on-chip may lead to low profile power modules with the following advantages: enhanced reliability through the reduction of interconnections, reduction of costs through collective fabrication, and co-integration with other components of the system. High densities and low losses for passive components are crucial goals. Reliability and cost are other concerns that must also be considered.

For the specific case of integrated capacitors in power conversion applications, the requirements are:

- A high specific capacitance: at least 1 µF/mm² to compete with MLCCs.
- A reasonable breakdown voltage (depending on the system output power). Typically, a rule of thumb would be to have a breakdown voltage 1.5 times higher than the operating output voltage.
- A low Equivalent Series Resistance (ESR): < 100 mΩ for minimum output ripple voltage and losses on the frequency range of system operation. Losses degrade the system efficiency.

This article reviews existing technologies and materials developed by industry and research labs to reach these objectives for on-chip capacitors: particularly high specific capacitance for which it is shown that the use of the third dimension is unavoidable. Solutions to reduce series resistance and compatibility of processes are reviewed and discussed for power systems integration: on-chip (SoC) with the active circuit including the power MOSFETS and the control digital circuit or intermediately in-package (SiP) with other passive components (inductor, resistor) inside an IPD (Integrated Passive Device). A process based on electrochemical etching of submicron-size pores in silicon is then proposed. The advantages and disadvantages of further decreasing the pore size are also discussed.

II. State of the Art

A. Technologies for high density capacitors

High specific capacitances may be reached by decreasing the dielectric thickness, increasing the surface area or by using a dielectric with high dielectric constant (*k*). Decreasing the dielectric thickness, like in gate-oxides, to a few monolayers is not an option for capacitors in power applications because this thinning leads to higher leakage current and lower breakdown voltages. Advances in dielectrics and 3D technologies are now reviewed.

1) Dielectrics

In planar form, high-*k* dielectrics have been widely investigated as a replacement for silicon oxide in transistors gate [1]. Other applications where high-*k* dielectrics are interesting include integrated capacitors for decoupling, RF Integrated Circuits (RFICs), analog/mixed signal circuits, or DRAM applications. Medium-*k* dielectrics such as Ta_2O_5, Al_2O_3, HfO_2, ZrO_2, La_2O_3, TiO_2, [2, 3, 4]with dielectric constants in the range of 10-20 (about 80 for TiO_2) are the most widely used because they can be deposited with Chemical Vapour Deposition (CVD) techniques and thermodynamically they show thermal stability with silicon. Very high-*k* dielectrics generally presents a perovskite structure, such as $SrTiO_3$ [5], $BaTiO_3$, $BaSrTiO_3$, $PbZrTiO_3$ [6], $PbLaZrTiO_3$ [7], which leads to dielectric constants typically above 100 and in some cases around or above 1000.

In planar configuration, capacitors with thin film high-*k* dielectrics (perovskite type or other) reach maximum specific capacitances of 40-50 nF/mm². In terms of other electrical characteristics, electric breakdown fields of these high-*k* dielectrics is much lower than SiO_2 (13 MV/cm) and it was shown by Jain et al.[8] that it follows an empirical relationship: E_{BD} (MV/cm)= 20/√k: the higher the dielectric constant, the lower the breakdown field. Furthermore, perovskite materials in particular present the major drawback of being variable versus voltage, temperature and frequencies. They also have to be crystallized at high temperature.

Alternative solutions are now been investigated to push forward the electrical intrinsic performance of dielectrics. Nano-laminates are a very interesting possibility: alternative deposition of medium-*k* dielectrics (for instance Al_2O_3/HfO_2 [9]) produce enhanced performance, low leakage, larger breakdown field and higher dielectric constant. A giant dielectric constant of around 1000 was recently demonstrated for AlO_x/TiO_y nanolaminates [10]. These giant dielectric constants are explained by the Maxwell-Wagners effect [11] where the charges accumulate at the interfaces of the dielectric material with the lowest conductance, producing an interfacial relaxation: this relaxation is the external contribution to the dielectric constant. A fine engineering on the layers thickness is necessary, however, to find a trade-off between a high dielectric constant and low leakage current. The inclusion of nanoclusters of one dielectric inside another (matrix) is another exploitation of the same effect. For instance, ZrO_2 in an amorphous La_2O_3 matrix leading to$La_yZr_{1-y}O_x$ [12] showed a reasonably high dielectric constant (k = 36) combined with lower leakage current and high breakdown field: 7 MV/cm for ZrO_2 grain size of 2 nm contained in the matrix compared to 4 MV/cm for pure La_2O_3. These results proved the possibility to push the limit imposed by the empirical relationship linking the breakdown voltage to the dielectric constant. Another big advantage of these nanolaminates or nanoclustered materials is that they can be deposited at relatively low temperature with Atomic Layer Deposition technique (ALD). Specific capacitances for planar capacitors including nanolaminates of around 20 nF/mm² have been reported [13, 14].

Research in high-*k* dielectrics is showing promise in producing MIM capacitors with enhanced performance. In planar form however, specific capacitances are still limited. To be considered in power systems applications, moving towards 3D structures is an unavoidable step which is now reviewed in the following section.

2) Three-dimensional electrodes.

Increasing the surface to volume ratio is an extensively studied solution for obtaining higher specific capacitance. Figure 1 presents a schematic of a 3D capacitor structure realized in silicon.

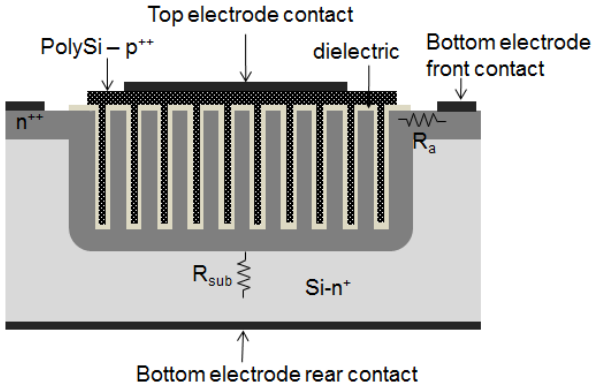

Figure 1. Schematic of a 3D capacitor realized in a silicon substrate with possible contacts. Bottom electrode can be contacted on the front side (horizontal configuration) or the rear side (vertical configuration).

Processes with high aspect ratio trenches or pores etched in silicon were originally developed in the 80's for miniaturizing the storage capacitor for DRAM applications. Among these processes, we can find electrochemical etching in HF-based electrolytes developed by Siemens in 1996 [15] and DRIE (Deep Reactive Ion Etching) by Philips Research in 2001 [16]. Specific capacitances of 125 nF/mm² (aspect ratio 85) and 30 nF/mm² (aspect ratio 20) were demonstrated respectively with standard dielectric stack ONO ($SiO_2/Si_3N_4/SiO_2$).

Patterns density as well as patterns geometry: holes or pillars, square or round shape [17] are important parameters to optimise the specific capacitance. It is easily understood that the best packing factor is provided by a hexagonal arrangement of patterns. In terms of patterns, tripods were adopted by Philips Research/NXP [18] as they can be placed easily in a hexagonal arrangement and offer an enhanced developed surface. They also facilitate transport of gaseous reagents and products during silicon etching and deposition of dielectrics.

Combining the deposition of high-*k* materials with high developed surface area is a natural evolution. However, conformal deposition of high-*k* dielectrics inside high aspect ratio 3D structures has remained a challenge in the last ten years. CVD processes are the most suitable techniques: MOCVD (Metal Organic CVD) [19] or ALD [20]. Single oxides (e.g. Al_2O_3, HfO_2) as well as binary metal oxides (e.g. $Hf_xAl_{1-x}O_y$) are most common for ALD processes thanks to available and volatile precursors. With ALD or MOCVD, ternary alloys such as $SrTiO_3$, $BaTiO_3$ can also be deposited [21] but it is more difficult to control and obtain

good uniformity and conformal deposition over 3D structures. It is foreseen that future research will focus on the deposition of nanoclustered materials or nanolaminates inside 3D structures.

To produce high specific capacitance, implementing multiple layers of metal/dielectric creating MIMIM structures is another option that has been explored by Philips Research: Klootwijk et al. demonstrated 440 nF/mm² by growing multiple layers by ALD of TiN/Al_2O_3 inside high aspect ratio pores [22]. However, this solution requires a high number of masks (one for each metal layer) which significantly increases the cost of manufacturing. With a similar type of stacking, IPDIA recently announced a 550 nF/mm² capacitor that will be soon in production [23].

3D structuration of the silicon substrate in the micrometer-range (macropores) with DRIE is a mature technology which allows actors in the industry to produce capacitors on-chip with a specific capacitance of the order of a few hundreds of nF/mm², excellent voltage stability, low leakage and a high manufacturing yield. 3D capacitors have been commercialized by IPDIA under the name of PICS™ technology (Passive Integration Connective Substrate); Infineon Technologies under the name of SilCap™ [24] and ST microelectronics under the name of IPAD™.

Beyond macroporous silicon, there is a trend towards nanostructures for high density capacitors in recent research. Alternative solutions for 3D capacitors have been recently demonstrated that introduce high aspect-ratio nano-structures such as nanotubes [25], nanopillars [26], nanomembranes [27] and coated nanopores in an anodic aluminium oxide (AAO) matrix [28,29]. The last two cases allow specific capacitances higher than 1 µF/mm². Important parameters such as equivalent series resistance (ESR), breakdown voltage and compatibility of processes however are rarely discussed.

B. Other challenges for capacitors in DC-DC converters application

1) Equivalent Series Resistance (ESR)

In the output filter of a switched-mode converter, the Equivalent Series Resistance (ESR) of the capacitor will be responsible for the output voltage ripple. It will also produce losses that will degrade the efficiency of the system. This is of major concern for realizing high efficiency power systems where other components of the circuit already generate losses: inductor, power MOS (on-state and switching losses). A typical acceptable resistance value for output filter capacitors in 1W power converters operating in the MHz range is between 50 and 100 mΩ.

ESR includes several contributions: the physical series resistance of the electrodes (ohmic contribution), the parallel resistance due to leakage current in the dielectric and the dissipation factor due to dielectric losses. For switched mode power converters, leakage current is not as important as in low frequency filtering applications. Capacitors are required to operate in the MHz frequency range and above where leakage current contribution no longer exists. Dissipation losses on the other hand, might present an issue in medium to high frequency applications. They are deeply linked to the dielectric nature with loss mechanisms due to relaxations and resonances spreading out on the frequency scale [30]. These AC losses are generally much higher for high-*k* dielectrics.

However, the major contribution of the ESR in 3D silicon integrated capacitors is the physical series resistance of the electrodes. To minimize this, one should work with low resistivity electrode material and tune the geometry to reduce access to external electrical contacts. In the case of 3D structures in silicon, the substrate is usually highly doped with a boron or phosphorus diffusion step. Doped polysilicon with a minimum resistivity of 1 mΩ.cm is generally used as the top electrode.

Aside the material itself, tuned designs are necessary to reduce the access resistance between the two electrodes of the capacitor. If the contact for the bottom electrode is taken on the rear side of the wafer as schematized in **Figure 1**, the bulk resistivity of the substrate will be an important factor. Solutions include reducing the thickness of the substrate by CMP (Chemical Mechanical Planarization) or creating cavities at the bottom of the structure [31,32]. If the contact for the bottom electrode is to be taken at the front side, the lateral resistance (R_a in Figure 1) will be dominant. A diffusion step to highly dope the substrate is compulsory. However, other factors can influence the lateral resistance. It was shown in our previously published work [33] that substrate initial doping is influencing the lateral resistance in doped Si/dielectric/PolySi 3D capacitors. On N-type silicon substrates with two different initial dopings: 10^{12} at/cm^3 and 10^{19} at/cm^3, the phosphorus diffusion step was applied to form a highly doped layer: 10^{21} at/cm^3 at the surface with a depth of 1.5 µm. It was shown that the series resistance for an initial doping of 10^{19}at/cm^3 is reduced by a factor 2 compared to the substrate with a doping of 10^{12} at/cm^3. Therefore, despite the doped region 10^{21} at/cm^3 at the surface, the substrate doping underneath still has a large effect over the series resistance.

Another solution to reduce this lateral access resistance is to place the contact for the bottom electrode inside the pores area in dummy trenches. Infineon capacitor design includes this type of dummy trenches [34]. On Semiconductor has also proposed a wrap-around PIP (PolySi/Isolation/PolySi) capacitor where a trench filled with polysilicon contacts the doped bottom plate [35]. This distributed electrodes configuration is beneficial to reduce the access resistance of the component.

To replace doped polysilicon/silicon, metals or conductive oxides/nitrides with lower resistivity are employed such as TiN (13 µΩ.cm), Pt (10 µΩ.cm), Ru (40 µΩ.cm), TaN (200 µΩ.cm). For perovskite material, some of these metals (in particular Pt, Ru) are essential in the growth of the crystalline phase due to the reduction of lattice mismatch at the electrode/dielectric interface. They can also behave as a diffusion barrier during high temperature deposition or crystallisation steps.

When considering 3D structures, similar to high-k dielectric materials, concerns about conformal deposition may arise. Some conductors are a better choice than others: TiN for example, is an excellent candidate because it is easily deposited by CVD techniques with a mixture of $TiCl_4$ and NH_3 gazes, and perfect conformal deposition over 3D structures can be obtained [22].

2) Integration in Power Systems: on-Chip (SoC) or in-Package (SiP).

The presented technologies for high-density capacitors have to be considered with regards to the objective of integration within the power system. For miniaturized DC-DC converter applications, several possibilities regarding implementation

can be proposed and the compatibility of processes is now discussed.

For a maximum level of integration leading to Power SoC, passive components should be integrated within the die which contains the power switches (MOSFETs) and the analog/digital circuits (for voltage regulation, signal conditioning, system control and diagnostics). Active devices technology supporting medium and low voltage loads is called smart power concept. For power functions including vertical power components, realization can be based on a 3D heterogeneous functional integration concept [36].

As discussed in the introduction, the increase of switching frequencies is the enabling factor for using small size passive components with low value and for an efficient integration on-chip. Converter topologies that allow operating at very high frequencies (around or above 100 MHz) and that are based on high-speed digital CMOS processes have been investigated. A first example is multiphase switched mode converters, in which interleaving is applied: several output passive components with lower value are parallelized. Following this path, a couple of fully integrated power converters have been reported in the literature, i.e. with passive components on-chip. For instance, a 2-stage interleaved synchronous buck converter (V_{in} = 2.8 V; V_{out} =1.8V) working at 45 MHz, with an output current of 200 mA was reported by Freescale and Arizona State University [37] where passive components are fabricated on the passivation level of the power circuit. A team from the University of Leuven [38] presented a four-phase converter 800 mW operating at 225 MHz (V_{in} = 2.6 V; V_{out} =1.2V), where 4 inductors (4nH) and 2 capacitors (12 nF) were fabricated directly on the CMOS-chip. Despite limited power densities (around 200 mW/mm² in general) and efficiencies from around 60% to a maximum of 80%, these types of converters are an interesting solution in terms of integration. Other foreseen power converters with a high level of integration are switched capacitors (SC) type converters. Their major advantages are they do not require any inductor and since they are also working at very high frequencies (above 100 MHz), they are using low value capacitors (MOS or MIM type). Combined with interleaving, up to 1 W/mm² and 80% efficiency was demonstrated by the University of California at Berkeley [39]. In both type of topologies, the number of additional steps for implementing passive components is kept minimum. Capacitors are fabricated at the same time as the MOS between the gate electrode and the strong inversion channel of a MOS device or are placed like inductors within the upper layers of the metal stack. The use of existing technologies, without introducing new materials is highly beneficial for industry in regards of cost.

However, it is clear that these types of applications could benefit in terms of power density of the technologies for high density capacitors presented in this article: high-*k* dielectrics and/or 3D technologies. It was recently demonstrated by IBM T.J. Watson Research Center that deep trench capacitors included in a switched capacitor voltage converter (V_{in} = 2 V; V_{out} =1V) can lead to 2.1 W/mm² [40]. In this case, CMOS compatibility of the processes employed to create the 3D capacitors should be ensured, as thermal budget from one component can create unwanted diffusion in the other component.

As an example of compatibility and pooling of technological steps between active and passive components, our team at LAAS-CNRS published a study on how to integrate 3D capacitors with power devices on the same wafer using the functional integration concept [41]. In power conversion, for switches control, the realization of drivers autonomous in energy, requires a storage cell. It was shown that a 3D capacitor can be integrated as a storage element with a diode and a NMOS. Some steps can be common between the active component and the passive component: the dielectric and doped polysilicon are two necessary steps for each type of component. If isolation from high voltages is required, it is proposed that the capacitor is realized inside a diffused region: in this particular case, the diffused region is the P^+ well of the MOS which is several microns deep and which is formed at the beginning of the process.

If capacitors are to be integrated within metal/passivation layers, the thermal budget should be less than 450°C, which corresponds to the Cu back-end line thermal budget. This temperature limitation prevents the use of some of the dielectric materials: perovskites for instance requiring annealing above 500°C for crystallization.

For power systems requiring higher values of passive components, in particular for higher power level (> 1W), or when adapting technologies on front-end production lines is too costly, a lower level of integration can be interesting where passive components are realized on a separate substrate. This is what's called Integrated Passive Devices (IPD). For realizing the whole System in Package (SiP), the active die (CMOS or other) is flip-chipped on the passive die. Larger flexibility on the processes is then allowed: the CMOS compatibility is no longer a necessity.

Following this idea of IPD, and lead by the highly developed field of 3D silicon interposer in the industry, the integration of passive components on or inside the interposer wafer is widely experimented [42,43]. The interconnect parasitics such as resistance inductance are reduced. A demonstration of a DC-DC converter implemented this way was shown by the University of Tokyo [44] and Philips Research team [45]. This type of integration benefits from research on high-*k* dielectrics [46].

The use of the third dimension for integration in an interposer has also been studied. To go further, companies such as ST Microlectronics, IBM are seeking to realize simultaneously TSV (Through Silicon Via) and capacitors. Although specific capacitance in this case is limited (less than 200 nF/mm²) [47], the realization of the capacitor doesn't require many additional steps, which is highly beneficial for reliability and cost.

Finally, if the capacitors are integrated with the MOS switches on the active die or within an interposer, some common issues need to be addressed. First, high specific capacitance should be combined with low profile. In 3D integration for SiPs, very thin substrates should be produced to avoid bulky 3D stacks: typical thickness for an interposer is 50 µm. In SoCs, active dies are also generally thinned down. Hence, low profile integrated capacitors are required.

The second issue concerns parasitics generated by proximity of components. In the case of passive dies, integrating the capacitor with the inductor raises some challenges: the capacitor is placed below or beside the inductor. If placed besides, the benefit of integration is limited due to non-optimised footprint area. If placed below, some parasitics effects are detected [45]. To avoid eddy current effects induced in the highly doped region of the 3D capacitor's electrodes, a magnetic shield (CoNiFe thin layer) below the

micro-inductor was proposed by our team at LAAS-CNRS [33].

III. Submicron patterning of silicon through nanolithography and electrochemical etching (EE) technique.

As explained in the previous section, going towards very high density pores arrays can present a real advantage to produce integrated 3D capacitors. We will now propose a technology based on nanolithography and electrochemical etching (EE) for submicron patterning of silicon.

A. Specific capacitance versus pore density: theory.

In 3D geometries, depth of patterns as well as packing densities will dictate the maximum achievable specific capacitance. The specific capacitance (C_s) in Farad per surface unit is expressed as follows:

$$C_s = \frac{\varepsilon_0 \varepsilon_r}{e} \frac{S_{3D}}{S_{plan}}$$

Where e is the thickness of the dielectric layer, S_{3D} is the developed surface due to pores, and S_{plan} is the projected surface.

For circular pores,

$$S_{3D} = S_{plan}(1 + n\pi wh)$$

n is the pore density, i.e. number of pores per surface unit, w is the diameter of a pore, h is the depth of a pore. n depends on the pore array type: hexagonal, regular…etc.

To maximise the specific capacitance, n, h and w should be increased. However, it is easily understood that w and n are linked geometrically: when n increases, the pitch (p) is reduced which implies that w will necessarily decrease. In parallel, w and h are linked by the etching technique (DRIE or electrochemical etching) that will dictate the maximum achievable aspect ratio (h/w).

For illustration purposes, calculations were made for circular pores arranged in hexagonal array with pore diameter w = ¾ p. Figure 2 is the calculated specific capacitance versus depth (h) for 4 different pore densities (n). Oxide nitride stack with equivalent permittivity of 5.7 was chosen as a dielectric. It has to be noted that for each pore density, the specific capacitance was plotted until the aspect ratio (h/w) reached 200, one of the highest reported aspect ratios for porous silicon [48].

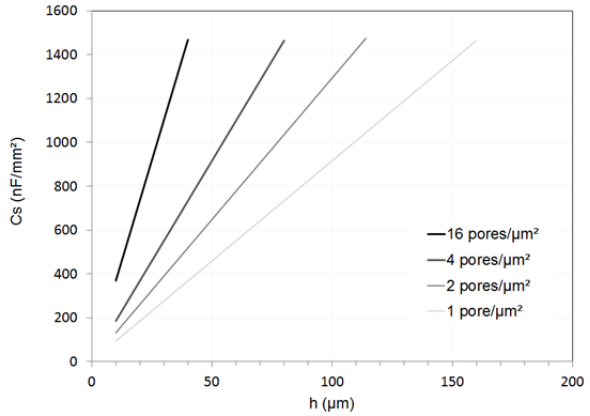

Figure 2. Specific capacitance versus depth (*h*) for 4 different pore densities. Pores are arranged in hexagonal arrays with *w*= ¾ *p*. Dielectric in this case is ON ($SiO_2$5 nm/$Si_3N_4$10 nm)

We show here that the higher the pore density, the lower the depth required to reach high specific capacitances. In figure 2, 1000 nF/mm² is obtained for a 1 pore/µm² density array with 110 µm deep pores. The same specific capacitance can be obtained with a depth of only 55 µm when the pore density is multiplied by 4. Reducing the pore depth is a major advantage for integration of the capacitor with active components or in 3D stacking of chips where thickness is critical as discussed earlier. The other advantage is the etching time which is reduced for shallow pores improving throughput during manufacturing.

In terms of available technologies for patterning silicon at the nanoscale, DRIE is a possibility but two limitations appear. First, the etched depth will be limited by the mask thickness. If nanosize patterns are to be produced, very thin photoresists are generally used, and they are quickly consumed under the etch gases. Secondly, the high aspect ratio of nanopores will be limited due to Aspect Ratio Dependent Etching (ARDE) effect. The alternative solution is the well-established technique of n-type silicon electrochemical etching with backside illumination in HF-based electrolytes [15]. The main interest of the electrochemical etching technique compared to DRIE is that once the pores are formed, the mask is no longer necessary and vertical etching carries on until diffusion limit. Aspect ratios of 200 are possible [48]. Additionally, the ARDE is less pronounced than in DRIE, no scalloping is produced and very high aspect ratios can be reached.

To demonstrate this possible technology for producing very high density capacitors, a process using nanotechnology and electrochemical etching was developed. The presented process is simple with only two steps: nanolithography and electrochemical etching. No initial pits formed by a KOH step are necessary [49,50].

B. Experimental.

The experimental setup used and the conditions required for a proper formation of submicron pores by electrochemical etching are widely described in [51] with arrays of 1 µm, 750 nm and 500 nm pitches. In this work, the diameter of the pores defined by lithography is 100 nm arranged in a regular array with a pitch of 1 µm corresponding to a density of the pore array of 1 pore/µm². Nanoimprint lithography and electron beam lithography were both used to pattern the array.

Briefly, in a standard cell made of Teflon, the electrochemical bath was prepared with the following composition Ethanol:BHF:H_2O/200:60:600. The use of Buffered HF (Merch-Ammonium fluoride etchant AF 87.5-12.5d) rather than HF prevents the resist from delaminating during etching. Illumination on the backside was assured by an infrared lamp that controlled the etching current. The electrochemical etching parameters, such as current, voltage, temperature, BHF concentration, together with the substrate doping were adjusted to obtain a regular array of well-formed pores. The objective was also to produce pores with a large diameter, ideally equal to ¾ of the pitch, in order to obtain the maximum specific capacitance while keeping a mechanically strong array structure. The resistivity of the substrate was adjusted to 0.43 Ω.cm.

Figure 3 shows a cross-section and top views (insert on the top left) of the pores at the end of 3h of electrochemical etching under 2V. The pores are measured to be 730 nm wide and 72.2 µm deep (etching rate of 0.4 µm/min) corresponding to an aspect ratio of 98. With 4h of etching,

90 µm could be reached. The effective area increase in this case is 210.

At the end of the etching step, a RCA clean was done, followed by the dielectric deposition: the dielectric was constituted of a thin silicon oxide layer (5 nm) thermally grown, on which a 10 nm Si_3N_4 layer was deposited by Low Pressure CVD (LPCVD). Highly doped p-type polycrystalline silicon was then deposited by LPCVD to fill the cavities and patterned into squares: 100 x 100 µm² and 250 x 250 µm². This layer constitutes the top electrode of the capacitor. Finally, metal contacts were created on top of the polycrystalline silicon layer by a lift-off of aluminium layer and on the bottom of the wafer by an Au-Si eutectic bonding on a package.

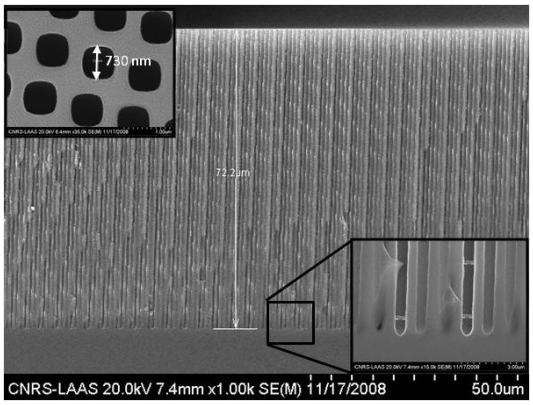

Figure 3. SEM pictures of array with a density of 1 pore/µm² after 3h of electrochemical etching with a zoom on the bottom of the pores; insert: top view where pore width is shown to be 730 nm.

C. Electrical characterizations.

On the fabricated 3D capacitors, electrical measurements were carried out under probes. Impedance characteristics were measured with an Agilent Impedance Analyser 4294A on a wide range of frequencies. I(V) characteristics were obtained with a KeithleySC4200prober. Figure 4a) shows the specific capacitance versus frequency for three 3D capacitors of each size. The specific capacitance measured is around 700 nF/mm². Some parasitic are affecting the measurements. In particular, at low frequencies (below 100 kHz), the capacitors present a parallel resistance due to leakage. Leakage is also clearly shown in Figure 4b) with the ESR increasing drastically below 100 kHz. Above 100 kHz, ESR is around 20 Ω for all capacitors. In this particular case, the resistance is related to the distance between the eutectic bonding on the rear of the silicon wafer and the beginning of the etched area as well as the resistivity of the silicon substrate. This is not the final configuration where both contacts will be taken at the front side and where the silicon will be highly doped by an additional phosphorus diffusion step. Leakage is also confirmed on the I(V) characteristics shown in

Figure 5: current densities of about $1x10^{-3}$ A/cm² are measured. The capacitors breakdown voltage occurs around 8V, which is lower than the expected theoretical breakdown voltage (13V).

It is believed that for very deep pores, the defects in the pores (transversal to the vertical pores) are at the origin of such leakage since the Si_3N_4 deposited by LPCVD may not cover properly all the asperities. Some investigation on the problem reveals that this transversal etching occurs by breakdown [51]. The breakdown is even more important when the silicon resistivity is low, and therefore could be overcome by adjusting the substrate resistivity. To summarize, the resistivity has to be high enough to limit breakdown and low enough to enable the formation of a regular high density array of well-formed pores.

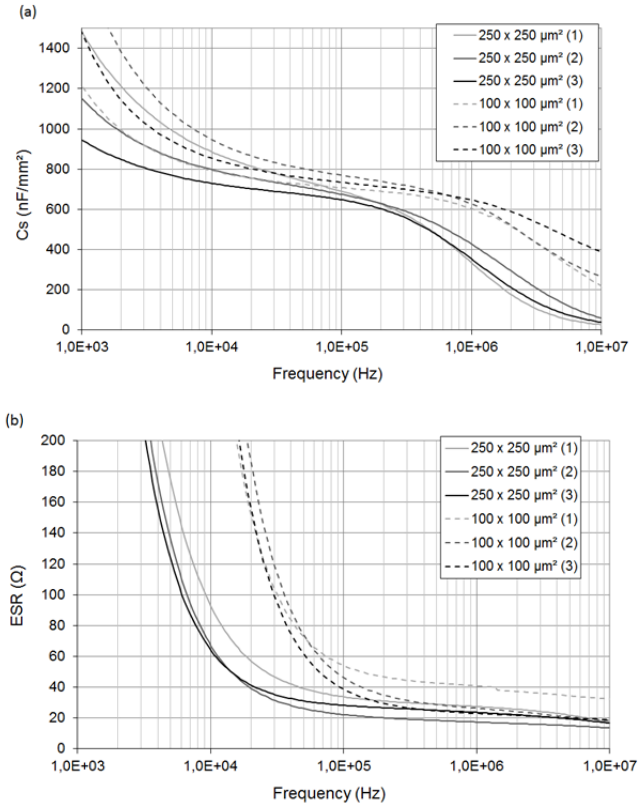

Figure 4. Measured a) specific capacitance and b) equivalent series resistance versus frequency for 250 x 250 µm² and 100 x 100 µm² 3D capacitors fabricated with electrochemical etching method. Density is 1 pore/µm²

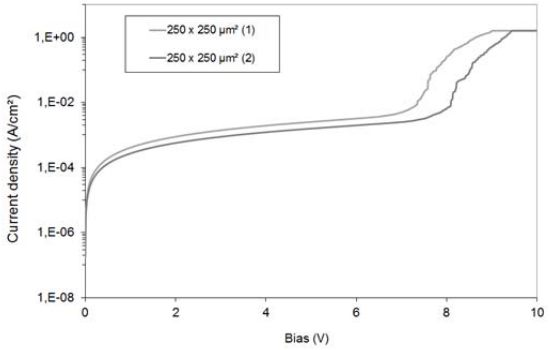

Figure 5. Measured current density versus bias for two 250 x 250 µm² 3D capacitors fabricated with electrochemical etching method.

Despite some technological issues on the components realization leading to leakage in the measured electrical characteristics, a very high specific capacitance could be demonstrated with submicron size pores (730 nm diameter). This is achieved with a minimum number of technological steps and standard dielectric layers. Going towards lower pitch pores arrays would allow to further decrease the thickness of the component in the silicon substrate. Arrays with a 300 nm pitch, corresponding to a density of 13 pores/µm², seem achievable [51]. Using such pore densities would significantly further increase the specific capacitance.

Table 1.Performance of State-of-the-Art Integrated Capacitors

Institution [Ref]	Configuration	Stack	V_{max} (V)	C (nF/mm²)	ESR (Ω)	Advantages	Disadvantages
Philips Res [16]]	3D by DRIE	n^+-polySi/ONO/n^+Si	30	25	0.145	Standard, conformal dielectrics CMOS compatible	Limited specific capacitance
Philips Res [22]	3D by DRIE	TiN/Al_2O_3 (x3)	6	440	10	CMOS compatible	High number of ALD layers and process steps (high cost)
Univ. Mary [28]	3D by AAO	TiN/Al_2O_3	4	1000 (<100 Hz)	Not given	Very low profile (<10 µm)	Very thin layers leading to low breakdown / high ESR Not CMOS compatible
This work	3D by EE	n^+-polySi /ON/n^+ Si	8	700	20	Standard, conformal dielectrics Low number of steps CMOS compatible	Substrate resistivity to tune

* ONO and polySi stacks are deposited through thermal oxidation or CVD; TiN/Al_2O_3 stacks are deposited by ALD.

IV. Discussion

A. Comparison with state-of-the-art.

Table 1 presents a comparison of the 3D capacitors realized in the previous section with the state-of-the-art. Advantages and disadvantages of each proposed technology are listed in light of integrated power applications. All reported processes in table 1 can be implemented in SiP, i.e. realized on the same substrate with other passive components or interconnections. Therefore, only indication of possible implementation on-chip (SoC) requiring CMOS compatibility is provided. Most processes including high-*k* dielectrics deposited by ALD (relatively low temperature) are considered as CMOS compatible. Indication of cost includes the number of steps and throughput of processes. ALD in this case is not advantageous as it is considered as a costly technique with low throughput.

The reported technology presents a good compromise between electrical properties for power applications and implementation within a system on chip. In addition, the process is CMOS compatible, uses standard dielectrics. The number of process steps is kept to a minimum. Demonstrated prototypes have a depth of 70 µm. A lower profile could be produced by etching higher density pores arrays. A disadvantage is the need to tune the substrate resistivity. However, to get around this problem, the pores array can be formed locally in a diffused region of the silicon substrate.

B. Towards nano-size pores?

With regards to going towards nano-sized pores (below 100 nm diameter), the question must be asked: is there a real benefit or is there an optimum point to reach for the application of capacitors for power systems?

Diminishing the pore diameter will influence the stacking: thicknesses will be dictated by the pore diameter. The full MIM structure has to be accommodated within the pore. For pores of 40 nm diameter for instance (such as the ones produced typically in an AAO matrix), thickness of the metal and dielectric layers is about a few nanometers [27,28]. Two disadvantages of this pore size reduction clearly appear: first, the thinner the dielectric, the lower the breakdown voltages. Leakage current can also increase drastically due to tunnelling. Secondly, with thinner metal layers, series resistance will increase considerably even if a metal with a very good conductivity is used.

Hence, for power systems applications, there is a limit in going towards nano-size pores. Depending on the application specifications, and the material used (metal and dielectric), there is a minimum pore size that can be determined to meet the requirements in series resistance and breakdown voltage. This study should be performed through fine modelling of the ESR in 3D structures.

V. Conclusions.

In this article, technologies for high density capacitors were reviewed and discussed in the perspective of power systems on-chip. It was demonstrated that 3D capacitors are currently necessary because high *k* dielectrics, despite major recent improvements in research, do not reach the requirement of 1 µF/mm² useful for power conversion systems working in the MHz frequency range. Other important points were also raised including ESR which should be minimized in power converter applications and compatibility of processes for SoC integration.

A technology based on nanolithography and electrochemical etching was developed to realize very high aspect ratio submicron pores arranged in dense regular arrays. With standard dielectrics stacks (oxide, nitride) the specific capacitance of realized 3D capacitors was measured to be around 700 nF/mm². The proposed technology leads to much higher pore densities and aspect ratios than DRIE.

Going towards arrays of nanosize pores was then discussed. Although very high specific capacitance can be reached, there is an optimum point to find to avoid the deterioration of series resistance and breakdown voltage.

VI. Acknowledgement

The authors would like to thank the Micro and Nano technology Platform of LAAS-CNRS, Jumana Boussey from LTM Grenoble for the nanoimprint lithography samples, Henri Schneider, Jean-Pierre Laur and Emmanuel Scheid from LAAS-CNRS for their helpful advice.

VII. References

[1] G. He, L. Zhu, Z. Sun, Q. Wan and L. Zhang, "Integrations and challenges of novel high-k gate stacks in advanced CMOS technology,"*Progress in Materials Science,* vol. 56, 2011, pp. 474-572.

[2] R. Ulrich and L. Schaper, "Materials options for dielectrics in integrated capacitors," in *Proc. Int. Symp. Adv. Packag. Mater.*, 2000, pp. 38-43.

[3] M. Thomas, A. Farcy, N. Gaillard, C. Perrot, M. Gros-Jean, I. Matko, M. Cordeau, W. Saikaly, M. Proust, P. Caubet, E. Deloffre, S. Crémer, S. Bruyère, B. Chenevier, and J. Torres, "Integration of a high density Ta_2O_5 MIM capacitor following 3D damascene architecture compatible with copper interconnects,"*Microelectron. Eng.*, vol. 83, no. 11/12, 2006, pp. 2163–2168.

[4] K. B. Jinesh et al, "Enhanced electrical properties of atomic layer deposited La_2O_3 thin films with embedded ZrO_2nanocrystals,"*Applied Physics Letters,*vol. 93, 2008, p.172904.

[5] S. W. Lee, O. S. Kwon, J. H. Han and C. S. Hwang, "Enhanced electrical properties of SrTiO3 thin films grown by atomic layer deposition at high temperature for dynamic random access memory applications,"*Applied Physics Letters,*vol. 92, 2008, p. 222903.
[6] J. Sigman, G. L. Brennecka, P. G. Clem, and B. A. Tuttle, "Fabrication of Perovskite-based high-value integrated capacitors by chemical solution deposition,"*J. Amer. Ceram. Soc.*, vol. 91, no. 6, 2008, pp. 1851-1857.
[7] B.H. Ma, S. Tong, M. Narayanan, S.S. Liu, S. Chao and U. Balachandran, "Fabrication and dielectric property of ferroelectric PLZT films grown on metal foils," *Materials Research Bulletin,*vol. 46, no. 7, 2011, pp. 1124-1129.
[8] P. Jain, E.J. Rymaszewski, "Embedded thin film capacitors – Theorical limits,"*IEEE Trans. Adv. Packag.,* vol. 25, 2002, pp. 454.
[9]S.J. Ding, H.F. Lim, S.J. Kim, X.F. Yu, C.X. Zhu, M.F. Li, B.J. Cho, D.S.H. Chan,S.C.Rustagi, M.B. Yu, A. Chin and D.L. Kwong, *IEEE Electron. Dev. Lett.,* vol. 25, 2004, p. 681.
[10] W. Li, Z. Chen, R. N. Premnath, B. Kabius and O. Auciello, "Controllable giant dielectric constant in AlOx/TiOynanolaminates,"*J. of Appl. Phys.,* vol. 111, 2011, p. 024106.
[11] G. Gatalan, D. O'Neill, R.M. Bowman and J.M. Gregg, Relaxor features in ferroelectric superlattices: A Maxwell-Wagner approach, *App. Phys. Lett.*, vol. 77, 2000, p. 3078.
[12] J.H. Klootwijk, K.B. Jinesh, F. Roozeboom, "MIM in 3D: Dream or reality?,"*Microelectron.Engin.,*vol. 88, 2011,pp. 1507-1513.
[13] J-C. Woo, Y-S. Chun, Y-H.Joo and C-Il Kim, "Low leakage current in metal-insulator-metal capacitors of structuralAl2O3/TiO2/Al2O3 dielectrics,"*Appl. Phys. Lett.,* vol. 100, 2012, p. 081101.
[14] V. Mikhelashvili, G. Eisenstein, A. Lahav, "High capacitance density metal-insulator-metal structure based on Al2O3-HfTiO nanolaminate stacks,"*Appl. Phys. Lett.,* vol. 90, no. 1, 2007, p. 013506.
[15] V. Lehmann, W. Hönlein, H. Reisinger, A. Spitzer, H. Wendt, and J. Willer, "A novel capacitor technology based on porous silicon,"*Thin Solid Films*, vol. 276, no. 1/2, 1996, pp. 138-142.
[16] F. Roozeboom, R. J. G. Elfrink, T. G. S. M. Rijks, J. F. C. M. Verhoeven, A. Kemmeren, and J. E. A. M. van den Meerakker, "High-density, low loss MOS Capacitors for Integrated RF decoupling," in *Proc. Int. Symp. Microelectron.*, 2001, pp. 477-483.
[17] M. Nongaillard, F. Lallemand, B. Allard, "Design for manufacturing of 3D capacitors," *Microelectronics Journal*, vol. 41, 2010, p. 845-850.
[18] F. Roozeboom, J.H. Klootwijk, J.F.C. Verhoeven, F.C. van den Heuvel et al., "ALD options for Si-integrated ultrahigh-density decoupling capacitors in pore and trench designs," *Trans. on Electrochem. Soc.,* vol. 3, no. 15, 2007, pp. 173-181.
[19] M. Brunet, H. MafhozKotb, L. Bouscayrol, E. Scheid, M. Andrieux, C. Legros, S. Schamm-Chardon, "Nanocystallized tetragonal metastable ZrO_2 thin films deposited by metal-organic-chemical vapor deposition for 3D capacitors," *Thin Solid Films*, vol. 519, 2011, pp. 5638-5644.
[20] M. Kemell, M. Ritala, M. Leskelä, E. Ossei-Wusu, J. Carstensen, H. Föll, "Si/Al_2O_3/ZnO:Al capacitor arrays formed in electrochemically etched porous Si by atomic layer deposition,"*Microelectron. Engin.,*vol. 84, 2007, pp. 313-318.
[21] S.W. Lee, O. S. Kwon, J. H. Han and C. S. Hwang, "Enhanced electrical properties of SrTiO3 thin films grown by atomic layer deposition at high temperature for dynamic random access memory applications," *Appl. Phys. Lett.,* vol. 92, 222903, 2008.
[22] J. H. Klootwijk, K. B. Jinesh, W. Dekkers, J. F. Verhoeven, F. C. van den Heuvel, H.-D. Kim, D. Blin, M. A. Verheijen, R. Weemaes, M. Kaiser, J. Ruigrok, and F. Roozeboom, "Ultrahigh capacitance density for multiple ALD-grown MIM capacitor stacks in 3-D silicon,"*IEEE Electron Device Lett.*, vol. 29, no. 7, 2008, pp. 740-742.
[23] Franck Murray, *International Microelectronics and packaging society, 8th international Conference and Exhibition on Device Packaging*, April 2012.
[24] C. Ahrens, A. Geiselbrechtinger,W. Hartung, C. Herzum and R. Losehand, "Capacitor and method for producing a Capacitor",*Patent no 7030457 B2,*
[25] J. I. Sohn, Y-S.Kim, C. Nam, B. K. Cho and T-Y.Seong, "Fabrication of high-density arrays of individually isolated nanocapacitors using anodic aluminum oxide templates and carbon nanotubes,"*Appl. Phys. Lett.*, vol. 87, 2005, p. 123115.
[26] S-W.Chang, J. Oh, S. T. Boles and C. V. Thompson, "Fabrication of silicon nanopillar-based nanocapacitor arrays,"*Appl. Phys. Lett.,*vol. 96, 2010, p. 153108.
[27] C. C. BofBufon, J. D. Cojal Gonzalez, D. J. Thurmer, D. Grimm, M. Bauer and O. G. Schmidt, "Self-assembled ultra-compact energy storage elements based on hybrid nanomembranes,"*Nanoletters*, vol. 10, 2010, pp. 2506-2510.
[28] P. Banerjee, I. Perez, L. Henn-Lecordier, S. B. Lee and G. W. Rubloff, "Nanotubular metal-insulator-metal capacitor arrays for energy storage,"*Nature Nanotechnology*, vol. 4, 2009, pp. 292-296.
[29] L. C. Haspert, S. B. Lee and G. W. Rubloff, "Nanoengineering strategies for Metal-Insulator-Metal electrostatic nanocapacitors," *Nano,*vol. 6, vo. 4, 2012, PP. 3528-3536
[30] A.K. Jonscher, "Dielectric relaxation in solids", *Chelsea Dielectrics Press*, 1983, 380 p.
[31] Marion Matters-Kammerer, "Trench capacitor device suitable for decoupling applications in high-frequency operation," *US Patent WO 7,839,622 B2*, Nov. 2010,
[32] M. Brunet, P. Dubreuil, E. Scheid, J-L. Sanchez, "Development of fabrication techniques for high-density integrated MIM capacitors in power conversion equipment," *SPIE MOEMS-MEMS Symposium, in Photonics West*, January 2006.
[33] P. Artillan, M. Brunet, D. Bourrier, J.P. Laur, N. Mauran, L. Bary, M. Dilhan, B. Estibals, C. Alonso, J.L. Sanchez**, "**Integrated LC filter on silicon for DC-Dc converter applications,"*IEEE Trans on Power Electron.,* vol. 26, No. 8, August 2011, pp. 2319-2325.
[34] A. Geiselbrechtinger, K. Buyuktas, K-H.Allers, W. Hartung, "A high-performance trench capacitor integrated in a passive integration technology," *Semicond. Sci. Technol.*,vol. 24, 2009, p. 015010.
[35] Gordon Grivna et al; *Power Supply on Chip 08 workshop*, Sept 22-24 2008, Cork, Ireland.
[36] J-L. Sanchez, A. Bourennane, M. Breil, P. Austin, M. Brunet, J-P. Laur, F. Morancho, 'A brief overview of silicon active and passive power devices technologies : potentialities of evolving towards 3D heterogeneous functional integration,'' *Internation. Sem. on Power Semicond. (ISPS) Conference*, 2010.
[37] S. Abedinpour, B. Bakkaloglu and S. Kiaei, "A multistage interleaved synchronous buck converter with integrated output filter in 0.18 µm SiGe process," *IEEE Trans. on Power Electron.,* vol. 22, no.6, Nov. 2007, pp. 2614-2175.
[38] M. Wens and M. Steyaert, "An 800mW fully-integrated 130nm cmos dc-dc stepdown multi-phase converter, with on-chip spiral inductors and capacitors," in *IEEEEnergy Conversion Congress and Exposition (ECCE=),*sept.2009, pp. 3706 –3709.
[39] M. D. Seeman, V. W. Ng, H-P. Le, M. John, E. Alon, S. R. Sanders, *IEEE workshop on Control and Modeling for Power Electronics(COMPEL),* 28-30 june 2010
[40] L. Chang, R. Montoye, B. Ji, A. Weger, K. Stawiasz and R. Dennard, "A fully integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3 A/mm²," *in IEEE Symp. VLSI Circuits Dig.*, June 2010, pp. 55-56.
[41] F. Capy, J.P. Laur, M. Breil, F. Richardeau, M. Brunet, E. Imbernon, A. Bourennane, C. Caramel, P. Austin, J.L. Sanchez., "New self-controlled and self-protected IGBT based integrated switch", *ISPSD 09*, Barcelona, June 2009.
[42] H. Lee, Y-S. Choi, E. Song, K. Choi, T. Cho and S. Kang, "Power delivery Network Design for 3D SIP Integrated over silicon interposer platform,"*IEEE Electron. Comp. and Technol. Conf. (ECTC),* 2007, pp. 1193-1198.
[43] B. Dang, S. L. Wright, P. Andry, E. Sprogis, S. Ketkar, C. Tsang, R. Polastre, J. Knickerbocker, "3D Chip Stack with Integrated Decoupling Capacitors,"*IEEE Electron. Comp. and Technol. Conf. (ECTC),* 2009.
[44] K. Ishida, K. Takemura, K. Baba, M. Takamiya, T. Sakurai, "3D stacked buck converter with 15 µm thick spiral inductor on silicon interposer for fine-grain power-supply voltage control in SIP's,"*3D systems integration conference (3DIC),* 2010 IEEE international, 16-18 nov. 2010, Tokyo, p. 1-4
[45] H.J. Bergveld, R. Karadi and K. Nowak, "An inductive down converter system-in-package for integrated power management in battery-powered applications*", IEEE Power Electronics Specialists Conference (PESC)*, 2008, pp. 3335-3341
[46] A. Shibuya, A. Ouchi and K. Takemura, "A silicon interposer with and integrated $SrTiO_3$ thin film decoupling capacitor and through-silicon vias,"*IEEE Trans. on Comp. and Pack. Tech.*vol.33, no. 3, september 2010.
[47] J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel, R. J. Polastre, K. Sakuma, et al., "Three-dimensional silicon integration,"*IBM J. Res & Dev.,*vol. 52, no. 6, Nov 2008, pp. 553-569.
[48] V. Lehmann, U. Grüning, "The limits of macropore array fabrication", Thin Solid Films, vol. 297, 1997, pp. 13-17.
[49] P. Kleimann, X. Badel, J. Linnros, "Toward the formation of three-dimensional nanostructures by electrochemical etching of silicon", *Appl. Phys. Lett.*vol. 86, 2005,p. 183108.
[50] P. Kleimann, J.Linnros, R. Juhasz, "Formation of three-dimensional microstructures by electrochemical etching of silicon", *Appl. Phys. Lett.*vol. 79, 2001,p. 1727.
[51] G. Laffite, M. Roumanie, C. Gourgon, C. Perret, J. Boussey, P. Kleimann, "Formation of submicrometer pore arrays by electrochemical etching of silicon and nanoimprint lithography,"*J. of Electrochem. Soc.,*vol. 158, no. 1, 2011, D10-D14.