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NVM cell degradation induced by femtosecond laser backside irradiation for reliability tests

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***Abstract*—In this paper we present the behavior of a single nonvolatile Flash floating gate memory cell when it is irradiated, from the backside, by femtosecond laser pulses. For the first time we show that the memory cell state can change using this type of stimulation. The measurements were carried out with an experimental setup with an *ad hoc* probe station built around the optical bench. We present the experimental results using different memory bias conditions to highlight the charge injection in the floating gate. Then, we study the cell degradation to check the state of the tunnel oxide and the drain-bulk junction. The aim is to understand the failure mechanisms and use this technique for accelerated reliability tests. Finally we report the experimental results achieved for different laser energies.**

***Index Terms*—Flash memory cells, laser, semiconductor device reliability.**

I. INTRODUCTION

The market of the smart connected objects is growing up driven by the incessant ideas of the new worldwide startuppers and developers. The silicon founders need to find new very reliable and low cost solutions in order to provide high performance electronic circuits for the embedded applications [1]. In this context the nonvolatile memories (NVM) play a key role for the systems on chip (SoC) [2].

Several papers are presented in literature concerning the effect of heavy ion and laser irradiation on NAND Flash memories to investigate the presence of current spikes [3, 4] and in CMOS circuits to inspect the mechanism for simultaneous charge collection [5, 6, 7]. Others studied the effects induced by static photoelectric laser stimulation (1064 nm) on a 90 nm technology metal–oxide–semiconductor (MOS) capacitor [8]. Moreover we found some studies dealing with SRAM cells exposed to pulsed photoelectrical laser stimulation, for applications in modeling and cell characterization [9]. Nevertheless, in our investigations the temperature effects can be neglected [10] and the evolution of the threshold voltage of single memory cells only depends on the charge injection and on the cell degradation. In addition, we irradiate the device from the backside through silicon thanks to an appropriate working wavelength [11].

In this paper we show for the first time, to our knowledge, the effects of a femtosecond laser beam on a single isolated nonvolatile Flash floating gate memory cell. The understanding of cells' behavior under backside laser irradiation will enable the development of special failure analysis techniques. The study of cell degradation can be compared to the results obtained during the classical electric tests, in order to reproduce faster experiments in-line during the fabrication process of semiconductor devices. This technique can be used in the failure analysis in-line tests, or after the fabrication as a parametric measurement, improving the investigation time, or to emulate radiative effects on NVM.

In the first paragraph we will present the femtosecond laser source and the tested devices. The dedicated experimental setup enables to carry out electrical characterization of capacitors, transistors and floating gate memory devices, while the laser irradiation is applied. The robustness of the setup will improve the quality of the electrical results.

After this part, we will show the results of a backside femtosecond laser irradiation on the programmed and erased Flash floating gate memory cells. We report the main effects of cell degradation on the drain current versus gate voltage (Id-Vg) electrical characteristic. Moreover we demonstrate that it is possible to switch the memory state without any electrical intervention.

This work has been carried out thanks to the support of the A*MIDEX project (n°ANR-11-IDEX-0001-02) funded by the "Investissements d'Avenir", French Government program, managed by the French National Research Agency (ANR).

In order to explain the failure mode we carried out some measurements on transistors and capacitors. The results show that the degradation of the drain-bulk junction is faster than the damaging of the tunnel oxide. The junction degradation is gradual and can be destructive for the storage cell. This is a crucial point for a memory device based on the charge injection mechanism. Finally, some experimental data involving a change in irradiation energy of the laser beam are reported. The novelty of these experimental results is in agreement with very last fundamental studies on femtosecond laser interaction with silicon substrates [12].

II. EXPERIMENTAL DETAILS

A. *Measurement setup*

The experimental setup employed to irradiate the cells from the polished rear surface of the silicon wafer is schematically depicted in Fig. 1a. It consists in a customized inverted microscope in which an infrared femtosecond laser beam is injected. The illumination source is based on a titanium-sapphire laser producing femtosecond pulses at 800 nm with 1 kHz repetition rate. An optical parametric amplifier (OPA) converts the laser wavelength to 1300 nm in order to access the transparency domain of silicon.

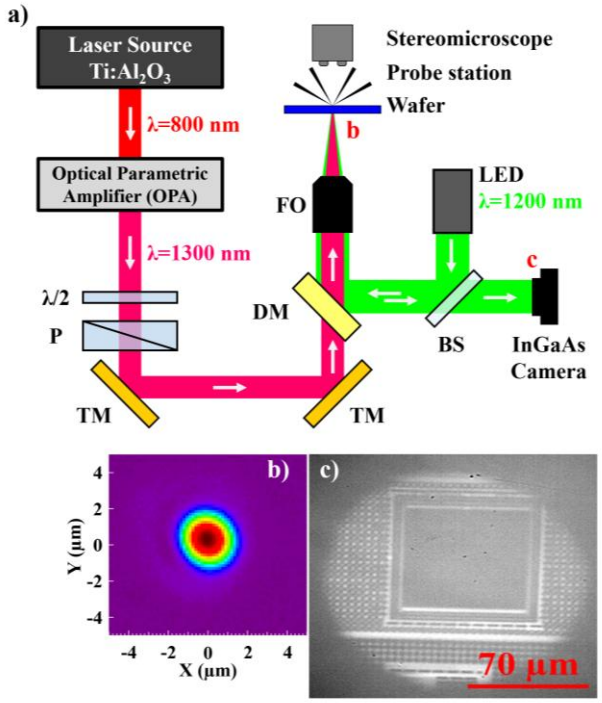


Figure 1. a) Schematic description of the experimental setup. λ/2: half-wave plate, P: polarizer, TM: transport mirror, DM: dichroic mirror, FO: focusing objective, LED: light-emitting diode, BS: beam splitter. b) The spatial shape of the beam measured at the focus in air, and c) a typical image recorded by the InGaAs camera.

The pulse duration is about 100 fs as measured using a single-shot autocorrelator (TiPA AT5C3, Light Conversion). The energy on the sample is adjusted between 12.5nJ and 450nJ, in these experiments, by means of a half-wave plate (λ/2) and polarizer (P) combination. The beam is focused on the cells using a focusing objective (FO) of 0.42 numerical aperture (NA) leading to near-Gaussian spots of about 3µm diameter (at $1/e^2$) as shown in the Fig. 1b. The FO is mounted on a motorized-stage along the Z axis (optical axis) and the wafer is placed on precision stages allowing its displacement in the (X,Y) plane. Accordingly, the focal region can be positioned with micrometer precision anywhere in the 3D space inside the wafer. For observations and positioning through the silicon substrate, we rely on a customized-microscopy system using the same objective as that for laser focusing. The system is based on a light-emitting diode (LED) at 1200 nm for illumination and an InGaAs camera for imaging. Finally, a dichroic mirror (DM) that transmits the laser beam at 1300 nm and reflects the light at 1200 nm is used so that we can simultaneously irradiate and observe the interactions (Fig. 1c). Additionally to the laser setup designed for backside irradiations of cells, a probe station placed on the frontside of the wafer enables us to measure the electrical properties of the flash memories before and after each laser pulse. It consists in a four-terminal sensing connected to the control gate, the drain, the source and the bulk of the Flash memory cell with the help of visualization by a stereomicroscope. The four terminals are connected to a precision semiconductor parameter analyzer (Agilent 4156C) measuring the drain current (Id) as a function of the applied control gate voltage (Vg).

There are unique advantages of using tightly focused femtosecond pulses at 1300 nm to study the reliability of microelectronic devices. First, pulses with extremely modest energies (a few tens or hundreds of nJ) can create high free-carriers densities (up to 10^{19} cm^{-3} [13]) inside silicon by two-photon ionization [14]. Second, the nonlinear nature of ionization confines the free-carrier injection and the potential consequences to a volume that can be smaller than the optical focus. Third, the impossibility to deposit in the bulk of silicon an intensity which is sufficient to reach the critical density has been demonstrated very recently [12], and prevents the material from any permanent modification (e.g., laser-induced damage). Taken together, the electrical properties of the flash memory cells can be changed locally with an extremely low thermal budget inducing no alteration of the medium in which the laser beam propagates. The laser method can be used to emulate the effects of other types of ionizing radiations [15, 16] because the total ionizing dose can be easily varied in the laser experiments (with the energy and number of applied pulses). Finally, the radiation tolerance levels can be derived.

B. *Description of test devices*

In this experimental work, the investigated device is a Flash floating gate memory cell (F.G.) conceived for embedded low energy applications. The F.G. transistors were integrated on 200 mm wafers using a standard 90 nm NOR flash technology node. In Fig. 2a a TEM (Transmission Electron Microscopy) image of the F.G. memory cell is shown. A 10nm tunnel oxide (TUN_{OX}) is grown on a p-type silicon substrate, while an Oxide/Nitride/Oxide (ONO) inter-poly dielectric stack layer is used to isolate the control gate and the floating gate. The width and length of the studied cell are 90nm and 180nm respectively.

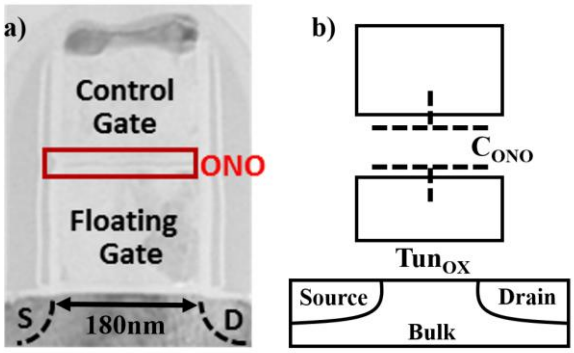


Figure 2. a) Transmission Electron Microscopy (TEM) picture of tested Flash floating gate memory cell. The control gate and the floating gate are isolated by the Oxide/Nitride/Oxide (ONO) interpoly dielectric layer. b) Schematic of memory cell where the tunnel oxyde (TUN_{OX}) and the interpoly ONO capacitance are highlighted.

The backside wafer surface has been polished for not disturbing the light propagation due to surface roughness. In Fig. 2b a schematic representation of the memory device is shown. The presence of the interpoly dielectric layer is indicated by the ONO capacitance (C_{ONO}) that is a fundamental parameter for the charge injection in the floating gate [17], and it will be used below to explain the mechanism of charge injection during the laser irradiation.

III. Observations of Laser Effect

In order to study the effects of backside laser irradiation on the Flash memories, we prepared some samples in programmed and erased state by using standard electrical pulses. The reading operation was performed by using the 4156C parameter analyzer. The two stable states of a floating gate memory cell depend on the quantity of charge Q_{FG} trapped in the floating gate [18]. The threshold voltage (Vt) is defined as follows:

$$Vt = Vt_0 - Q_{FG}/C_{ONO} \quad (1)$$

where Vt_0 is the memory threshold voltage when no charges are present in the floating gate. To read our devices we carried out drain current-control gate voltage (Id-Vg) characteristics and extracted the threshold voltage (Vt) as the value of the gate voltage at fixed drain current value (Id=1µA). The difference between the thresholds of the programmed and the erased states of a cell is defined as the programming window.

A. Impact of laser irradiation on nonbiased memory

In Fig. 3 the evolution of the drain current versus the control gate voltage, depending on the number of applied laser pulses, is shown for an initially erased single cell. The laser energy (E) was kept constant at 0.1µJ. The Id-Vg characteristic is performed without laser irradiation and shifts after just 3 laser shots. We can notice that while increasing the number of shots, the cell is sequentially programmed. The shifts of the characteristics tend to saturate as more electrons reach the floating gate. A high number of energetic electron/hole pairs is generated in the cell substrate and at the bulk/TUN_{OX} interface. The charges are thus attracted by the vertical electric field that is induced by the floating gate potential (Vfg). Moreover, an increasing of the leakage current for the lowest gate voltage values is highlighted as well as the degradation of the drain current level measured for a control gate voltage of 10V (I_{10V}).

This latter, can be associated to a degradation of the bulk/TUN_{OX} interface or to the degradation of the drain(source)/bulk junction. On the contrary, if the memory cell is initially programmed (floating gate charge with electrons), the threshold voltage slightly decreases before the cell degradation starts (Fig. 4). After a burst of 1k laser irradiations, we note the same failure mechanism as the erased cell.

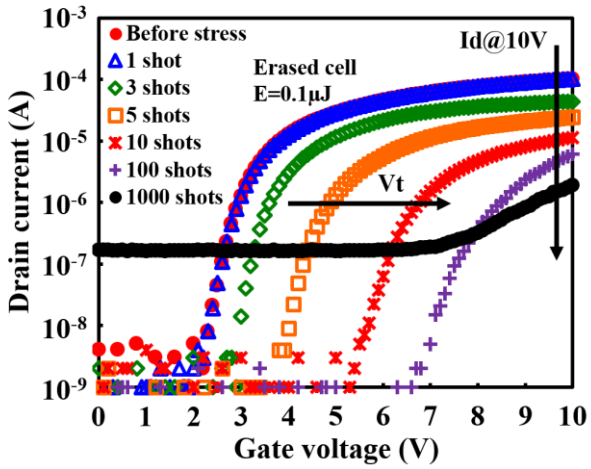


Figure 3. Evolution of the drain current versus control gate voltage characteristics for an erased memory cell after cumulative laser shots (E=0.1µJ).

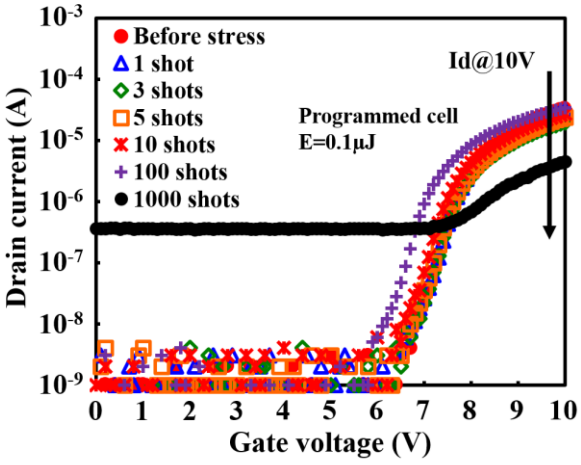


Figure 4. Evolution of the drain current versus control gate voltage characteristics for a programmed memory cell after cumulative laser shots (E=0.1µJ).

In order to explain the different behavior of the single cell under the laser stress depending on the initial memory state, the physical mechanisms involved in our experiments are investigated.

Firstly, the interaction between a femtosecond pulse and silicon results in the production of a plasma by a two-photon ionization mechanism [14]. The number of electron/hole pairs is given by the electron density of the plasma which can be estimated to be on the order of 10^{19} cm^{-3} in our experiments [12, 13]. Let us first assume that the laser-generated electrons in the floating gate are responsible for the change in the Id-Vg curves in Figs. 3 and 4. The electron/hole pairs induced during the laser pulse of about 100fs will recombine in a few nanoseconds [19], and the plasma has completely disappeared during the *post-mortem* electrical measurements.

In other words, no change in the Id-Vg curves should be measured, which is contradictory with Figs. 3 and 4. Thereby, these electrical modifications necessarily originate from an excess of electrons (or holes) produced in another layer which have reached the floating gate. It is worth noting that both the tunnel oxide and the ONO have a wide band gap preventing from an ionization sufficient for modifying the electrical properties of the Flash memory. Hence, the most likely candidate for playing the role of the ionized medium is the bulk.

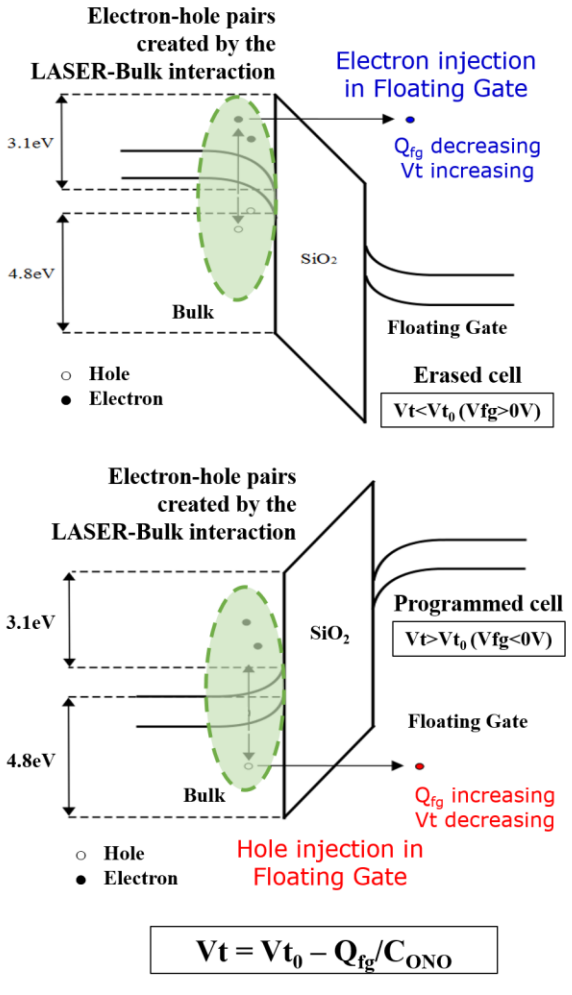


Figure 5. Band diagram schematics of an erased (top) and programmed (bottom) floating gate memory cell during a femtosecond backside laser irradiation.

In order to examine in details the potential migration of the particles from the bulk towards the floating gate, we reported in Fig. 5 a simplified band diagram of the device structure for both situations. When the cell is in the erased state, the floating gate potential is positive, which attracts the energetic electrons present in the substrate. The energy barrier seen by the electrons in this case is 3.1eV. On the other hand, when the cell is programmed the floating gate is full of electrons (Vfg<0V) and the holes are attracted. In this case the holes in the substrate have to tunnel a barrier of 4.8eV, decreasing the injection probability in the floating gate.

Since the electron/hole pairs are produced both in the bulk and the floating gate, the evoked tunnel mechanism cannot explain the experimental results alone. Indeed, the probability that a particle tunnels from the floating gate to the bulk is identical to the one in the other direction. The change in the Id-Vg curves shown in Fig. 3 and Fig. 4 can thus be attributed to the reflections at the silicon/tunnel oxide interfaces which decrease significantly (> 31%) the laser intensity between the bulk and the floating gate. Thereby, the number of electron/hole pairs is higher in the bulk than in the floating gate, and more carriers can tunnel downstream the laser flux. These static measurements, without biasing, show the first results of Flash cell Id-Vg characteristics variation due to the femtosecond backside laser irradiation. Hence, for the parametric failure analysis tests it is important to extract the main parameters that can describe the cell behavior. In relation with Fig. 3 and Fig. 4, we plot in Fig. 6a) and b) respectively the threshold voltage and the drain current measured at Vg=10V after a cumulative stress.

These two main parameters can represent the flags to indicate the level of degradation of a memory cell, before the breakdown. Two different devices are tested, one to extract the parameters of the programmed cell and another for the erased. One can notice that the programming window is closed after 10 laser shots using an energy of 0.1µJ.

While the threshold voltage quickly increases for the erased cells, its decrease is slower for programmed cells, as explained before. This also impacts the drain current at Vg=10V, showing a higher degradation level for the erased cell. In the next section, we will demonstrate that the Vt shift is due to the electron injection in the floating gate.

B. Effect of control gate bias

In this section we will study the behavior of a single cell after laser irradiation while its control gate is biased. The aim of this experiment was to demonstrate that the charge injection in the floating gate is related to the vertical electric field present in the tunnel oxide during the generation of electron/hole pairs.

In Fig. 7 we report the results of these measurements. We plot the erased threshold voltage evolution versus the number of irradiation shots. In the inset a schematic of memory cell polarization is presented. We compared to the standard case, when all the terminals are floating, two different situations: when Vg=+3V and Vg=-3V, starting from an erased cell. In the first case (Vg=+3V), the external electric field, imposed by the control gate biasing, matches the internal electric field

resulting from the floating gate potential in terms of direction. The threshold voltage shift is thus accelerated with respect to the standard floating condition. On the contrary, when Vg=-3V, the external electric field is opposite to the internal field and the probability to inject the electrons in the floating gate is decreased. Hence, the maximum threshold voltage shift is 2.6V. For all these cases, we note that the threshold voltage shift increases at the beginning of irradiation, and tends to saturate when the presence of negative charges in the floating gate compensates the effects of the internal and external electric fields, as well as the programming kinetics of standard Flash memory cells [20]. This demonstrates the real charge injection in the floating gate during the laser irradiation that gives energy to the electron/hole pairs generated in the substrate and at the bulk/TUN_{OX} interface.

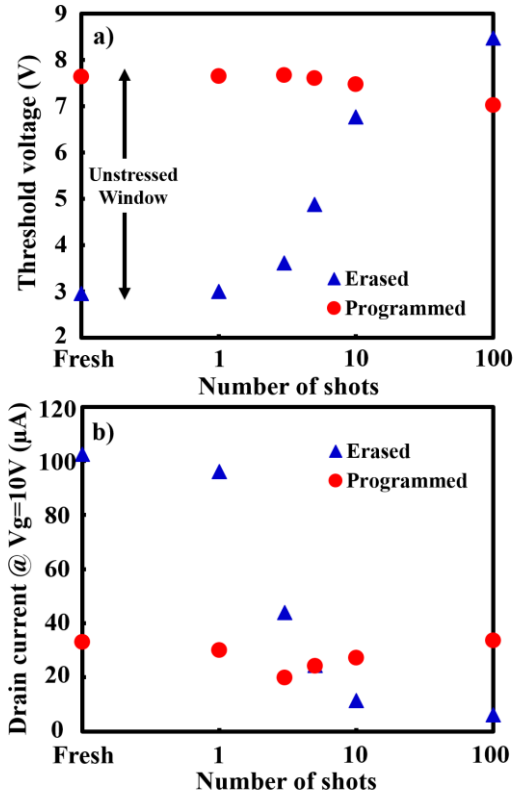


Figure 6. a) Threshold voltage and b) Drain current at Vg=10V evolution during the laser irradiation, measured fot both erased and programmed cells.

IV. FAILURE MECHANISM UNDERSTANDING

To understand the failure mode after the degradation we tested several alternative structures like capacitors and dummy cells on the same wafer of memories. The capacitors had the same oxide as that of memory devices (tunnel capacitors). The tests on this structure will allow to understand if the tunnel oxide is damaged by the laser irradiation. The dummy cells are MOS transistors sharing the architecture of the memory cells but with the control gate and the floating gate connected together. Thanks to this structure, we will carry out some measurements of gate current and drain/bulk junction current, in order to establish where the cell is more damaged.

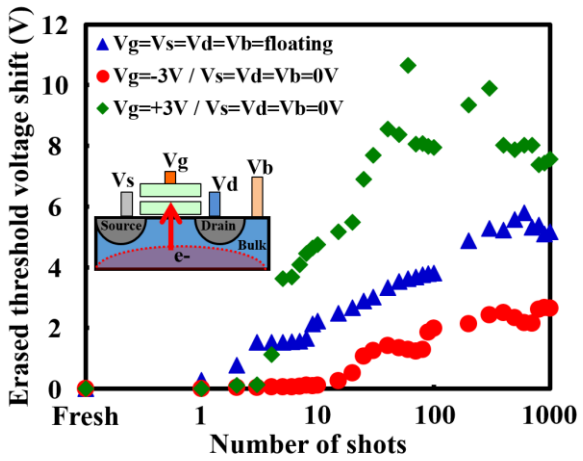


Figure 7. Erased threshold voltage shift as a function of the number of laser shots (E=0.1μJ) for different control gate bias conditions. In the inset a schematic of the irradiated single memory cell is shown.

A. *Effect of laser irradiation on tunnel capacitor*

In Fig. 8 the capacitance-voltage (C-V) and current-voltage (I-V) characteristics of a tunnel capacitor are reported before and after an irradiation of 1000 laser shots using a high energy beam (E=0.45μJ). In accord with [8], the laser effect on C-V curves is not evident after the stress. Moreover, in our case the thermal budget of the femtosecond laser interaction with the substrate and the oxide, is extremely low.

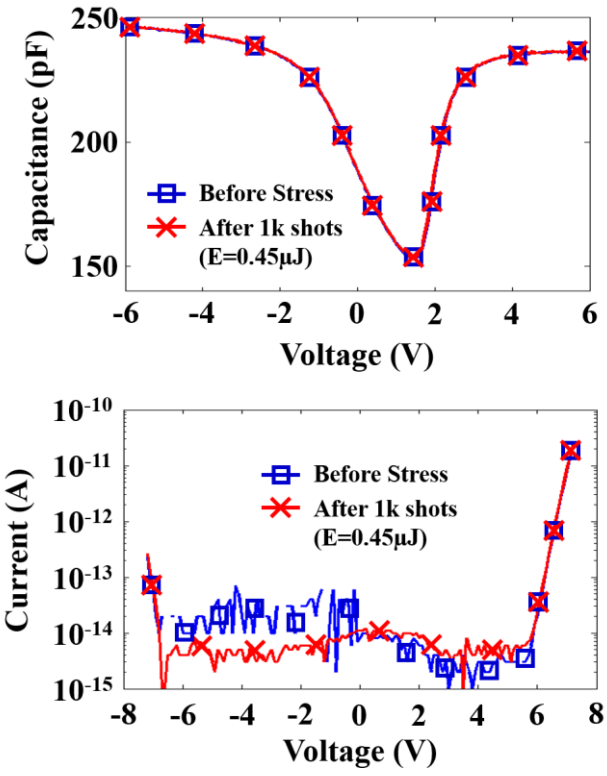


Figure 8. Capacitance-voltage (top) and current voltage (bottom) characteristics of a tunnel capacitor, before and after the laser irradiation.

The differences in the results before and after the stress are insignificant. This leads us to conclude that the tunnel oxide is not damaged in the single memory cell. The current-voltage characteristics confirm a very low tunneling current value through the oxide which preserved its integrity.

B. Dummy cell characterization

In Fig. 9 the gate and drain currents of a single dummy cell are plotted as a function of gate voltage.

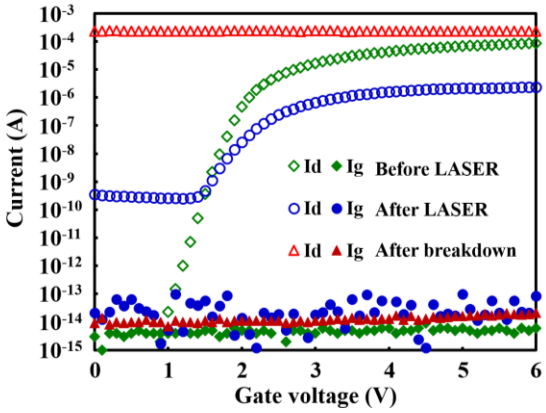


Figure 9. Drain and gate currents versus gate voltage characteristics of a dummy cell before and after laser degradation and after the dummy breakdown. (1k shots at E=0.45µJ).

Laser irradiation is here identical to that used for the experiments on the capacitors (E=0.45µJ). Once again the results confirm the tunnel oxide integrity even after the transistor breakdown as the gate current, indeed, remains very close to the noise level. The Id-Vg characteristics of the dummy cell follow the same trend as that for the memory device, if they are compared to the characteristics in Fig. 3 and Fig. 4. Of course the charge injection is not present because the floating gate is not isolated, but shorted with the control gate. Instead the drain current degradation and the leakage increasing are pushed up to the breakdown. The high value of the drain current in this case leads us to think about the drain/bulk junction degradation.

C. Memory cell drain-bulk junction characterization

To confirm that drain/bulk junction degradation is the main failure mechanism of a Flash floating gate memory cell, we measured the drain-bulk current by biasing only the junction, before and after the laser irradiation. The results presented in Fig. 10 show the drain-bulk current when the forward (Vd<0V) and reversed (Vd>0V) biases are applied on the junction. Before the laser irradiation the reverse current is low, but it increases with the number of laser shots, demonstrating the failure mechanism.

This kind of characteristics are also observed in [21, 22]. Further measurements and analysis are needed to investigate the dopant redistribution due to the laser irradiation. This could enhance the electric field in the spatial charge region of the drain-bulk junction up to the breakdown. The drain and source implants have been made at the same time during the memory fabrication process, so the same effect can be expected.

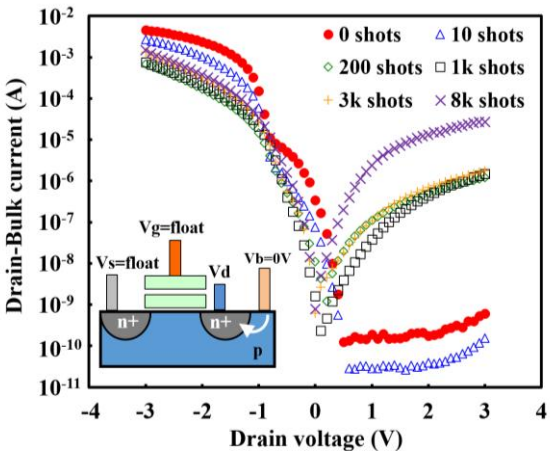


Figure 10. Drain-bulk current as a function of drain voltage with the 0V bulk biasing. The characteristic is carried out after several irradiation shots (E=0.1µJ). The inset is a schematic of memory cell with the bias conditions.

V. DEPENDENCE ON LASER IRRADIATION ENERGY

Finally we carried out a set of measurements on memory cells using different laser energies, in order to evaluate the effect of the latter on cell degradation. The results displayed in Fig. 11 show that there is no significant change in the trend between various energies if we do not take into account the high dispersion likely due to the use of different devices. This is consistent with [12] where it is shown that the delivered maximum intensity in the material (and thus the produced electron density) is independent on the input energy in the tested range. It will be necessary to decrease the laser energy to verify if the oxide degradation can occur before the junction breakdown.

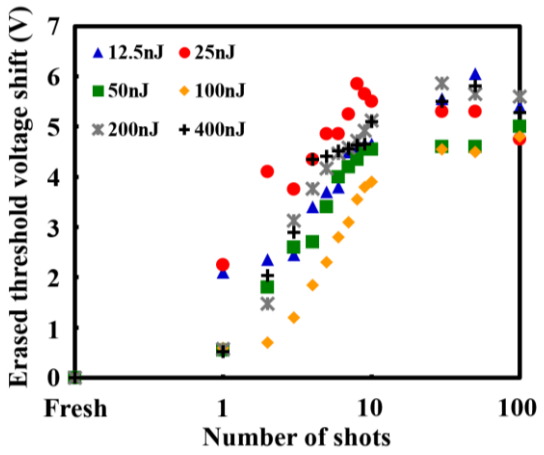


Figure 11. Threshold voltage evolution as a function of the number of laser shots measured for different energies.

CONCLUSION

This work shows for the first time that it is possible to flip or damage a single Flash floating gate memory cell by a femtosecond laser backside irradiation. In particular, an erased cell can be sequentially programmed depending on the number of laser shots. The electric field imposed on the tunnel oxide

by the floating gate potential or the control gate voltage has been shown to enhance charge tunneling during laser irradiation. The electrical characterization on memory devices, capacitors and dummy cells demonstrated that in spite of this charge transit through the tunnel oxide, its degradation level remains low. The main cause of the single memory cell failure mechanism is found to be the drain(source)/bulk degradation. Further studies can be carried out to verify the dopant distribution, close to the junctions, due to the backside laser irradiation. These tests could play a pioneering role in the development of new techniques of failure analysis for in-line tests, or after the fabrication as a parametric measurement, improving the investigation time, or to emulate radiative effects on NVM.

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