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BEOL-investigation on selfheating and SOA of SiGe HBT

R. D’Esposito, S. Fregonese, T. Zimmer

BipAk, Infineon Munich

November 24-25, 2016
Outline

• SiGe HBTs for THz applications
  • Thermal issues in state of the art SiGe HBTs

• Technologies under study: IFX B11HFC and ST B55

• Characterization of BEOL impact in single finger HBTs (IFX B11HFC)

• Physical modeling of the BEOL impact (IFX B11HFC)

• Impact of BEOL and transistor layout in multifinger HBTs (ST B55)

• Conclusions & future perspectives
Temperature issues in SiGe HBTs

High speed performances till sub-THz range

- DTI (poor thermal conductivity)
- Aggressive shrink of the active part
- High current densities
- High internal electric fields at the BC junction

- Can be modeled as a heat source

Serious thermal issues due to self-heating

- Shift and deterioration of the DC and AC characteristics
- Eventually device failure
- Positive electro-thermal feedback => electro-thermal loop

http://users.ece.gatech.edu/cressler/
Scaling and high integration consequences

Device level:
- Multifingered architectures

Circuit level:
- Higher density of components

Scaling increases performances, but leads to higher $J_C$ and thus to higher power densities

INTRA-DEVICE thermal coupling

INTER-DEVICE thermal coupling

Pascal Chevalier, “55nm SiGe BiCMOS for Optical, Wireless and High-Performance Analog Applications” EuMW2015
A high value of $R_{th}$ has a negative impact on the DC behavior: it leads to IC instability.

A high $R_{th}$ decreases the $f_T$ and $f_{MAX}$ figures of merit.
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Technologies under study: IFX B11HFC

130nm MOSFETs (C11) + Scaled SiGe HBTs (DOTFIVE SiGe HBT) + mmWave BEOL

- 7 BEOL metals
  - 4 thin Cu
  - 2 thick Cu
  - 1 Alu for pads

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Technologies under study: ST B55

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9 BEOL metals

- 5 thin Cu
- 2 medium Cu
- 1 thick Cu
- 1 Alu for pads
BEOL metallization evolution

Evolution over time of a CMOS technology node

- The dimensions of the active part of the transistors decreases
- The complexity of the BEOL increases

Akira Tsuchiya (Kyoto University, Japan)
Scenario of the thermal impact of the BEOL

**Thermal conductivity**

- **FEOL Si** → 1.54 W/cm K
- **BEOL SiO₂** → 0.014 W/cm K
- **BEOL Cu** → 3.85 W/cm K

- Can the heat generated at the BC junction be dissipated through the metal stacks above it?
- How much the impact of the added metals on the behaviour of the component?
- Is it possible to model this effect to take it into account into circuit simulator?

**HEAT SOURCE**: BC junction
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Test structures to evaluate BEOL impact

narr test set:
Minimum volume of metal added

wide test set:
More volume of metal added

The metal dummies do not change the electrical connections: emitter is grounded at metal-1 level

Metal added upon the base contacts

B1E1: reference test structure
Test structures for evaluation of the BEOL impact

- E2narr
- E3narr
- E4narr
- E2wide
- E3wide
- E4wide
- B2
- B3

$A_E = (0,34 \times 5) \ \mu m^2$
Δ$I_c$ % increases if the volume of metal increases; if metal is added to base contacts effect is stronger.
Measured $f_T$ and $f_{MAX}$ figures of merit

de-embedding using the same OPEN and SHORT structures

No deterioration in the small signal RF figures of merit is measured

A sensible increment of $f_T$ and $f_{MAX}$ can be observed

$V_{CE}=1.5V$
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Test structures for compact modeling of the BEOL impact

\[ A_E = (0.22 \times 5) \, \mu m^2 \]

M1 test structure

M6 test structure

Electrical connections are unaltered among the two structures
M1 test structure and schematic representation of the Rth

- Rth of the BEOL part is just given by oxide (very high value, $P_d\text{BEOL}$ is negligible)
- Total $P_d$ can be approximated by just the $P_d$ of the lower part
M6 test structure and schematic representation of the $R_{th}$

- Metallization reduces the overall $R_{th}$ of the BEOL part and helps vehicle $P_d$ upwards.

- Total $P_d$ is now split in 2 branches: one flows in the lower part and the other in the BEOL part.
DC current lowers for M6 in the high power dissipation region ($V_{be} \sim 900 \text{mV}$) due to lower Rth ($\sim 10\%$ variation) => better thermal stability
DC measurements and thermal network simulated in HiCuM

M1 test structure

Rth for M1 test structure is verified with dedicated on-wafer measurements

M6 test structure

- Equivalent Rth drops from 4.0kΩ to 3.78kΩ (-5.5%)
Zth extraction using low frequency S-parameters measurements

\[ Z_{TH} = \frac{\frac{dI_c}{dT_j}(I_c + V_{ce}Y_{22\_meas} + V_{be}Y_{12\_iso})}{Y_{22\_meas} - Y_{22\_iso}} \]

Y\(_{22}\) is sensible to dynamic self heating and used for Zth calculation

Y\(_{22}\) that would be theoretically measured if there were no self-heating effects in the component

Rinaldi, “Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis” TED 2001
Low frequency $Y_{22}$ measurements

- Adding metal dummies in the BEOL changes the $Y_{22}$ in the range DC $\rightarrow$ 2~6MHz
- Thermal diffusion is a distributed phenomenon: an infinite number of RC poles is theoretically needed
- Measured $Y_{22}$ in the range 10kHz $\rightarrow$ 500MHz shows **three main slopes**

V$\text{be}$=0.90V  
V$\text{ce}$=1.5V
Proposed thermal network to take into account distributed $Z_{th}$

\[ R_{th_{jn}} = k_r^n R_j \]

\[ C_{th_{jn}} = k_c^n C_j \]

$k_r < 1$

$k_c > 1$

Lower part thermal network
(FEOL up to metal-1)

D’Esposito, S. Fregonese, A. Chakravorty and T. Zimmer, “Dedicated test-structures for investigation of the thermal impact of the BEOL in advanced SiGe HBTs in time and frequency domain” ICMTS 2016
Thermal model for the M1 test structure

BEOL part is neglected for the M1 test structure.

This thermal network takes into account the thermal effect of the FEOL and of the BEOL till metal 1.

Same Rth than DC case is used, but cut into 3 parts.
Thermal model for the M6 test structure

The thermal network of the lower part is kept the same as M1.

2\textsuperscript{nd} and 3\textsuperscript{rd} poles have very high capacitances (big metal volume added).
The $Y_{22}$ parameter is fit nicely for the 2 test structures under study using the proposed thermal networks.

- $V_{BE} = 0.90V$
- $V_{CE} = 1.5V$

- $|Y_{22}|$ versus frequency
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Thermal unbalances in multifinger devices (ST B55)

Thermal coupling in multifinger HBTs:

1) unbalanced temperature distribution
2) hotspot formation
3) current hogging
4) device instability
5) device failure
Proposed alternative finger layouts: HL structures

Reference structure:
VM3
(active part is unaltered)

Non-uniform finger length
HL2

Lower power dissipated on
the central fingers

Emitter segmentation
HL3

Enlarged DTI
HL1

Increased cross section surface for power dissipation

(a) VM test structures
DTI enclosed area = 71.78 μm²
\( A_E = 4.5 \mu m^2 \)

(b) HL1 test structure
DTI enclosed area = 86.83 μm²
\( A_E = 4.5 \mu m^2 \)

(c) HL2 test structure
DTI enclosed area = 71.78 μm²
\( A_E = 3.91 \mu m^2 \)

(d) HL3 test structure
DTI enclosed area = 71.78 μm²
\( A_E = 3.91 \mu m^2 \)
VM structures to evaluate the BEOL impact in multifingers

VM8 dummies till metal-8
VM6 dummies till metal-6
VM3 reference test structure

VM1 just metal-1 is present

The active part of the transistor is not modified, just heat spreaders are added
Electrical connections are unaltered among the different transistor structures
3D representation of the BEOL test structures

5xCBEBEBC architecture

VM8 test structure

Metal dummies connected upon emitter contacts (VM8)

Base connections

Emitter metallization till metal-3: connected to ground plane

Collector connections

ground plane connection (on both sides)
guard ring (in metal-1)
Output curves

Adding metal heatspreaders above the emitters lowers the slope of $I_C$ in the high $P_{diss}$ region.

The increase of the DTI enclosed area allows an even lower slope.

The slope of $J_C$ is even lower for the devices with reduced $A_E$.

Emitter segmentation yields the best electro-thermal performances.

Going from high to low frequencies, the thermal oscillations penetrate till higher metal levels. When the temperature variations will reach metal-1, there will be a split between the $Z_{th}$ of VM1 and VM3.

At low frequency the DTI limits the temperature variations. If it is wider, or if the emitters are smaller $\Rightarrow$ lower $Z_{th}$.
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Conclusions: BEOL impact

- Mechanical stress
- Decrease of $R_{th}$
- Stabilizing effect for $I_C$
- Better RF performances
- The metallization helps to evacuate the heat generated by the transistor
- The metal volume slows down the thermal response and keeps the temperature more stable
- These effect can be modeled on a physical base and simulated
Conclusions: layout modifications

- Modifications in the transistor layout have a stronger electro-thermal impact (DTI enlargement, emitter segmentation)

- In AC the temperature sinusoidal variations penetrate the transistor till different depths according to the frequency

- Changes in the transistor layout mostly induce $Z_{th}$ variations at very low frequencies
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Thank you for your attention!