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Classic and alternative methods of p-type doping 4H-SiC for integrated lateral devices

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Abstract - P-type 4H-SiC layers formed by ion implantation need high temperature process generating surface roughness, losing and incomplete activation of dopants. Due to dopant redistribution and channeling effect, it is difficult to predict the depth of the formed junctions. Vapor-Liquid-Solid (VLS) selective epitaxy is an alternative method to obtain locally highly doped p-type layers in the 10^{20} cm^{-3} range or more. The depth of this p-type layers or regions is accurately controlled by the initial Reactive-Ion-Etching (RIE) of the SiC. Lateral Junction Field Effect Transistor (JFET) devices are fabricated integrating p-type layers created by Al ion implantation or VLS growth. The P-type VLS layers improve the access resistances on the electrodes of the fabricated devices.

Keywords—ion implantation, VLS epitaxial growth, RIE, JFET.

1. Introduction

Power discrete SiC devices as Schottky diodes, Bipolar Junction Transistors (BJT), Junction Field Effect Transistors (JFET) and MOSFET are already commercialized. To improve reliability in power electronics, a monolithic integration of this type of devices in SiC single crystal wafers is recommended. Thus the size of converters is reduced, the switching operation is improved and the power loss is decreased. Monolithic integration of SiC devices was already invoked to build vertical JFET and Junction Barrier Schottky diodes [1] and vertical or lateral BJT [2]. Industrial development of the SiC monolithic technology is still in progress, delayed by the need to improve technological steps, particularly those that can enhance the quality of semi-insulating SiC substrates or that can reduce the resistivity of the p-type layers.

In this paper, for the first time, SiC p-type doping by aluminum (Al) ion implantation is compared to the alternative VLS epitaxy method.

2. Al ion implantation

P-type localized regions in SiC are in general obtained by ion implantation which is still a unique method of local doping due to the very slow diffusion of dopants in SiC. Moreover, due to the high energies of ionization of the p-type dopants in SiC (~0.2 eV for aluminum and ~0.3 eV for boron), obtaining a net doping level requires to implant higher doses of ions. That leads to create numerous crystalline defects up to local amorphisation of the material if the ion implantation is processed at room temperature (RT).

To recover a good crystalline quality and to activate the implanted impurities by migration of implanted ions in SiC atomic substitutional sites (for example, Al is a dopant only when it substitutes to a Si site), a high temperature annealing is necessary, typically in the range of 1600-1800°C [3]. Figure 1a presents sheet resistances (R_{sh}) measured with a four-point probe technique on p-type layers created by Al ion implantation. R_{sh} decreases when either the annealing temperature or the annealing time increases, the linearity of the R_{sh} variations proving a non-saturation of the electrical dopant activation even after annealing at 1800°C [4].

The annealing temperature is limited by the surface deterioration of the implanted layers. A strong degradation of the surface occurs by sublimation of Si from the SiC, resulting in a rough surface. Surface roughness limits device performances by inducing an increase of leakage currents in off-state and a degradation of the breakdown voltages. The roughness increases when either the annealing temperature or the annealing time increases (Fig. 1b) by forming terraces of several tens of nanometers (Fig. 2). By increasing temperature, the sublimation of Si can induce also an etching effect of the SiC surface and thus a significant loss of implanted dopants in the near surface region [5]. Figure 3 presents Al implanted doping profiles measured before and after annealing. Compared to samples just implanted, the Al profiles after annealing seems

to be offset toward the surface. The quantity of the dopant loss increases with the annealing temperature. It is worth mentioning that on these samples the ion implantation was performed at 300°C to avoid SiC amorphization. [6].

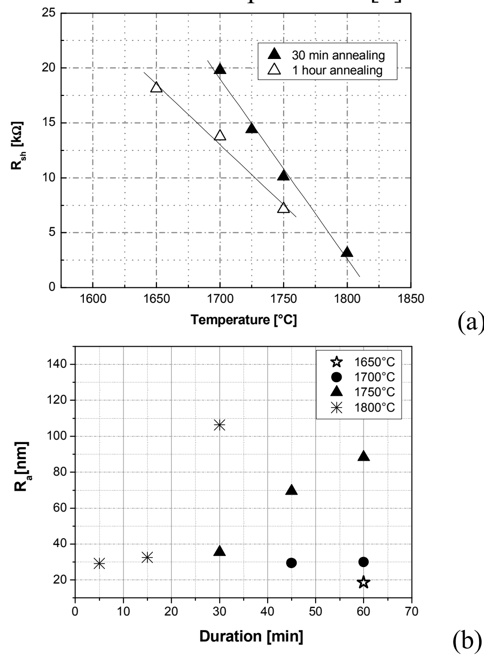

Fig. 1. Sheet resistance measured at RT by four-point probe technique (a) and arithmetic average roughness (R_a) measured with Tencor alpha-step stylus (b) on p-type SiC layers created by Al ion implantation and annealed at different temperatures and durations.

Moreover, losing the implanted dopants should induce an increase of the sheet resistance of the p-type layers which is in contradiction with the results we present in figure 1a where the sheet resistance decreases by increasing the post-implantation annealing temperature. The p-type SiC sheet resistances from figure 1 have been measured on samples whose surfaces were protected with a dedicated cap (detailed hereafter). Therefore, in figure 1a the decreasing of the sheet resistances either with the temperature and the duration of the annealing is fundamentally caused by the increase of the dopants activation.

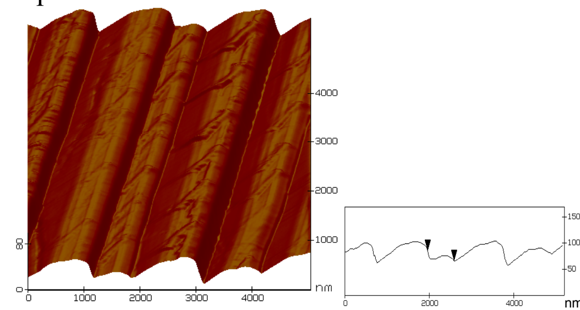

Fig. 2. Atomic Force Microscopy (AFM) image on non implanted SiC sample annealed at 1700°C during 30 min.

Si sublimation has been reported to be prevented by capping the surface with AlN [7], graphite (C) [8] or by using silane partial overpressure during annealing [9]. In this later case an accurate control of the gas flux is necessary to prevent Si droplet deposition. However, the efficiency of these protections is shown to be temperature limited except for the graphite layer which resists up to 1800°C. The graphite cap layer is obtained by baking at ~750°C a photoresist layer deposited by spin-coating at the SiC wafer surface. This method is widely used today in SiC device fabrication needing doping by ion implantation.

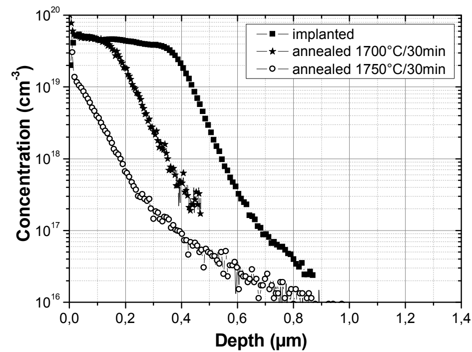

Fig. 3. Al profiles measured by Secondary Ion Mass Spectrometry (SIMS) before and after post-implantation annealing highlighting the loss of the dopants after high temperature annealing.

The C cap showed a very good preservation of the sample surface state. After 1800°C/30 min annealing, the average roughness is 0.46 nm, slightly higher than for an unimplanted sample (0.31 nm) [10]. Nevertheless, the surface morphology after annealing was shown to depend on implantation parameters (temperature and total doses), even when using a graphite cap protection. The use of the graphite cap influences the diffusion of dopants and their activation rate.

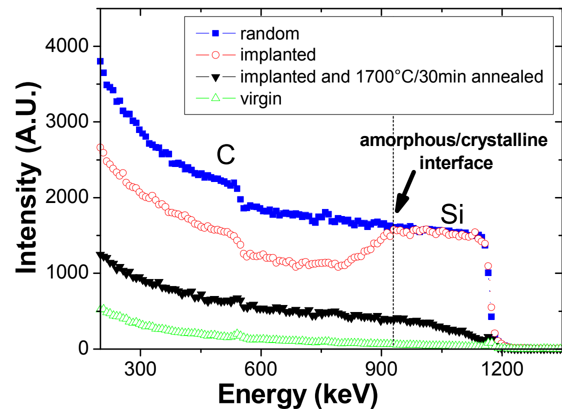

Fig. 4. RBS/C spectra on 4H- SiC samples implanted at RT with 1.75×10^{15}cm^{-2} Al total dose, before and after annealing

When ion implantation is performed at RT, dopant redistribution occurs also during the annealing, by a gettering phenomenon localized at the proximity of the end-of-range defects formed at the initial amorphous-crystalline interface [11]. The presence of the amorphous layers has been identified by Rutherford Backscattering Spectrometry in the channeling mode (RBS/C) measurements. Figure 4 presents the example of the 1.75×10^{15} cm^{-2} Al implanted sample at RT.

After annealing, dopant diffusion increases with the dopant dose. In figure 5 the SIMS (Secondary Ion Mass Spectroscopy) dopants profiles are presented for four total implanted doses after 1700°C/30min annealing. The shape of the dopant profile considerably affects the electrical behavior of devices based on these p-n junctions. Dopant redistribution may have a positive influence on the increase of the p-n junction breakdown voltage. Nevertheless, graduate junctions are in general not compatible with high levels of carrier injection.

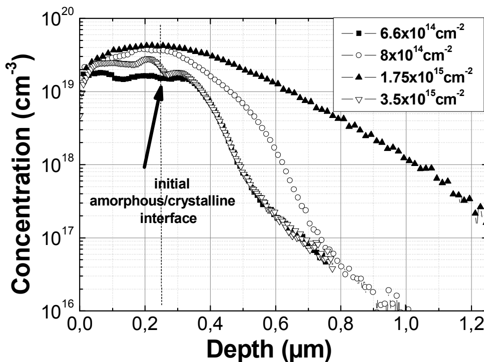

Fig. 5. SIMS doping profiles obtained after annealing on samples implanted Al with varying total doses [11]

Implanted dopants profiles and the depth of the formed junctions are also difficult to be accurately estimated due to the channeling effect. As 4H-SiC presents a hexagonal crystalline structure, a strong channeling effect is observed especially in the case of Al ions. The channeling of the Al ions is quite difficult to control and to eliminate even when an amorphous layer as SiO_2 is present in the surface. Dedicated Monte-Carlo software has been developed considering the crystalline structure of the SiC [12]. Electrical characteristics of the final fabricated SiC devices could be predicted, but with uncertainties due to the difficulty to estimate the depth of the different p-type layers.

3. Vapor-Liquid-Solid Growth

An alternative method to locally dope SiC is Vapor-Liquid-Solid (VLS) selective epitaxy. Highly p-type doped SiC can be obtained leading to considerable reduction of both the p-type SiC resistivity and of the specific resistance of the ohmic contacts formed on it.

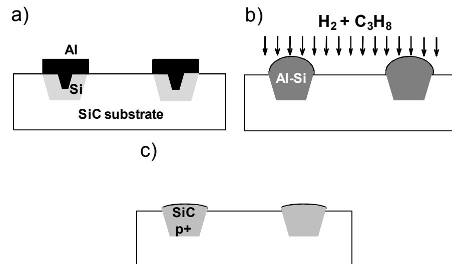

Fig. 6. Schematic description of the VLS process: a) deposition of Al-Si stack inside the trenches formed by RIE in SiC, b) melting of Al-Si and addition of propane for the VLS growth, c) formation of P^+-type SiC [13].

The technological process is detailed in [13] and is schematically presented in Fig. 6. The depth of the p-type layers is accurately controlled by the initial Reactive-Ion-Etching (RIE) of the SiC, performed to create the wells where the Al-Si stacks are deposited and converted in 4H-SiC by VLS epitaxy. The RIE is made with SF_6/O_2 chemistry and using a Ni hard mask defined by photolithography at the surface of the SiC samples.

During the VLS growth the samples are heated in a vertical cold wall reactor up to 1100°C. This value is very low compared to the temperatures needed for post-implantation annealing (~1700°C) or classical CVD epitaxy (~1400°C).

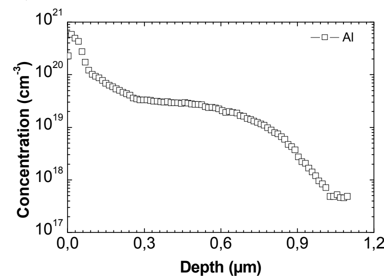

Fig. 7. Al doping profile from SIMS on VLS SiC P^+ layers.

P^+-type SiC layers are obtained by VLS with high Al doping concentrations, in the 10^{20} cm^{-3} ranges. Fig. 7 presents typical profiles obtained by SIMS [14].

Ohmic contacts have been evaluated on these P-type VLS layers with patterned Transfer Length Method (TLM) structures using a specific Ni-Ti-Al metal alloy [15]. The contact is already

ohmic without post-metallization annealing. Specific contact resistances as low as 1.3×10^{-6} $\Omega.cm^2$ have been obtained after 500-800°C Rapid Thermal Annealing [16].

4. Integrated lateral JFETs

Lateral JFET transistors with N-type and P-type channels have been fabricated, integrated monolithically within the same SiC wafer. Several batches have been fabricated, the first one (detailed in [17]) with P^+ wells created by Al ion implantation, and the second one (detailed in [18]) with VLS P^+ wells. The P^+ wells were utilized as source and drain contacting layers for the P-JFET and as P^+ gate for the N- JFET. The N^+ wells have been obtained by nitrogen ion implantation.

For the structure with both P^+ and N^+ wells realized by ion implantation, an experimental study based on SIMS measurements and MC simulations was necessary to consider the channeling effect in the 4H-SiC hexagonal crystalline structure. A technological process has been defined to obtain devices working despite the presence of the channeling effect.

The electrical characteristics of the JFET with P^+ wells created by VLS are affected by the interface between the VLS P^+ gate and the N-type channel, which is a CVD epilayer. The structural defects observed by Transmission Electronic Microscopy explain the high reverse gate/source leakage current measured. Nevertheless, the obtained results have shown that the P^+ VLS layers could already be used to improve the access resistances on the P-JFET transistors where the VLS P^+ layers have been utilized as source and drain.

5. Conclusion

Industrial development of the SiC monolithic technology needs a significant drop of the resistivity of the p-type layers and of the ohmic contact formed on them. A technological breakthrough will be obtained when an alternative method to ion implantation will be found in order to locally dope SiC, using only low-temperature processes, thus preserving the surface state and allowing to precisely predict the junction depths. VLS selective epitaxy is a good candidate for such objectives. If creating reliable P/N junctions by this method seems to be yet premature, highly p-type doped layers and ohmic contacts with specific contact resistances as low as 1.3×10^{-6} $\Omega.cm^2$ have already been obtained by VLS. Therefore we demonstrated that VLS layers could already be utilized on the top of p-type CVD epilayers in order to improve the access resistances.

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