A Voltage Limiter Circuit for Indoor Light Energy Harvesting Applications

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Abstract. A voltage limiter circuit for indoor light energy harvesting applications is presented.This circuit is a part of a bigger system, whose function is to harvest indoor light energy, process it and store it, so that it can be used at a later time. This processing consists on maximum power point tracking (MPPT) and stepping-up, of the voltage from the photovoltaic (PV) harvester cell. The circuit here described, ensures that even under strong illumination, the generated voltage will not exceed the limit allowed by the technology, avoiding the degradation, or destruction, of the integrated die. A prototype of the limiter circuit was designed in a 130 nm CMOS technology. The layout of the circuit has a total area of 23414 μm^2. Simulation results, using Spectre, are presented.

Keywords: CMOS integrated circuits, Energy harvesting, Voltage limiters, Voltage reference circuits.

1 Introduction

To achieve indefinite operation in any location, sensor nodes must obtain their power directly from the environment. In a wireless sensor network, it may be difficult to power each node, either using batteries or the power grid. Sensor networks supplied by grid connections are limited to a small range of applications, as they can never be too far from the power outlet. Although the use of batteries allows for more freedom of sensor distribution, its replacement can become burdensome and costly, if a large number of sensors are deployed. As such, energy harvesting systems tend to take over the powering paradigm for pervasive operation [1], beingalso ecological and thrifty. The sources that can be harvested are diverse [2] and, amongst those, light is the one with the highest energy density per unit of volume [2].Energy can also be obtained from indoor light. In this ambient, powering an electronic application is an increased challenge, as the levels of available light power inside buildings are much lower than those obtained outside. At the most, the Sun can provide about 1 kW/m^2, but in indoor environments, the Sun and the artificial lighting provide a much lower energy density.

2 Relationship to Internet of Things

The circuit presented in this paper is an essential part of an indoor light energy harvesting system. This energy harvesting will allow a variety of electronic systems to operate indoors without needing batteries or a connection to the power grid, adding an enormous degree of freedom, regarding their location. These electronic systems can communicate with other devices and, ultimately, connect to the Internet. The light energy source, when compared to other sources, has the highest energy density, making the harvester discreet and small. Light energy harvesters are simple and cheap to build. As long as light is available, any device supplied by energy harvested from ambient light can be deployed to anywhere, making it a part of the Internet of Things.

3 Motivation and Background

The unpredictable nature of light energy, results in a variable amount of available power. Since the PV cells must be sized in order for the energy harvesting system to be able to receive enough energy even when the light intensity is weak, this can result in large power, available from the same PV cells, when the light intensity is strong. The circuit described in this paper, fits in a system designed to deal with very low levels of light energy, typically found in indoor environments. However, when this system is illuminated by direct sunlight or generally, by high levels of light intensity, the energy harvested by the PV cells is much higher than the value that was expected under the normal indoor illumination conditions. In this situation, the energy harvesting system must be able to manage the excess of energy that is obtaining.

The architecture of the system is depicted in Fig.1,being constituted by PV cells followed by a voltage step-up converter with MPPT capability.

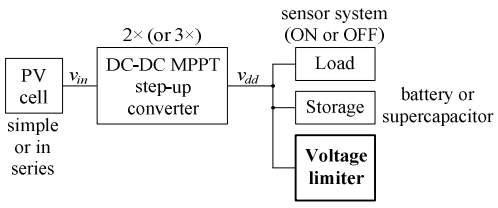


Fig.1. An energy harvesting architecture that hosts the voltage limiter described in this paper.

The output voltage of the converter (v_{dd}) is the one that will be limited by the voltage limiter. The v_{dd} voltage also supplies the inner circuits of the step-up converter. The system can work with one or two PV cells in series and step-up the input voltage (v_{in}) by two or three, depending on the type of PV cells and on the expected light intensities. The power from the PV cell is dependent on its area and on the illumination level, as shown in Fig.2.According to a set of light power intensity measurements, the lowest illumination obtained indoors had an ambient irradiance of 0.1 W/m^2 and the typical irradiance using artificial lighting, was about 0.7 W/m^2.

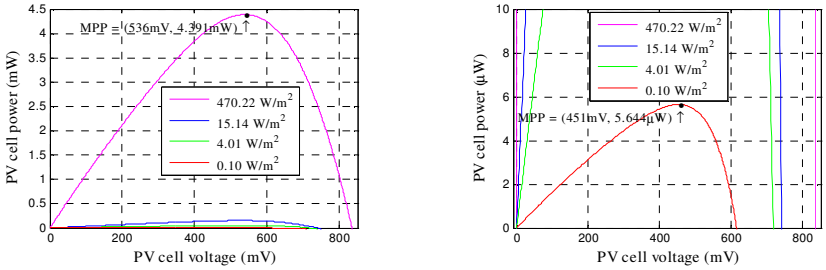


Fig.2. a) Available power from the PV cell with 1 cm^2, for different irradiance levels. b) Detail showing the power function that corresponds to the lowest irradiance level.

The system must be designed for a worst case scenario (low illumination), meaning that when the light is stronger, the system will produce a large voltage at its output.

The system was designed in a 130 nm CMOS technology, having a maximum voltage of about 1.4V.If this value is exceeded, the devices in the die are stressed, reducing their operating lifetime. With a larger voltage, they can even be destroyed.

The v_{dd} voltage can be used to power any application, for example, a sensor node. Since the available power from the PV cells is low, this application typically will work using an ON-OFF regime with a low duty-cycle. While the application is OFF, the harvested energy is stored in a supercapacitor. When the application is ON, it works using this stored energy. In the case of a high light intensity, after the supercapacitor is charged to a desired voltage value, the step-up converter continues to supply a current to the output node (v_{dd}). This results in the output voltage to increase to a value that can be dangerous, being necessary to add a circuit to limit it, by absorbing the excess current supplied by the step-up converter.

In literature, some work can be found concerning voltage limiters. In [3], the voltage limitation is achieved by opening a switch to a capacitor, whenever its voltage exceeds a certain limit, on a sample-and-hold basis. There are other systems that also use voltage limiter circuits, like in [4] and [5], where the voltage limitation problem appears under the context of RFID applications. The amount of available power to a RFID tag is dependent upon the distance to the reader device, resulting in a similar problem to the one in a light energy harvesting system. In [4], the voltage limitation is done by performing a comparison to a desired limit. In [5], a band gap reference circuit is used to generate a reference voltage to which the desired voltage is compared to. This approach is similar to the one proposed in this paper.

4 Voltage Limiter Circuit Architecture

The architecture of the voltage limiter is shown in Fig.3.

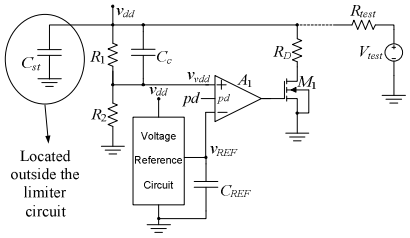


Fig.3. Architecture of the voltage limiter described in this paper.

The Thévenin equivalent, at the right hand side of the dashed line, represents the voltage step-up converter. The aim of the circuit is to limit the v_{dd} voltage, to be lower than 1.4 V – 5% = 1.33 V. The voltage limiter operates by drawing current through M_1. This current causes a voltage drop across R_{test}, such that v_{dd} remains constant. The value, at which v_{dd} is to be limited, is controlled by a Voltage Reference Circuit (VRC), providing a stabilized and temperature compensated voltage reference.

In normal operation, the voltage divider formed by R_1 and R_2, provides at v_{vdd}, a voltage close to v_{REF}. The amplifier A_1 amplifies the error between v_{vdd} and v_{REF}, providing, at its output, a voltage that directly controls the v_{gs} voltage of M_1, and thus the current drawn from the v_{dd} node, through R_D.

4.1 Voltage Reference Circuit

The VRC was adapted from [6], and its schematic is shown in Fig.4 a).The generated reference voltage (v_{REF}), versus the supplying voltage (v_{dd}), and the supply current of the VRC are depicted in Fig.4 b).

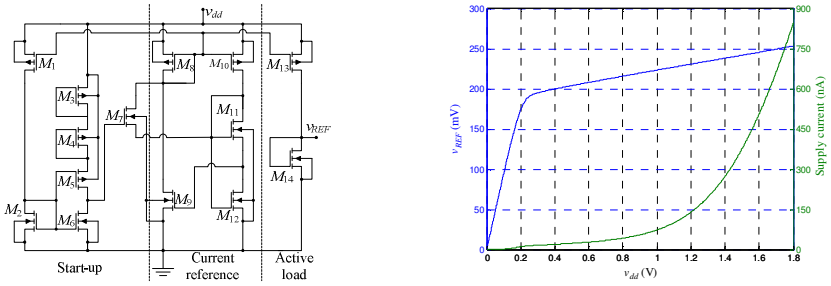


Fig.4. a) CMOS Voltage Reference Circuit. b) Output reference voltage (v_{REF}), and supply current, as a function of v_{dd}.

M_2 and M_{12} are high voltage transistors (3.3 V), while the others are low voltage ones (1.2 V). The main difference between the original circuit, and the one that was built, is the fact that the one in [6] was built in a 180 nm CMOS technology, whereas the present one uses a 130 nm technology. The transistors were sized based on the sizes presented in [6], making only adjustments due to the different technologies.

The layout of the VRC circuit occupied 15647 μm^2. In normal operation, considering that v_{dd} = 1.2 V and a temperature of 27 ºC, the nominal output voltage of the VRC is 230.9 mV. The supply current, in this case, is 139.5 nA. These data are depictable in Fig.4 b). In Fig.5, the supply current and the reference voltage values, as a function of temperature, for different supplying voltages, are shown.

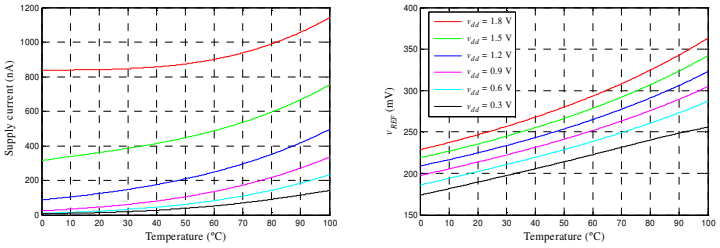


Fig.5. Temperature dependence of the supply current, and generated voltage reference, for different supplying voltages, for the VRC that is used.

4.2 Differential Voltage Amplifier

The topology of the amplifier is shown in Fig.6.This amplifier has a power down feature (*pd*) to disable it, in order to turn off the voltage limiter circuit. The layout of the amplifier occupied 7767 μm^2.The input stage of this amplifier uses PMOS devices, as the typical values of the input voltage are around 200 mV to 300 mV.

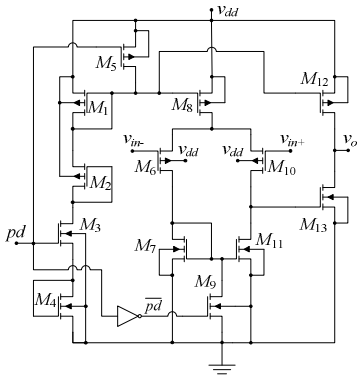


Fig.6. Differential amplifier circuit.

5 Stability Analysis

Since this is a closed loop system (Fig.3), it is important to analyze its stability. The feedback network is constituted by R_1, R_2, C_c and C_p (parasitic capacitance at the amplifier input). The feedback factor, β, is given by

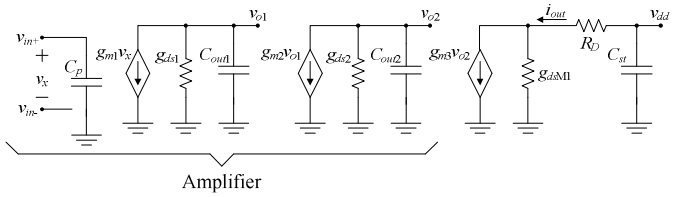
$$\beta(s) = \frac{v_{vdd}}{v_{dd}} = \frac{R_2 + sC_cR_1R_2}{R_1 + R_2 + sR_1R_2(C_c + C_p)}. \quad (1)$$

The impedance,Z_{22}, of the feedback network from v_{dd} to ground, is

$$Z_{22}(s) = \frac{R_1 + R_2 + sR_1R_2(C_c + C_p)}{(1 + sR_1C_c)(1 + sR_2C_p)}. \quad (2)$$

The small-signal model of the amplifier, including the output transistor M_1, is depicted in **Fig.7**.As the output variable, i_{out}, is the current drawn from the v_{dd} node, and the input variable is the input differential voltage of the amplifier (v_x), there will be a transconductance function $G_M(s)$ given by

$$G_M(s) = \frac{i_{out}}{v_x} = \frac{g_{m1}g_{m2}g_{m3}}{(g_{ds1} + sC_{out1})(g_{ds2} + sC_{out2})} \quad (3)$$



$g_{ds1} = g_{ds10} + g_{ds11}$ $\quad C_{out1} = C_{gd10} + C_{db10} + C_{db11} + C_{gs13}$ $\quad (g_{dsM1})^{-1} >> R_D \Rightarrow i_{out} \cong g_{m3}v_{o2}$

$g_{ds2} = g_{ds12} + g_{ds13}$ $\quad C_{out2} = C_{gd12} + C_{db12} + C_{gd13} + C_{db13} + C_{gsM1}$

Fig.7. Small-signal model of the amplifier and the output M_1 transistor.

The impedance seen from v_{dd} to ground, defining $R_o = (g_{dsM1})^{-1} + R_D$, is

$$Z_{out}(s) = Z_{22}(s) // \left(1 \Big/ sC_{st} \right) // R_o. \quad (4)$$

The loop of the system in Fig.3was open before the "+" terminal of A_1. By injecting signal in the "–" terminal, and computing the ratio to the signal obtained at the output of the feedback network, the loop gain is

$$G_L(s) = G_M(s)Z_{out}(s)\beta(s). \quad (5)$$

This function has four poles and one zero. Their expressions are as follows, considering that C_{st}, connected to the output node, is much higher than C_c and that C_p:

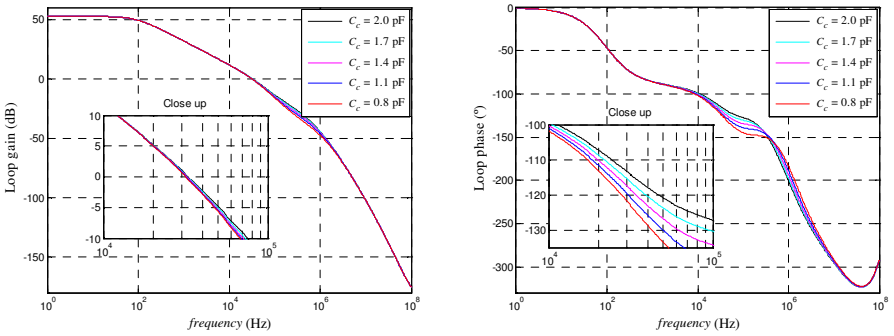
$$f_{p1} = \frac{g_{ds1}}{2\pi C_{out1}}; \quad f_{p2} = \frac{g_{ds2}}{2\pi C_{out2}}; \quad f_{p3} = \frac{1}{2\pi (R_o // (R_1 + R_2))C_{st}};$$
$$f_{p4} = \frac{1}{2\pi (R_1 // R_2)(C_c + C_p)}; \quad f_z = \frac{1}{2\pi R_1 C_c}. \quad (6)$$

The values of f_{p4} and f_z can be approximately equal, by selecting an appropriate value for C_c, thus canceling out each other, making the system equivalent to having only the other three poles. This is useful in improving the phase margin of the system.

Assuming that $R_1 + R_2 >> R_o$, which is the case, the DC loop gain is given by

$$G_L(0) = \frac{g_{m1} g_{m2} g_{m3} R_2 R_o}{g_{ds1} g_{ds2} (R_1 + R_2)}. \quad (7)$$

The magnitude and phase of the open loop gain are determined through an AC sweep analysis and shown next in Fig.8a) and b), respectively. C_c is swept from 0.8 pF to 2.0 pF, to check what would be the consequence on the phase margin of the system. In these simulations, the value of the storage capacitor, C_{st}, was 1.8 µF.



a) b)

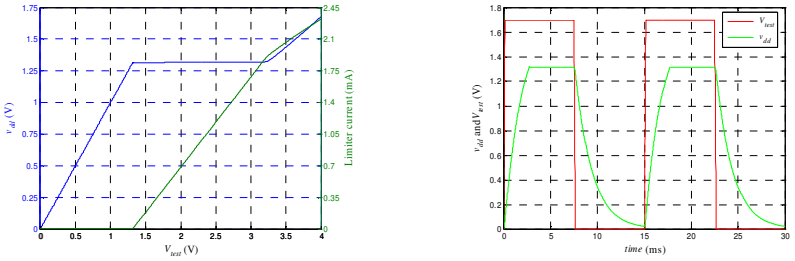
Fig.8. Magnitude and phase functions of the feedback loop circuit ofFig.3.

It can be seen, in the close up inset in Fig.8 a), that regardless of the value of C_c, the zero crossing of the loop gain function occurs at about 32 kHz. As seen by the close up inset in Fig.8 b), at the previous frequency, the spreading of phase values according to the value of C_c, results in a minimum phase margin value of 57º. In order to have an acceptable phase margin value of 60º, the value of C_c was selected to be 1.4 pF. It is important to note that, if the value of C_{st} is increased, the phase margin will also increase. The value of 1.8 µF is still a relatively small value for a storage capacitor, as it can get to units of Farads, or more, thus corresponding to a worst case.

6 Simulation Results

To check the behaviour of the circuit, it was simulated in Spectre. In Fig.9 a) and b), there are depicted the results of a DC sweep and a transient response, respectively, to show the correct operation in different ways. The function in Fig.9 a) was obtained by running a DC sweep, using V_{test}, on the right hand side of the dashed line in Fig.3.The function in Fig.9b) was obtained by using a square wave voltage generator for V_{test}. As seen in both Fig.9a) and b), the voltage limiter comes into action whenever the

voltage in the v_{dd} node tends to be higher than the limit. The voltage at which the limitation in v_{dd} is achieved, is about 1.31 V, which is inside the desired limit. In these tests, the supply current of the amplifier was, typically, about 900 nA.



a) b)

Fig.9. a) DC sweep response. b) Dynamic transient response, with a period of 15 ms.

7 Conclusions

A voltage limiter for indoor light energy harvesting applications has been presented.This circuit is a part of a bigger system, whose function is to harvest indoor light energy, process it and store it so that it can be used at a later time. This system can be used as the supplying module for a node of the Internet of Things.

The circuit that was described, ensured that even under a strong illumination, the generated voltage would not exceed the maximum value allowed by the technology, to avoid stressing, or destroying the devices in the die. Simulation results, using Spectre, were presented and showed that the proposed circuit can successfully limit the output voltage (v_{dd}) to the desired ceiling.

References

1. Paradiso, J.A., Starner, T.: Energy scavenging for mobile and wireless electronics. In: Pervasive Computing, vol.4(1), pp. 18–27. IEEE, Los Alamitos (2005)
2. Chalasani, S., Conrad, J.M.: A survey of energy harvesting sources for embedded systems. In: Southeastcon, April 3-6, pp.442–447. IEEE, Los Alamitos (2008)
3. Silva-Martinez, J.: Adjustable CMOS voltage limiters for low-voltage applications. In: Proc. IEEE International Symposium on Circuits and Systems (ISCAS)1996. - Connecting the World, May 12-15, pp.465–468 (1996)
4. Kim, J., Nam, C., Lee, K.-Y.: A design of transceiver for 13.56 MHz RFID reader using the peak detector with automatic reference voltage generator and voltage limiter. In: Proc. International SoC Design Conference (ISOCC) 2010, Nov.22-23, pp.287–289 (2010)
5. Fernandez, E., Beriain, A., Solar, H., Garcia-Alonso, A., Berenguer, R., Sosa, J., Monzon, J.M., Garcia-Alonso, S., Montiel-Nelson, J.A.: Low power voltage limiter design for a full passive UHF RFID sensor. In: Proc. IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS) 2011, Aug.7-10, pp.1–4 (2011)
6. Magnelli, L., Crupi, F., Corsonello, P., Pace, C., Iannaccone, G.: A 2.6 nW, 0.45 V Temperature-Compensated Sub threshold CMOS Voltage Reference. In: IEEE Journal of Solid-State Circuits, vol. 46 (2), pp. 465-474 (2011)