I-DLTS, Electrical Lag and Low Frequency Noise measurements of Trapping effects in AlGaN/GaN HEMT for reliability studies

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Abstract **GaN technologies have penetrated the microelectronic markets, proving the high potential of this technology for a wide variety of applications (optoLEDs and Laser, power and RF electronics). However, robustness of these widebandgap technologies still needs to be improved: a large number of studies have addressed the main different roots provoking degradation of RF, DC or thermal performances of transistors dedicated to high frequency applications. However, experiencing reliability studies mechanisms on a given technology cannot be carried out to another one, depending on changes of the doping, passivation layer thickness or material, content of Al or In in the ternary composition of the channel… Among the more problematic causes of degradation for high electron mobility transistors (HEMT), traps need to be accurately identified: this paper proposes the jointed expertise using three different experimental workbenches to identify trapping-detrapping effects and free charges effects in AlGaN/GaN HEMT devices over samples from a European foundry. Different samples have been stressed using DC biased devices at ambient temperatures of 25°C and 150°C, and using HTRB stresses at 150°C. Stressed devices and virgin samples are measured using pulsed I-V characterizations (lag effects attributed to free charges), current Deep Level Transient Spectroscopy (I-DLTS) measurements and low frequency noise (LFN) measurements. Each experimental setup has its own specificities, and allows the determination of activation energies and capture sections of the traps, or how these traps or charges affect the transistor performance under realistic HF conditions. Drain-Lag and Gate-lag signatures evidence the large stress effect on the devices, but with different nuances partially correlated to gate leakage currents. Traps measured with I-DTLS and LFN techniques evidence partially correlated origins, and thermally activated traps can be discriminated from electrically activated ones. This approach gives a deeper insight of the prevailing mechanisms causing partial or total failures of the AlGaN/GaN devices.**

Index Terms **— GaN HEMT, reliability, drain-lag, gate-lag, low frequency noise, I-DLTS, trapping effects.**

I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMT) stand as an interesting solution to substitute GaAs and SiGe technologies for power and high frequency applications, as they take advantages from higher breakdown voltage, higher power density, higher thermal conductivity and from good low noise capabilities [1][2][3]. Hence, GaN devices can pretend to be integrated in SatCom high frequency transceivers for power amplification (ground segment), low noise robust amplification (ground and space segments), high power frequency sources and highly linear mixers (radar applications). As space and military applications need qualified technologies for the development of highly reliable systems, GaN transistors have to attest the lower failure risk, particularly under high thermal conditions, high electrical field. Reliability studies are on going to develop behavioral models and to focus on the degradation trends (drift in power, PAE) under RF, DC or temperature stresses [4]. The tricky context of GaN devices (wide bandgap, piezoelectric effects, thermal effects, lattice mismatches ...) binds technologies suppliers to widen their experimental field of investigations, and to cross results from different characterization tools; so the physical origin of the degradation can be evidenced effectively. We thereafter present results issued from pulsed I(V) characterizations, low frequency noise (LFN) measurements and current deep level transient spectroscopy (I-DLTS) measurements. All these tools are experienced as accurate workbenches for the characterization of material defects (LFN), traps identification (LFN and I-DLTS) and fixed charges effects (pulsed I(V), I-DLTS and C-DLTS).

AlGaN/GaN HEMT devices are grown by MOCVD technique on SiC substrate. Transistors feature 0.25*8*125 µm² gate area, 27% alumina content and non intentionally doped layers. Devices are stressed using different stress conditions:

-IDQ stress is performed at I_{DS} Quiescent drain current of 50mA/mm and V_{DS}=30V, at temperatures of 25°C or 150 °C.

-HTRB stress is performed at High Temperature (150°C) Reverse Bias on the gate (V_{GS}=-7V), while the drain is biased at 50V.

In the first section, pulsed I(V) characteristics are presented, according to a procedure allowing the discrimination of thermal, gate and drain effects. The second section is dedicated to I-DLTS measurements where activation energies and capture section of the traps are given. Then the last section proposes spectra from LFN measurements, featuring numerous trapping-detrapping effects according to a smooth repartition versus the frequency measurement range. Virgin and stressed samples are measured and compared to reveal the impact of the stress on the devices. Preliminary static measurements have been performed, featuring an average

degradation of 40% on I_{DSS} before and after the application of the stress (2000h).

Thereafter, the only results related to HTRB stress are presented: other IDQ and HTRB stressed devices will be joined in the conclusion of the final paper.

II. GATE-LAG AND DRAIN-LAG CHARACTERIZATION

This method is based on I(V) pulsed measurements at specific quiescent bias points to discriminate gate-lag and drain-lag phenomena from self-heating effects. The pulse duration τ is chosen as short as possible (0,1 µs) in order to limit self-heating, and the period T between pulses is set to 50 ms. Thereafter, $V_{quiescent}$ (resp. $I_{quiescent}$) represents the voltage (resp. current) during the T period, while V (rep. I) represents the voltage (resp. current) measured during the duration τ of the pulse (cf. figure 1 for the measurement of the I_{DS} current).

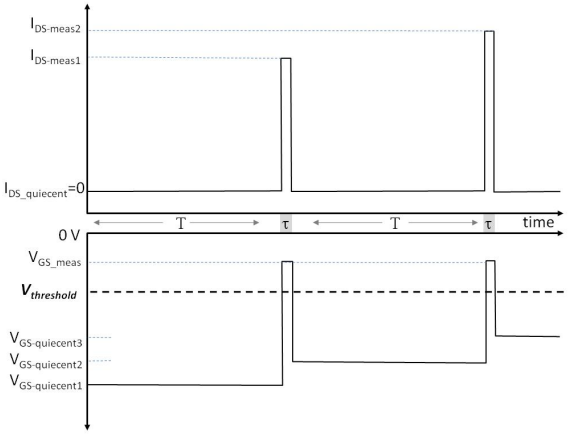

Fig. 1. time representation of the pulse, with the quiescent (stand-off) current/voltage between 2 measurements (pulses τ). Here, V_{DS} is fixed at $V_{DS\text{-}quiescent}$ for gate-lag measurements.

A. Gate-lag modeling

Pulsed I(V) characterization is realized with a DIVA D210 commercial setup (figure 2). A current probe has been added to observe the shape of the pulses of drain current in the time domain (using an oscilloscope, figure 3).

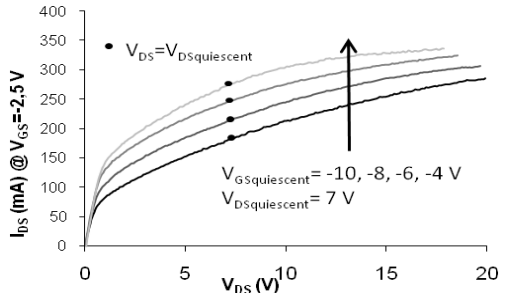

Fig. 2. classic pulsed I(V) curves for different $V_{GSquiescent}$. Only $V_{DS}=V_{DS\text{-}quiescent}$ is considered for gate-lag. Measurement is shown for a stressed device.

Firstable, in order to remove self-heating effects at the quiescent bias point, $V_{GSquiescent}$ varies from -10 V to $V_{pinch\ off}$ (-4 V) while $V_{DSquiescent}$ remains constant ($P_{DCquiescent}$=0 W on the explored V_{GS} range as I_{DS} is null). Then, $I_{DS}(V_{DS})$ for different V_{GS} are used to extract gate-lag behaviors when drain-lag contribution is neglected: the procedure consists in extracting the data at $V_{DS}=V_{DSquiescent}$ (figure 2) which represents the only point where the only lag contribution comes from the gate.

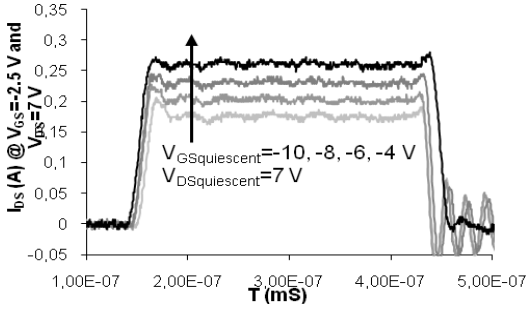

Fig. 3. time domain characterization of I_{DS} pulses at $V_{DS}=V_{DS\text{-}quiescent}$ for different $V_{GS\text{-}quiescent}$. Same device than for Fig. 2.

Time domain characterization of figure 3 gives the rise and fall profile of the pulse shape: as lag effect can be attributed to time constant (RC) or to pulse level modification (fixed charges), it can be noticed here that only the level of the current is changed according to $V_{GS\text{-}quiescent}$. Thus, the lag cannot be attributed to RC time constant but to fixed charges in the structure. The two techniques illustrated on figure 2 and figure 3 are in good agreement, and a linear signature of the lag effects on the gate access is given in figure 4 for a stressed device.

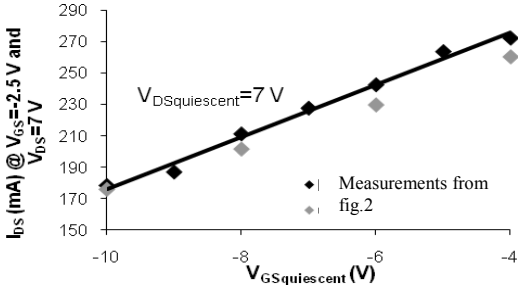

Fig. 4. Gate-lag evolution versus V_{GS}: extracted from pulsed measurements (from classic I(V) and time domain measurements).

The variation on I_{DS} can be as high as 40% variation when V_{GS} swings with ±3V from the biasing DC point. As V_{GS} is shifted while V_{DS} remains constant, both V_{DG} and V_{GS} can be invoked to locate the fixed oxide charges under the passivation layer respectively between drain and gate or between gate and source: from studies on devices featuring different passivation techniques, it has been shown that gate-lag effects can be reduced even if they are still sensitive (less than 20% variation on I_{DS}, i.e. in the same order than for virgin devices). Electrical and thermal stress under HTRB impacts the material integrity by generating charges in the active regions of the devices, impacting the command of the

transistor. The HTRB stress and tunneling effects will be discussed in the final version.

B. Drain-lag

Using the same experimental procedure, pulsed I(V) measurements have been performed to evaluate drain-lag effects. For that purpose, $V_{GSquiescent}$ is now kept at a constant value while $V_{DSquiescent}$ varies from 0 V to 15 V. Moreover, $V_{GSquiescent}$ is set at $V_{pinch\ off}$, preventing from any thermal effect (P_{DC}=0 W): however gate-lag effects also contribute to the overall lag signature. This problem can be removed by deembedding the gate lag contribution using the previous gate-lag model (at $V_{DSquiescent}$ = 7V only, for figure 3) for both the test sample and the stressed device.

Figure 5 represents the drain-lag profile versus $V_{DS\text{-}quiescent}$ for devices from HTRB batch: the stressed devices feature the same behavior but with larger I_{DS} swings (more than 30% for a stressed device, versus less than 10% for a virgin sample)..

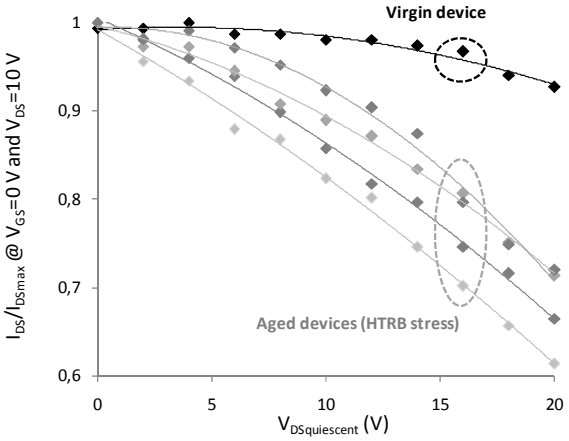

Fig. 5. relative drain-lag effect on HTRB-aged and virgin devices measured at V_{GS}=0V and V_{DS}=10V.

III. I-DLTS MEASUREMENTS

Deep level characterization of a semiconductor material allows the determination of the concentration and section of defects in the bulk material. We have matched this DLTS workbench for HEMT device characterization. For each stressed and virgin devices, current DLTS plots are measured (figure 6, for a stressed device). Measurements are performed over a temperature range between 90 K and 450 K. The Fast Fourier Transform of the I-DLTS signal is used to convert data into the Arrhenius plot (figure 7): the activation energy and the section of the traps are then extracted for each sample.

According to the employed passivation technique, activation energies vary: the results are consistent with the quantification of lag effects from the previous section. Virgin devices feature two activation energies at Ea=0.57eV (trap section of σ_T= 1.3 10^{-15} cm²) and Ea=0.7eV (trap section of σ_T=7.5 10^{-15} cm²). Devices from HTRB#2 batch (lower plate temperature) have been measured with an activation energy of Ea=0.206eV (σ_T=6 10^{-17} cm²). All these traps are electron trap states. Transistors from HRTB#1 batch (higher plate temperature) feature electron trap states with Ea=0.64eV (trap section σ_T=3.7 10^{-15} cm²), and hole trap states with Ea=0.3eV (trap section of σ_T=6 10^{-20} cm²). Electron trap states and hole trap states can probably be associated to interface states at the surface near the gate, and possibly in the AlGaN bulk.

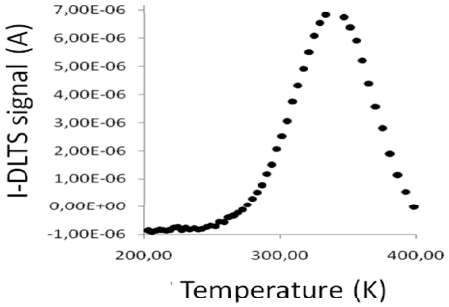

Fig. 6. Current Deep Level Transient Spectroscopy for HEMT AlGaN/GaN (IDQ stress). Device biased at V_{GS}=-3V, V_{DS}=8V.

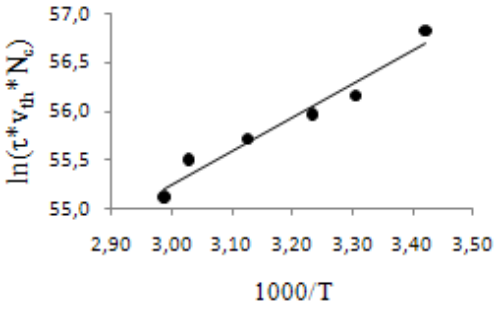

Fig. 7. Arrhenius plot for HEMT AlGaN/GaN (IDQ stress @ 150°C). The device is biased at V_{GS}=-3V, V_{DS}=8V.

IV. LOW FREQUENCY NOISE MEASUREMENTS

Low frequency noise measurements are largely used as a diagnostic tool to evaluate and locate defects in the structure. It is thus suitable for reliability studies, as the tracking of the noise sources constituting the spectra gives information on the related activation parameter (thermal, electrical, ..). We have performed different set of measurements on gate (S_{IG}) and drain (S_{ID}) accesses, as well as the correlation between these two extrinsic noise current sources when needed (i.e. when S_{IG} is less than 5 orders of magnitude lower than S_{ID}). We focus on evolution of the noise spectra under ohmic and saturated biasing conditions. Measurements are carried out using a transimpedance amplifier direct measurement technique which allows rapid LFN measurements of S_{ID}, S_{IG}, and the correlation coefficient over a wide frequency range (from 1 Hz to 100 kHz).

Stressed and virgin transistors noise characteristics differ by the magnitude of the overall noise spectra on S_{ID}: current spectral density of aged devices is one to three orders higher

than current spectral density of virgin devices. Anyway, whatever the device or the biasing condition (Ohmic or saturated), a large number of GR noise sources is superimposed with the 1/f flicker source. These GR centers are attributed to distributed traps close to the gate, where charges flow through the AlGaN barrier (tunneling) or at the passivation/AlGaN interface towards the drain access. When V_{GS} decreases down to the pinch-off voltage, a stronger contribution of several GR appears, attributed to thermally activated traps at the AlGaN/GaN interface [5][6].

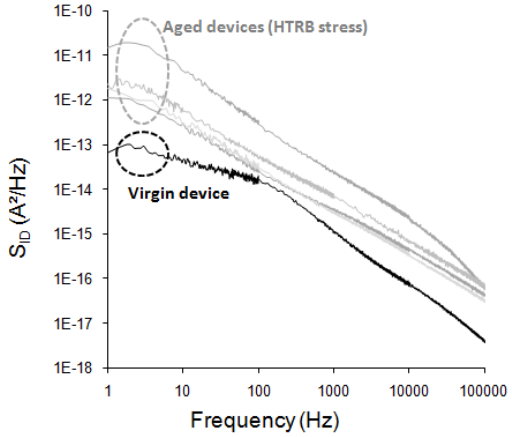

Fig. 8. normalized drain current noise spectral density S_{ID}/I_D for HTRB#1 (high storage temperature): devices are biased at V_{GS}=0V and V_{DS}=10V

S_{IG} strongly depends on gate leakage currents, but aged devices present large dispersion. From Fig. 9, S_{IG} spectral source is clearly related to gate leakage conduction modes. As the gate current of aged devices increases drastically, the correlation between gate and drain noise sources becomes important. This also indicate tunneling effects from the gate access to the 2 dimension electron gas.

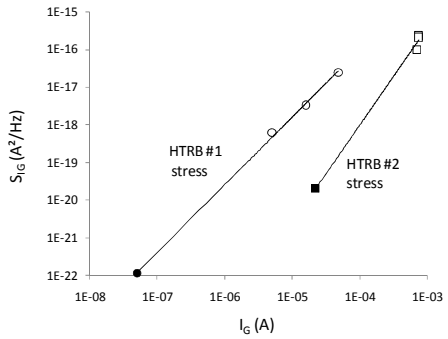

Fig. 9. gate current noise spectral density from HTRB batches at two different plate temperatures: Temp. HTRB#1 > Temp. HTRB#2 (black symbols represent virgin devices, white symbols are for aged devices, i.e. higher gate leakage currents). LFN measured at V_{GS}=-3V and V_{DS}=10V. The inset presents the frequency spectra for aged and virgin devices (HTRB#2).

From the different experimental tools used to characterize the trapping effects, we have evidenced correlations between electrical pulsed characterization and I-DLTS measurements, and also between I-DLTS and LFN measurements. However, these correlations are not absolute, and complex mechanisms seem to be bind in the transistor.

VII. CONCLUSION

We have proposed a characterization of AlGaN/GaN HEMT devices with electrical pulsed workbenches dedicated to lag modeling, current deep level transient spectroscopy and low frequency noise measurements setups: from I(V) pulsed measurements, gate-lag and drain-lag behaviors have been extracted under different pulse periods conditions. The stressed devices feature larger lag effects than the sample devices, but the change of passivation layer reduces significantly gate lag as well as drain lag effects. These lag effects are attributed to fixe oxide charges between source and gate and between gate and drain. I-DLTS have evidenced numerous traps, with lower activation energies for aged devices at 0.206eV, 0.64eV (electron trap states) and 0.3eV (hole trap state). LFN measurements have also revealed numerous distributed GR centers; some trapping-detrapping noise sources are located at the AlGaN/GaN interface while temperature dependant traps are evaluated between drain and gate under the passivation layer.

REFERENCES

[1] Lan, X. Wojtowicz, M. Smorchkova, I. Coffie, R. Tsai, R. Heying,B. Truong, M. Fong, F. Kintis, M. Namba, C. Oki, A. Wong, T., "AQ-band low phase noise monolithic AlGaN/GaN HEMT VCO",*IEEE Microwave and Wireless Components Letters*, Vol. 16 (2006), pp 425-427.

[2] G. Soubercaze-pun, J.G. Tartarin, L.Bary, J.Rayssac, E.Morvan, B.Grimbert, S.L. Delage, J-C. De Jaeger, J. Graffeuil, 'Design of X-band GaN oscillator: from the low frequency noise device characterization and large signal modeling to circuit design', *IEEE MTT Symposium 2006, San Francisco (U.S.A),* pp.747

[3] M. Rudolph et al. "Highly rugged 30 GHz GaN Low-Noise Amplifiers", *IEEE Microwave and Wireless components Letters*, Vol. 19, N°. 4, April 2009, pp. 251-253.

[4] Dumka, D.C. and Lee, C. and Tserng, H.Q. and Saunier, P., "RF reliability performance of AlGaN/GaN HEMTs on Si substrate at 10 GHz," *IEEE Electronics Letter.,* vol. 40, no. 24, pp. 1554-1556, Novembre 2004.

[5] J.G Tartarin, G. Soubercaze-Pun, J.L. Grondin, L. Bary, J. Mimila-Arroyo, J. Chevallier, 'Generation-recombination in AlGaN/GaN HEMT on SiC substrate evidenced by low frequency noise measurements and SIMS characterization', *International Conference on Noise and Fluctuations*, ICNF 2007, Tokyo, Japan, pp. 163-166.

[6] G.Astre, J.G.Tartarin , B. Lambert, 'Trapping related degradation effects in AlGaN/GaN HEMT', European Microwave Integrated Circuits Conference (EuMIC 2010), Paris (France), 2010, pp.298-301.