I-DLTS, Electrical Lag and Low Frequency Noise measurements of Trapping effects in AlGaN/GaN HEMT for reliability studies

Jean-Guy Tartarin, Serge Karboyan, François Olivié, Guilhem Astre, Laurent Bary, B Lambert

To cite this version:


abstractAccess=no

userType=inst>. <hal-01343977>
I-DLTS, Electrical Lag and Low Frequency Noise measurements of Trapping effects in AlGaN/GaN HEMT for reliability studies

J.G. Tartarin¹,², S. Karboyan¹,², F. Olivie¹,², G. Astre¹,², L. Bary²
¹ Université de Toulouse
² LAAS-CNRS
7 av. du Colonel Roche
31.077 Toulouse Cedex 4, France
tartarin@laas.fr

B. Lambert
United Monolithic Semiconductors SAS
Route Départementale 128 – BP 46
91.401 Orsay cedex - France
Benoit.lambert@ums-gaas.com

Abstract GaN technologies have penetrated the microelectronic markets, proving the high potential of this technology for a variety of applications (optoLEDs and Laser, power and RF electronics). However, robustness of these wide bandgap technologies still needs to be improved: a large number of studies have addressed the main causes of degradation of high electron mobility transistors (HEMTs), traps need to be accurately identified: this paper proposes the joint expertise using three different experimental workbenches to identify trapping-detrappping effects and free charges effects in AlGaN/GaN HEMT devices over samples from a European foundry. Different samples have been stressed using DC biased devices at ambient temperatures of 25°C and 150°C, and using HTRB stresses at 150°C. Stressed devices and virgin samples are measured using pulsed I-V characterizations (lag effects attributed to free charges), current Deep Level Transient Spectroscopy (I-DLTS) measurements and low frequency noise (LFN) measurements. Each experimental setup has its own specificities, and allows the determination of activation energies and capture sections of the traps, or how these traps or charges affect the transistor performance under realistic HF conditions. Drain-Lag and Gate-lag signatures evidence the large stress effect on the devices, but with different nuances partially correlated to gate leakage currents. Traps measured with I-DLTS and LFN techniques evidence partially correlated origins, and thermally activated traps can be discriminated from electrically activated ones. This approach gives a deeper insight of the prevailing mechanisms causing partial or total failures of the AlGaN/GaN devices.

Index Terms — GaN HEMT, reliability, drain-lag, gate-lag, low frequency noise, I-DLTS, trapping effects.

I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMT) stand as an interesting solution to substitute GaAs and SiGe technologies for power and high frequency applications, as they take advantages from higher breakdown voltage, higher power density, higher thermal conductivity and from good low noise capabilities [1][2][3]. Hence, GaN devices can pretend to be integrated in SatCom high frequency transceivers for power amplification (ground segment), low noise robust amplification (ground and space segments), high power frequency sources and highly linear mixers (radar applications). As space and military applications need qualified technologies for the development of highly reliable systems, GaN transistors have to attest the lower failure risk, particularly under high thermal conditions, high electrical field. Reliability studies are on going to develop behavioral models and to focus on the degradation trends (drift in power, PAE) under RF, DC or temperature stresses [4]. The tricky context of GaN devices (wide bandgap, piezoelectric effects, thermal effects, lattice mismatches...) binds technologies suppliers to widen their experimental field of investigations, and to cross results from different characterization tools; so the physical origin of the degradation can be evidenced effectively. We thereafter present results issued from pulsed I(V) characterizations, low frequency noise (LFN) measurements and current deep level transient spectroscopy (I-DLTS) measurements. All these tools are experienced as accurate workbenches for the characterization of material defects (LFN), traps identification (LFN and I-DLTS) and fixed charges effects (pulsed I(V), I-DLTS and C-DLTS).

AlGaN/GaN HEMT devices are grown by MOCVD technique on SiC substrate. Transistors feature 0.25*8*125 μm² gate area, 27% alumina content and non intentionally doped layers. Devices are stressed using different stress conditions:

- I-V characteristics are measured using pulsed I(V) characterizations (lag effects attributed to free charges), current Deep Level Transient Spectroscopy (I-DLTS) measurements and low frequency noise (LFN) measurements. Each experimental setup has its own specificities, and allows the determination of activation energies and capture sections of the traps, or how these traps or charges affect the transistor performance under realistic HF conditions. Drain-Lag and Gate-lag signatures evidence the large stress effect on the devices, but with different nuances partially correlated to gate leakage currents. Traps measured with I-DLTS and LFN techniques evidence partially correlated origins, and thermally activated traps can be discriminated from electrically activated ones. This approach gives a deeper insight of the prevailing mechanisms causing partial or total failures of the AlGaN/GaN devices.

Index Terms — GaN HEMT, reliability, drain-lag, gate-lag, low frequency noise, I-DLTS, trapping effects.

I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMT) stand as an interesting solution to substitute GaAs and SiGe technologies for power and high frequency applications, as they take advantages from higher breakdown voltage, higher power density, higher thermal conductivity and from good low noise capabilities [1][2][3]. Hence, GaN devices can pretend to be integrated in SatCom high frequency transceivers for power amplification (ground segment), low noise robust amplification (ground and space segments), high power frequency sources and highly linear mixers (radar applications). As space and military applications need qualified technologies for the development of highly reliable systems, GaN transistors have to attest the lower failure risk, particularly under high thermal conditions, high electrical field. Reliability studies are on going to develop behavioral models and to focus on the degradation trends (drift in power, PAE) under RF, DC or temperature stresses [4]. The tricky context of GaN devices (wide bandgap, piezoelectric effects, thermal effects, lattice mismatches...) binds technologies suppliers to widen their experimental field of investigations, and to cross results from different characterization tools; so the physical origin of the degradation can be evidenced effectively. We thereafter present results issued from pulsed I(V) characterizations, low frequency noise (LFN) measurements and current deep level transient spectroscopy (I-DLTS) measurements. All these tools are experienced as accurate workbenches for the characterization of material defects (LFN), traps identification (LFN and I-DLTS) and fixed charges effects (pulsed I(V), I-DLTS and C-DLTS).

AlGaN/GaN HEMT devices are grown by MOCVD technique on SiC substrate. Transistors feature 0.25*8*125 μm² gate area, 27% alumina content and non intentionally doped layers. Devices are stressed using different stress conditions:

- I-DLTS stress is performed at IGS=1 Quiescent drain current of 50mA/mm and VDS=30V, at temperatures of 25°C or 150 °C.
- I-V characteristics are measured using pulsed I(V) characterizations (lag effects attributed to free charges), current Deep Level Transient Spectroscopy (I-DLTS) measurements and low frequency noise (LFN) measurements. Each experimental setup has its own specificities, and allows the determination of activation energies and capture sections of the traps, or how these traps or charges affect the transistor performance under realistic HF conditions. Drain-Lag and Gate-lag signatures evidence the large stress effect on the devices, but with different nuances partially correlated to gate leakage currents. Traps measured with I-DLTS and LFN techniques evidence partially correlated origins, and thermally activated traps can be discriminated from electrically activated ones. This approach gives a deeper insight of the prevailing mechanisms causing partial or total failures of the AlGaN/GaN devices.

Index Terms — GaN HEMT, reliability, drain-lag, gate-lag, low frequency noise, I-DLTS, trapping effects.

I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMT) stand as an interesting solution to substitute GaAs and SiGe technologies for power and high frequency applications, as they take advantages from higher breakdown voltage, higher power density, higher thermal conductivity and from good low noise capabilities [1][2][3]. Hence, GaN devices can pretend to be integrated in SatCom high frequency transceivers for power amplification (ground segment), low noise robust amplification (ground and space segments), high power frequency sources and highly linear mixers (radar applications). As space and military applications need qualified technologies for the development of highly reliable systems, GaN transistors have to attest the lower failure risk, particularly under high thermal conditions, high electrical field. Reliability studies are on going to develop behavioral models and to focus on the degradation trends (drift in power, PAE) under RF, DC or temperature stresses [4]. The tricky context of GaN devices (wide bandgap, piezoelectric effects, thermal effects, lattice mismatches...) binds technologies suppliers to widen their experimental field of investigations, and to cross results from different characterization tools; so the physical origin of the degradation can be evidenced effectively. We thereafter present results issued from pulsed I(V) characterizations, low frequency noise (LFN) measurements and current deep level transient spectroscopy (I-DLTS) measurements. All these tools are experienced as accurate workbenches for the characterization of material defects (LFN), traps identification (LFN and I-DLTS) and fixed charges effects (pulsed I(V), I-DLTS and C-DLTS).

AlGaN/GaN HEMT devices are grown by MOCVD technique on SiC substrate. Transistors feature 0.25*8*125 μm² gate area, 27% alumina content and non intentionally doped layers. Devices are stressed using different stress conditions:

- I-DLTS stress is performed at IGS=1 Quiescent drain current of 50mA/mm and VDS=30V, at temperatures of 25°C or 150 °C.
- HTRB stress is performed at High Temperature (150°C) Reverse Bias on the gate (VGS=-7V), while the drain is biased at 50V.

In the first section, pulsed I(V) characteristics are presented, according to a procedure allowing the discrimination of thermal, gate and drain effects. The second section is dedicated to I-DLTS measurements where activation energies and capture section of the traps are given. Then the last section proposes spectra from LFN measurements, featuring numerous trapping-detrappping effects according to a smooth repartition versus the frequency measurement range. Virgin and stressed samples are measured and compared to reveal the impact of the stress on the devices. Preliminary static measurements have been performed, featuring an average
degradation of 40% on $I_{DS}$ before and after the application of the stress (2000h).

Thereafter, the only results related to HTRB stress are presented: other IDQ and HTRB stressed devices will be joined in the conclusion of the final paper.

II. GATE-LAG AND DRAIN-LAG CHARACTERIZATION

This method is based on I(V) pulsed measurements at specific quiescent bias points to discriminate gate-lag and drain-lag phenomena from self-heating effects. The pulse duration $\tau$ is chosen as short as possible (0.1 $\mu$s) in order to limit self-heating, and the period $T$ between pulses is set to 50 ms. Thereafter, $V_{\text{quiescent}}$ (resp. $I_{\text{quiescent}}$) represents the voltage (resp. current) during the $T$ period, while $V$ (resp. $I$) represents the voltage (resp. current) measured during the duration $\tau$ of the pulse (cf. figure 1 for the measurement of the $I_{DS}$ current).

![Fig. 1. time representation of the pulse, with the quiescent (stand-off) current/voltage between 2 measurements (pulses $\tau$). Here, $V_{\text{in}}$ is fixed at $V_{DS\text{-quiescent}}$ for gate-lag measurements.](image)

A. Gate-lag modeling

Pulsed I(V) characterization is realized with a DIVA D210 commercial setup (figure 2). A current probe has been added to observe the shape of the pulses of drain current in the time domain (using an oscilloscope, figure 3).

![Fig. 2. classic pulsed I(V) curves for different $V_{GS\text{-quiescent}}$. Only $V_{\text{in}}=V_{DS\text{-quiescent}}$ is considered for gate-lag. Measurement is shown for a stressed device.](image)

Firstable, in order to remove self-heating effects at the quiescent bias point, $V_{GS\text{-quiescent}}$ varies from -10 V to $V_{\text{pinch-off}}$ (-4 V) while $V_{DS\text{-quiescent}}$ remains constant (PDCquiescent=0 W on the explored $V_{GS}$ range as $I_{DS}$ is null). Then, $I_{DS}(V_{GS})$ for different $V_{GS}$ are used to extract gate-lag behaviors when drain-lag contribution is neglected: the procedure consists in extracting the data at $V_{DS}=V_{DS\text{-quiescent}}$ (figure 2) which represents the only point where the only lag contribution comes from the gate.

![Fig. 3. time domain characterization of $I_{DS}$ pulses at $V_{DS}=V_{DS\text{-quiescent}}$ for different $V_{GS\text{-quiescent}}$. Same device than for Fig. 2.](image)

Time domain characterization of figure 3 gives the rise and fall profile of the pulse shape: as lag effect can be attributed to time constant (RC) or to pulse level modification (fixed charges), it can be noticed here that only the level of the current is changed according to $V_{GS\text{-quiescent}}$. Thus, the lag cannot be attributed to RC time constant but to fixed charges in the structure. The two techniques illustrated on figure 2 and figure 3 are in good agreement, and a linear signature of the lag effects on the gate access is given in figure 4 for a stressed device.

![Fig. 4. Gate-lag evolution versus $V_{GS}$: extracted from pulsed measurements (from classic I(V) and time domain measurements).](image)

The variation on $I_{DS}$ can be as high as 40% variation when $V_{GS}$ swings with $\pm$3V from the biasing DC point. As $V_{GS}$ is shifted while $V_{DS}$ remains constant, both $V_{DS}$ and $V_{GS}$ can be invoked to locate the fixed oxide charges under the passivation layer respectively between drain and gate or between gate and source: from studies on devices featuring different passivation techniques, it has been shown that gate-lag effects can be reduced even if they are still sensitive (less than 20% variation on $I_{DS}$, i.e. in the same order than for virgin devices). Electrical and thermal stress under HTRB impacts the material integrity by generating charges in the active regions of the devices, impacting the command of the
transistor. The HTRB stress and tunneling effects will be discussed in the final version.

B. Drain-lag

Using the same experimental procedure, pulsed I(V) measurements have been performed to evaluate drain-lag effects. For that purpose, $V_{D\text{S\text{quiescent}}}$ is now kept at a constant value while $V_{D\text{S\text{quiescent}}}$ varies from 0 V to 15 V. Moreover, $V_{D\text{S\text{quiescent}}}$ is set at $V_{\text{pinch-off}}$, preventing from any thermal effect ($P_{DC}=0$ W); however gate-lag effects also contribute to the overall lag signature. This problem can be removed by deembedding the gate lag contribution using the previous gate-lag model (at $V_{D\text{S\text{quiescent}}}=7$V only, for figure 3) for both the test sample and the stressed device.

Figure 5 represents the drain-lag profile versus $V_{D\text{S\text{quiescent}}}$ for devices from HTRB batch: the stressed devices feature the same behavior but with larger $I_D$ swings (more than 30% for a stressed device, versus less than 10% for a virgin sample).

![Figure 5](image)

**Fig. 5.** relative drain-lag effect on HTRB-aged and virgin devices measured at $V_{GS}=0$V and $V_{DS}=10$V.

**III. I-DLTS MEASUREMENTS**

Deep level characterization of a semiconductor material allows the determination of the concentration and section of defects in the bulk material. We have matched this DLTS workbench for HEMT device characterization. For each stressed and virgin devices, current DLTS plots are measured (figure 6, for a stressed device). Measurements are performed over a temperature range between 90 K and 450 K. The Fast Fourier Transform of the I-DLTS signal is used to convert data into the Arrhenius plot (figure 7): the activation energy and the section of the traps are then extracted for each sample.

According to the employed passivation technique, activation energies vary: the results are consistent with the quantification of lag effects from the previous section. Virgin devices feature two activation energies at $E_a=0.57$eV ($\sigma_T=1.3 10^{-15}$ cm²) and $E_a=0.7$eV (trap section of $\sigma_T=7.5 10^{-15}$ cm²). Devices from HTRB#2 batch (lower plate temperature) have been measured with an activation energy of $E_a=0.206$eV ($\sigma_T=6 10^{-17}$ cm²). All these traps are electron trap states. Transistors from HTRB#1 batch (higher plate temperature) feature electron trap states with $E_a=0.64$eV (trap section $\sigma_T=3.7 10^{-15}$ cm²), and hole trap states with $E_a=0.3$eV (trap section of $\sigma_T=6 10^{-20}$ cm²). Electron trap states and hole trap states can probably be associated to interface states at the surface near the gate, and possibly in the AlGaN bulk.

![Figure 6](image)

**Fig. 6.** Current Deep Level Transient Spectroscopy for HEMT AlGaN/GaN (IDQ stress). Device biased at $V_{GS}=-3$V, $V_{DS}=8$V.

![Figure 7](image)

**Fig. 7.** Arrhenius plot for HEMT AlGaN/GaN (IDQ stress @ 150°C). The device is biased at $V_{gs}=-3$V, $V_{ds}=8$V.

**IV. LOW FREQUENCY NOISE MEASUREMENTS**

Low frequency noise measurements are largely used as a diagnostic tool to evaluate and locate defects in the structure. It is thus suitable for reliability studies, as the tracking of the noise sources constituting the spectra gives information on the related activation parameter (thermal, electrical, ..). We have performed different set of measurements on gate ($S_{Gn}$) and drain ($S_{Dn}$) accesses, as well as the correlation between these two extrinsic noise current sources when needed (i.e. when $S_{Gn}$ is less than 5 orders of magnitude lower than $S_{Dn}$). We focus on evolution of the noise spectra under ohmic and saturated biasing conditions. Measurements are carried out using a transimpedance amplifier direct measurement technique which allows rapid LFN measurements of $S_{GD}$, $S_{DG}$, and the correlation coefficient over a wide frequency range (from 1 Hz to 100 kHz).

Stressed and virgin transistors noise characteristics differ by the magnitude of the overall noise spectra on $S_{GD}$, current spectral density of aged devices is one to three orders higher.
than current spectral density of virgin devices. Anyway, whatever the device or the biasing condition (Ohmic or saturated), a large number of GR noise sources is superimposed with the 1/f flicker source. These GR centers are attributed to distributed traps close to the gate, where charges flow through the AlGaN barrier (tunneling) or at the passivation/AlGaN interface towards the drain access. When $V_{GS}$ decreases down to the pinch-off voltage, a stronger contribution of several GR appears, attributed to thermally activated traps at the AlGaN/GaN interface [5][6].

Fig. 8. normalized drain current noise spectral density $S_{ID}/I_D$ for HTRB#1 (high storage temperature): devices are biased at $V_{GS}$=0V and $V_{DS}$=10V

$S_{ID}$ strongly depends on gate leakage currents, but aged devices present large dispersion. From Fig. 9, $S_{IG}$ spectral source is clearly related to gate leakage conduction modes. As the gate current of aged devices increases drastically, the correlation between gate and drain noise sources becomes important. This also indicate tunneling effects from the gate access to the 2 dimension electron gas.

Fig. 9. gate current noise spectral density from HTRB batches at two different plate temperatures: Temp. HTRB#1 > Temp. HTRB#2 (black symbols represent virgin devices, white symbols are for aged devices, i.e. higher gate leakage currents). LFN measured at $V_{GS}$=-3V and $V_{DS}$=10V. The inset presents the frequency spectra for aged and virgin devices (HTRB#2).

From the different experimental tools used to characterize the trapping effects, we have evidenced correlations between electrical pulsed characterization and I-DLTS measurements, and also between I-DLTS and LFN measurements. However, these correlations are not absolute, and complex mechanisms seem to bind in the transistor.

VII. CONCLUSION

We have proposed a characterization of AlGaN/GaN HEMT devices with electrical pulsed workbenches dedicated to lag modeling, current deep level transient spectroscopy and low frequency noise measurements setups: from $I(V)$ pulsed measurements, gate-lag and drain-lag behaviors have been extracted under different pulse periods conditions. The stressed devices feature larger lag effects than the sample devices, but the change of passivation layer reduces significantly gate lag as well as drain lag effects. These lag effects are attributed to fixe oxide charges between source and gate and between gate and drain. I-DLTS have evidenced numerous traps, with lower activation energies for aged devices at 0.206eV, 0.64eV (electron trap states) and 0.3eV (hole trap state). LFN measurements have also revealed numerous distributed GR centers; some trapping-detrapping noise sources are located at the AlGaN/GaN interface while temperature dependant traps are evaluated between drain and gate under the passivation layer.

REFERENCES


