Influence of gate leakage current on AlGaN/GaN HEMTs evidenced by low frequency noise and pulsed electrical measurements

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Abstract

The study of the pulsed drain current or noise characteristics in AlGaN/GaN HEMTs is the key of knowledge for designing the power amplifiers, the low noise amplifiers and the oscillators or mixers, but it is well accepted today that this study is not fully accomplished without pointing on the effect of the gate leakage current; It is obvious that the transistor's leakage current may disturb its operation at high power and high frequency. Leakage currents studies are also an area of great importance in optimization of safe operating area and reliability of HEMTs. Therefore, room temperature pulsed I-V and low frequency noise measurements of gate and drain currents of AlGaN/GaN HEMTs have been investigated under different bias conditions on two devices showing identical drain current and different gate current levels. The results show a correlation between two non-destructive measurement techniques applied on devices under test.

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1. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are of great interest for microwave circuits (power amplifiers, robust low noise amplifiers, high frequency switches,...) because of their properties matched for high power, high frequency and low noise applications [1]. If the first reliability studies were focused on the drain current behavior in the channel, it is now largely assumed that leakage currents are major indicators of the state of a device, and are more prone to reveal their future degradation. The improvement of the reliability for a technology must be achieved through the close control of the leakage current. The gate control zone is then the sensitive area where the performances of the device can be optimized as it determines the drain current flowing in the channel during the life of the device. The present paper is not related to reliability purpose but focuses on electrical and noise analysis on the gate and drain terminals to evidence specific mechanisms induced on leaky and non-leaky devices. Thus, the qualification of these devices needs rigorous experiments on the drain as well as on the gate current.

The paper focuses on the electrical and low frequency noise characterization of devices issued from an industrial process:

(a) Pulsed I-V measurements are presented on the gate and drain currents. These measurements provide information about traps activated under non-isothermal conditions [2-4].

(b) Low frequency noise (LFN) measurements are performed on gate and drain terminals. This technique is convenient for getting fine information about the nature of the defects and their location in the device [5-7].

These techniques are performed on a set of devices featuring high and low leakage levels. Next, the results are proposed for one representative device from each set. This study highlights the impact of gate conduction mechanisms over the transistor behavior despite the quasi-similar drain current values measured for both transistors. Drain current is also investigated as defects can impact the dynamic characteristics of the device.

The paper is organized as follows. In section 2, we briefly describe the device structure and the experimental conditions used for the two techniques. Sections 3 and 4 report on the pulsed I-V and LFN measurements respectively. Section 5 sets the conclusions drawn from the two techniques.

2. Devices under test and experimental conditions

AlGaN/GaN HEMTs under study ($4\times400\mu m \times 0.5\mu m$) are grown on SiC substrate by MOCVD, and feature 18% of Al content. Two devices are tested presenting differences in the gate leakage current: T1 with low leakage current (265 µA/mm @ V_{DS}=50V and V_{GS}= -7V) and T2 with high leakage current (855 µA/mm, same biasing conditions). These devices are representative of each set of leaky and non-leaky devices, featuring a Gaussian distribution on the I_{GS} values (at a given quiescent point V_{DS}, V_{GS}).

The pulsed I-V measurements are carried out at different quiescent bias (QB) conditions (V_{GS0}, V_{DS0}) in order to quantify the gate and drain lag phenomena [2]:

(1)   (V_{GS0}, V_{DS0}) = (0V, 0V),
(2)   (V_{GS0}, V_{DS0}) = (-3V, 0V),
(3)   (V_{GS0}, V_{DS0}) = (-3V, 20V),

To quantify the gate-lag effects, measurements carried out with conditions (1) and (2) are compared.

The drain-lag effects are quantified by comparing measurements performed with conditions (2) and (3). A pulse width of 300 ns is used with a duty cycle of 0.01% to reduce self-heating effects.

LFN measurements are performed in a shielded room to reduce interferences with the external environment. Outside this room, the measurements are recorded on a computer connected to the HP89410A analyzer. A set of bias-Tees are used to prevent from possible oscillation of the devices. To set the bias point, gate and drain-biasing resistors are connected to batteries to reduce the excess noise sources which may be caused by a power supply. A Model 5182 transimpedance preamplifier (for the gate current LFN measurements) and a Model 5184 voltage preamplifier (for the drain current LFN measurements) are used to amplify the output signal level measured on the analyzer. The measurements are carried out at room temperature in the frequency range 1 Hz -100 kHz.

3. Pulsed I-V measurements: Gate-lag and drain-lag effects

3.1. Gate lag effects

The gate-lag (GL) is a delayed response of the drain current with respect to the gate voltage variation [8].

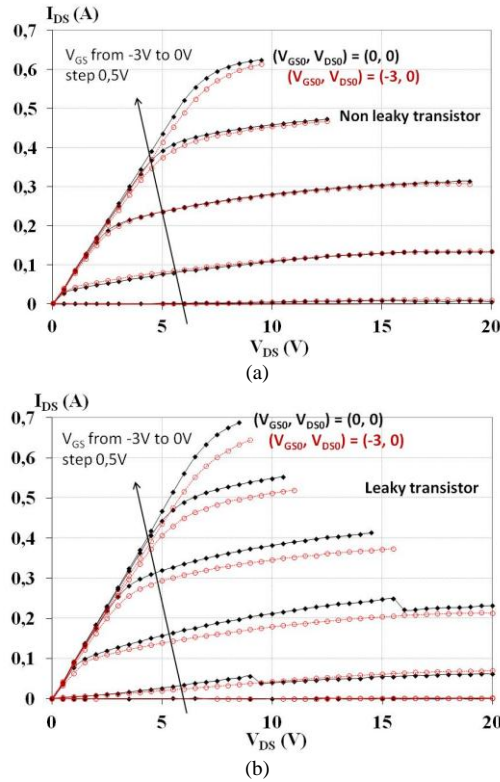Figure 1 shows 300 ns pulsed I-V measurements of

(a)

(b)

Fig. 1. 300ns pulsed I-V measurements of the AlGaN/GaN HEMTs at QB conditions (1) and (2). (a) non-leaky transistor T1.(b) leaky transistor T2.

a non-leaky and a leaky HEMTs (Figure 1a for T1 and Figure 1b for T2) using the two quiescent bias conditions (1) and (2): from Figure 2, it is obvious that the non-leaky HEMT presents a gate lag ratio lower than 5% in all the V_{DS} range and that the gate lag is more pronounced for the leaky device over the same V_{DS} range, which can hamper the large gate voltage variations under class A amplification.
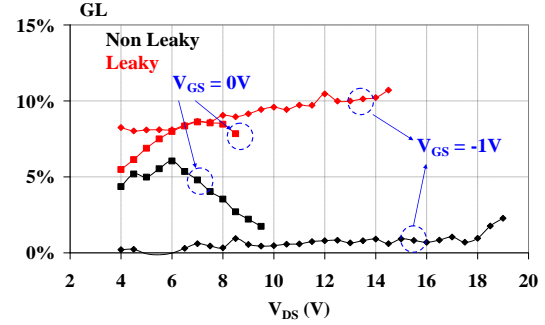

Fig.2. Relative gate lag (GL) between quiescent points @V_{GS0}=0V & V_{GS0}=-3V versus V_{DS} (data extracted from measurements shown in Figure 1), for leaky and non-leaky devices.

3.2. Drain-lag effects

The drain-lag (DL) is a delayed response of the drain current with respect to the drain voltage variation.

Figure 3 shows 300 ns pulsed I-V measurements of a non-leaky and a leaky HEMTs (Figure 3a for T1 and Figure 3b for T2) using the two quiescent bias conditions (2) and (3). T1 and T2 present approximately the same decreasing evolution of the drain lag ratio over the V_{DS} measurements range, with less than 10% of variation between the two extreme biasing conditions (V_{DS}=0V, V_{DS}=20V) over the investigated V_{DS} values. Moreover, the magnitude of the drain-lag is approximately identical for the leaky and non-leaky devices as it differs from less that 3% over the V_{DS} and V_{GS} investigated range.

3.3. Discussion

The pulsed I-V characteristics of T1 show lower drain current dispersion between (V_{GS0}, V_{DS0}) = (0V, 0V) and (V_{GS0}, V_{DS0}) = (-3V, 0V) than T2. This higher gate-lag effect for the leaky device is attributed to traps with time constants higher than 300ns (that is the pulse width) and lower than the period duration (@ 30µs).

The pulsed I-V characteristics of T1 and T2 between (V_{GS0}, V_{DS0}) of (-3V, 0V) and (-3V, 20V) show almost the same drain lag magnitude.
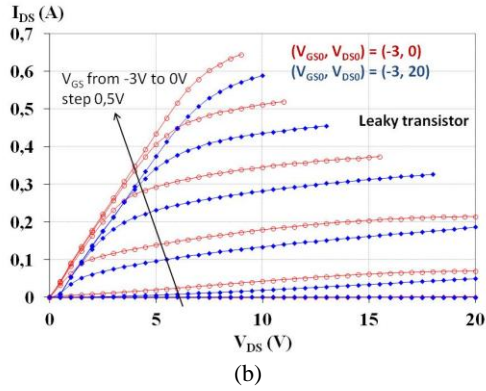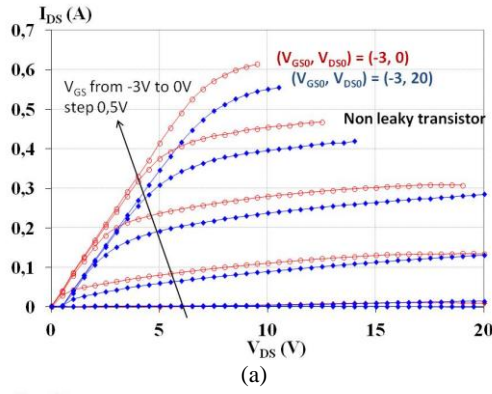
Fig.3. 300ns pulsed I-V measurements of the
AlGaN/GaN HEMTs at QB conditions (2) and (3).
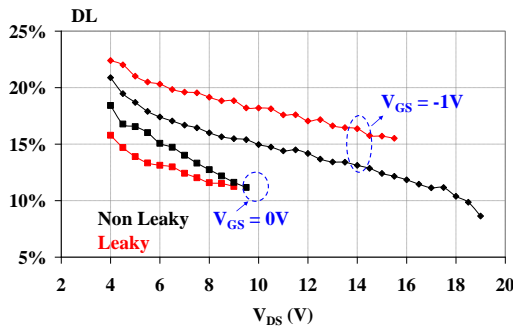(a) non-leaky transistor T1.
(b) leaky transistor T2.

Fig.4. Relative drain lag (DL) between quiescent points @
V_{DS0}=0V & V_{DS0}=20V versus V_{DS} (data extracted from
measurements shown in Figure 3), for leaky and non-leaky
devices (for V_{GS}=0V and V_{GS}=-1V).

Moreover, the comparison at all quiescent bias
conditions between the two transistors shows that the
pulsed drain current is always slightly higher for T2
than for T1. This means higher output power for the
leaky transistor. From the analysis between the
transconductance gains, no difference is noticeable
from DC measurements over a wide temperature range
(100K-400K) for the leaky and non-leaky devices.
However, transconductance gain g_m from pulsed
measurements at ambient temperature features large

difference versus gate voltage (g_{m-max}, V_{th}) (figure 5).
As the dynamic transconductance gain is not higher for
the leaky device, and considering identical
piezoelectric and spontaneous charges for the leaky and
non-leaky devices (same structures), this increase in the
current for the leaky transistor T2 can be attributed to a
higher density of charges n_i. This manifestation on
pulsed measurements (I_{DS}-V_{DS}, g_m) can be explained
through the compensation of donors by dynamic
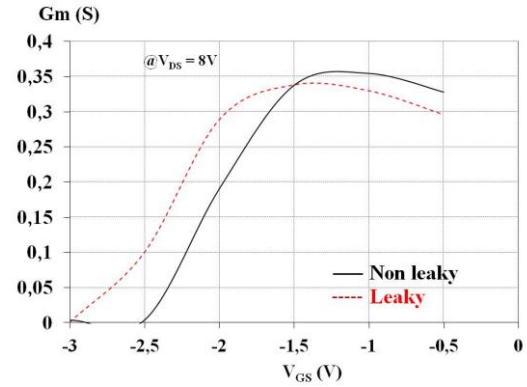charges (dynamic change of the space charge region
depth in the 2DEG).

Fig.5. pulsed transconductance gain versus V_{GS} for leaky
and non-leaky devices @V_{DS}=8V.

Moreover, a shift between the ohmic curves at
V_{DS}=0V and V_{DS}=20V (Figure 3a and 3b) can be
observed. This shift has been found to be reproducible
and depends on the pulse width and on the V_{DS0}
quiescent voltage. This can be modeled by an intrinsic
voltage generator between drain and source that
increases by -0.5V when V_{DS0} varies from 0V to 20V
for both leaky and non leaky devices. The origin of this
V_{DS0}-activated mechanism is not yet identified.

From Figure 4 on the relative drain lag values
(expressed in %), two different trends can be sorted out
at V_{GS}=0V and at V_{GS}=-1V:
(a)   At V_{GS}=0V, more pronounced lag effects are
      visible in the ohmic region (low V_{DS} values),
      whereas the difference decreases when V_{DS}
      measurement increases. An identical relative drain
      lag is obtained (11%) for leaky and non-leaky
      devices at a measurement condition of V_{DS}=10V.
      This former condition concerns a situation when the
      relative voltage variation from quiescent to
      measurement ($|V_{DS0}-V_{DS}|$) is the same (i.e. same
      difference between the quiescent condition,
      V_{DS0}=0V and V_{DS0}=20V, and the measurement
      point at V_{DS}=10V). Here are under concern traps
      between gate and drain, probably located at the
      AlGaN/GaN interface. More information can be
      found in [4], where gate lag effects are discussed
      (i.e. same mechanisms between G-S region).

(b) At V_{GS}=-1V, the leaky and non-leaky devices feature the same behavior (same slope of the relative drain-lag regression versus V_{DS}). Thus it can be assumed that another mechanism is superimposed to the previous one. Here, the same mechanism is involved for both the leaky and non-leaky devices under the gate biasing conditions V_{GS}=0V, even if the lag effect is more pronounced for the leaky device (more traps activated).

4. Gate and drain low frequency noise measurements

4.1. Gate current noise spectral density

The LFN measurements on gate and drain terminals are performed at room temperature. Figure 6 shows the gate current noise spectral density (S_{IG}) of non-leaky (T1) and leaky (T2) transistors at V_{GS}=-3V, V_{DS}=8V and V_{GS}=-5V, V_{DS}=8V. A difference in the noise level is noticed as T2 presents a noise level 3 decades higher than the spectra related to T1. Moreover, the spectra shape (i.e. noise sources contributing to the overall noise) differs for the two devices, revealing different conduction mechanisms for T1 and T2. While the 1/f noise source of the non leaky device is only masked at high frequencies (frequency>1kHz), the 1/f noise source cannot be extracted from the spectra for the leaky device: a large number of traps (GR centers) are revealed by the S_{IG} spectra of T2. Thus, the power current law S_{IG}~I_G^x does not evolve with the same x index for the leaky and non leaky devices [9].
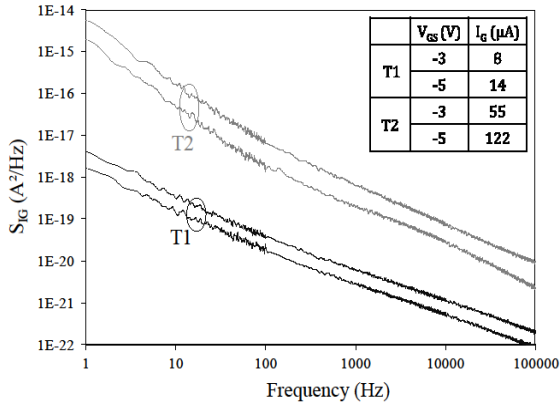

Fig. 6. Gate noise current spectral density of the AlGaN/GaN HEMTs (T1: non-leaky transistor and T2: leaky transistor) biased at V_{GS}=-3V and -5V.

4.2. Drain current noise spectral density

Another aspect concerning the defects in the device is the study of the LFN on the drain access. Figure 7 presents the low frequency noise measurements performed on the drain current (S_{ID}) for T1 and T2.

Both transistors feature the same S_{ID} level (for the same I_{DS} current): the two spectra of T1 and T2 are quasi-superimposed, in spite of a difference of less than one decade at low frequencies between 10 Hz and 100Hz due to more pronounced GR centers effect for the leaky device [9]. These GR centers (time constants between 0.01s and more than 1s) measured under isothermal conditions can be related to the defects discussed in section 3.3.
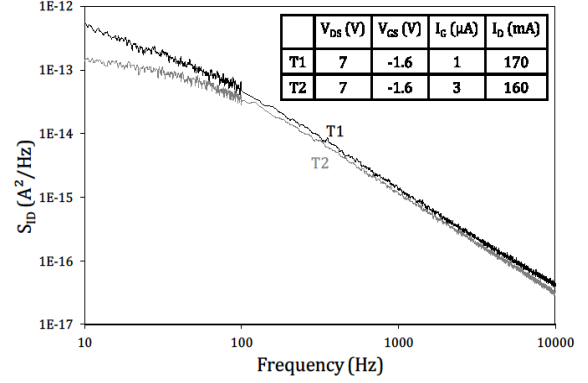

Fig. 7. Drain noise current spectral density of the AlGaN/GaN HEMTs (T1: non-leaky transistor and   T2: leaky transistor) biased at V_{GS}=-1.6V and V_{DS}=7V.

Figure 8 reports on the drain LFN measurements of three samples from the same set of devices (referred as T1 in this paper: non-leaky devices). The obtained results can be considered as statistically relevant. Moreover, the LFN drain current noise spectra are known to be an accurate prober of the crystal defects in the transistor: the absence of dispersion stands as a good indicator of the homogeneity of the devices under test. As shown in Figures 8 and 9, thermally activated defects are evidenced for three different biasing conditions (temperature increases when P_{DC}=$I_{DS}.V_{DS}$ increases, at constant V_{DS} when I_{DS} varies with V_{GS}).
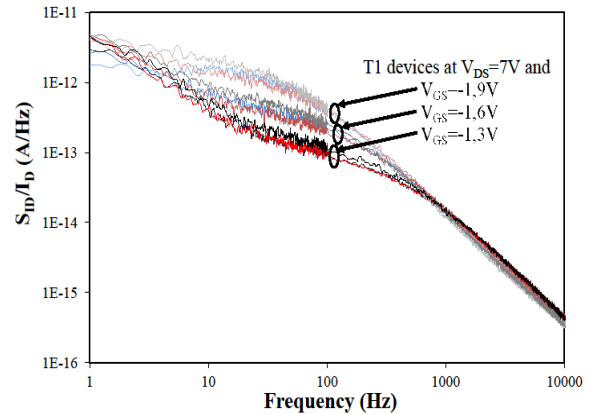

Fig. 8. Drain noise current spectral densities normalized versus drain current for three T1-type devices. The measurements are performed at constant V_{DS} value of 7V and at V_{GS}=-1.9 to -1.3V with ΔV_{GS}= 0.3V.
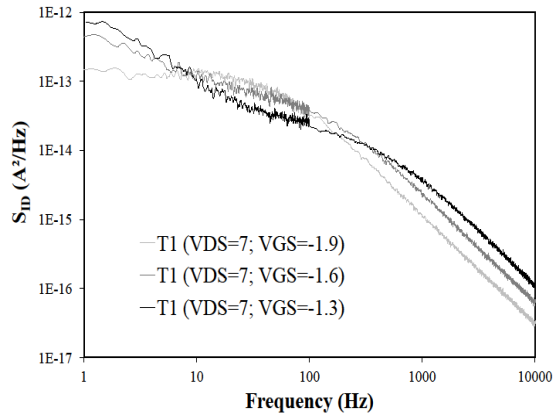
Fig. 9. Drain noise current spectral densities of T1 at V_{DS}=7V and at V_{GS}=-1.9 to -1.3V with ΔV_{GS}= 0.3V.

4.3. Discussion

The insets in Figures 6 and 7 indicate the difference between the gate currents of the devices under test (14 µA for T1 and 122 µA for T2 at V_{GS}=-5V and V_{DS}=8V), whereas the devices feature quasi-identical drain currents values. According to Vandamme and al. [10-11], devices with slight differences in drain current noise can have quite a different gate current noise. Actually, these results are quite consistent with pulsed electrical characterizations, as the numerous traps revealed by LFN on the gate terminal can reasonably be correlated with a higher level of gate lag on the leaky devices. These traps act as trapping-detrapping processes with time constants ranging from few microseconds to some seconds (also revealed by pulsed I-V transient characterizations). The surface passivation and the mastering of the gate Schottky diode are key points concerning the performance and the reliability of the devices, through a reduction of traps and leakage currents. Concerning the drain terminal, no strong difference is noticed between leaky and non-leaky sets of devices, in spite of numerous GR centers revealed by LFN characterization in the lower frequency band. Traps have been located at the interface between the AlGaN and GaN layers, and are activated with the extension of the space charge region between gate-source and gate-drain regions when the respective voltages V_{GS} and V_{DG} are applied [4]. Moreover, no correlation is found between noise current densities of gate and drain terminals.

5. Conclusion

The paper presents a synthesis issued from different experimental techniques performed on the gate and drain currents of AlGaN/GaN HEMTs. Pulsed electrical measurements and low frequency noise measurements evidence the importance in mastering the gate Schottky diode, and specially lowering the gate leakage currents, to lower the lag effects and the noise sources (GR centers). The gate-lag effect and GR centers have been associated to the ionized donor states located on the surface [13] as well as to the trapping centers located in the barrier or in the buffer [8]. Despite the importance of the drain access and hence of the drain current, the gate leakage current is a major indicator to follow up; the results indicate that the gate technological process remains a critical issue for the qualification of competitive and reliable GaN technologies. However, at this stage of the development, the devices feature an elevated median time to failure (MTTF) at 3.10^7 (resp. at 2.10^6) hours for a junction temperature of 175°C (resp. 200°C) [13].

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