Reliable GPS position on an unreliable hardware
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OBJECTIVES

This work addresses the fault tolerance topic in the GPS context. Starting from a noiseless GPS receiver, redundant mechanisms can be added to design a more resilient GPS receiver in the presence of errors due to process, voltage and temperature (PVT) variations [1]. These mechanisms are based on different layers of abstraction to guarantee a mutual trade-off of system performance (quality of the position given by the GPS receiver), hardware reliability and implementation complexity. An application-specific integrated circuit (ASIC) will be designed with two versions of the GPS receiver: the standard version, and a complex version where fault-tolerant techniques are added to make the GPS receiver more tolerant to errors.

REFERENCES


INTRODUCTION

- There is continual motivation to reduce power consumption and extend battery life of mobile devices.
- Power consumption and device lifetime can be improved by operating at minimal supply voltage, which increases the likelihood of momentary/persistent faults.
- GPS satellite signals are made of three components: spreading code, carrier and navigation message.
- Tracking GPS satellite signals evolves three main processes:
  - GPS receivers use, Numerically controlled oscillators (NCO), to produce a local copy of the carrier of incoming satellite signals. Moreover, copies of spreading codes of GPS satellites are produced, locally, by two 10-stage LFSR (Linear feedback shift register) modules, designated G1 and G2.
  - A correlation function is computed every 10 ms between local signals and incoming signals. A maximum correlation output is achieved when the two signals are time aligned.
  - Two feedback loops are used to update the local generated signals over time, since satellites are in continuous motion and the receiver is also dynamic. Each loop is made of discriminators and filters.

RELIABLE GPS POSITION ON AN UNRELIABLE HARDWARE

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DESIGN OF THE SIMULATION PLATFORM

The GPS receiver algorithm was first designed with the MATLAB high level software. Then, an implementation of the GPS receiver algorithm is done for an FPGA target to explore low level performances compared to the high level Matlab performances. The implemented platform can be split into three main parts:

- User interface: This represents the space from where the FPGA is controlled.
- Signal source file: Signal received from more than 4 GPS satellites, over a significant period of time, are stored in a file. This file is added in the memory of an FPGA to replace a real-time receiving process of a GPS receiver.
- FPGA target: This will contain the hardware description of the acquisition and the tracking algorithms for a GPS receiver. It contains also a micro-blaze that manages the communication between the user interface and the hardware description of the GPS receiver.

REFERENCES