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To cite this version:

HAL Id: hal-01325114
https://hal.archives-ouvertes.fr/hal-01325114
Submitted on 1 Jun 2016

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Mixed-Signal PI Controller in Current-Mode DC-DC Buck Converter for Automotive Applications

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Abstract—This paper proposes a fully-integrated solution for the PI compensation circuits in current-mode DC-DC converters used in automotive applications. In such applications, the switching frequencies are low and hence conventional PI compensation circuits employ large capacitors. The proposed analog/mixed-signal PI comprises an analog proportional amplifier and a digital integrator. The analog proportional amplifier provides the required response time and maintains system stability. The digital integrator block is used to eliminate the output voltage steady-state error. Simulink is used to model the proposed DC-DC buck converter on the system level. The proposed system is verified by full system level simulation. The digital part is synthesized with HDL coder and laid-out using 0.35 μm CMOS technology. The estimated silicon area of the proposed solution is about 0.1 mm². This result highlights the simplicity and the capacity for integration of the proposed control loop along with its potential for seamless implementation into pre-existing solutions with minor modifications.

I. INTRODUCTION

Switching mode power supplies (SMPS) are widely used in automotive applications. They provide stable and robust power supplies with different voltages for the diverse electronic circuits on-board. The switched-mode power supplies are classified based on the feedback control loop as voltage-mode control or current-mode control. The former is based on sensing the output voltage. Such control loop contains two poles that are conventionally compensated by Proportional-Integral-Differential (PID) circuit. The main function of this compensation circuit is to maintain the desired loop gain crossover frequency and phase margin, hence preserving the loop stability. In addition to complex control dynamics, the voltage-mode SMPS needs techniques to limit the inductor current during start-up (i.e., soft-start techniques) and overload conditions (i.e., current sensors to sense the inductor current).

On the other hand, the current-mode is based on sensing the output voltage and the inductor current. The current-mode loop has only one dominant pole and another pole near the switching frequency [1]–[3]. The key advantages of the current-mode control are simple dynamics due to the presence of one pole and inherited current limiting. Sensing the inductor current with minimum losses is the major challenge for such control loops.

The compensation circuit can be purely analog or digital. The analog compensation circuits are commonly used for their stability and minimum delay. However, in high-voltage automotive applications, the switching frequencies are in the range of hundreds of kHz [4] in order to limit electromagnetic interference (EMI) emissions. In such low frequencies, the implementation of proportional-integral (PI) compensation circuit requires capacitance in order of nF which cannot be integrated.

Digital compensation circuits allow the implementation of complex control schemes and the dynamic control of the systems [5]. However, digital control suffers from signal processing delay and hence it requires a relatively high clock frequencies with respect to the switching frequencies [6]–[9]. Higher clock frequencies increase the electromagnetic emissions levels, which are highly undesirable for automotive applications. Besides, the implementation of Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) at such high frequency is power hungry solution.

The aim of this paper is to propose an analog-mixed approach of PI compensator for current-mode control used in buck DC-DC converter adequate for automotive applications. In this proposed system, the proportional part is implemented as analog circuit to maintain the required crossover frequency. The integrator part is implemented in digital domain to compensate the steady state error. The analog-mixed solution relaxes clock speed requirements on the ADC, DAC, and digital circuits and can be fully integrated.

The paper is organized as follows, Section II describes the conventional control architecture for the current-mode SMPS. Section III shows the proposed mixed PI control system operation and implementation. Simulation results are reported in Section IV. Section V concludes the paper.

II. CONVENTIONAL CONTROL FOR CURRENT-MODE BUCK CONVERTERS

A simplified peak current-mode control DC-DC buck converter is shown in Figure 1. To sense the output voltage $V_{out}$, it is scaled by a divider circuit $H_{divider}$ and compared to a reference voltage $V_{ref}$ providing an error signal $v_{e}(t)$. An analog PI compensator is used to integrate and amplify the error signal and generate the control signal $v_{c}(t)$. This $v_{c}(t)$ is converted into a current signal to ease the subtraction of the compensation ramp signal. The compensation ramp signal...
is used in order to prevent the subharmonic oscillations when the duty cycle exceeds 50% [2].

For the inductor current sensing, transistor M3 acts as a sense FET. Its aspect ratio is a portion of high-side (HS) switch M1. A current gain is used to achieve reasonable ratios between the sense FET and the high-side switch. The comparator turns off the HS switch when \( V_g > V_x \) but \( V_y = V_{in} - i_{sense}(t) \times R_M3 \) and \( V_z = V_{in} - i_L(t) \times R_M1 \) where \( R_M1 \) and \( R_M3 \) are the on resistance of the HS switch M1 and the sense FET, respectively.

Hence, the condition for switching the HS switch off can be expressed as:

\[
i_L > i_{sense} \times \frac{R_M3}{R_M1}
\]  

In this example, the ratio \( R_M3/R_M1 \) is 2000. Hence, \( i_{sense} \) can be scaled down 2000 times compared to \( i_L \). The switching frequency is determined by the clock (CLK) used to turn on the HS switch each switching cycle.

To illustrate the main issue concerning the analog PI circuit, a conventional PI circuit is shown in Figure 2 [10]. The transfer function is given as

\[
A(s) = \frac{\hat{v}_c}{\hat{v}_{in}} = \frac{1}{H_{divider} \times V_{o}} = g_m \times R_z \frac{s + 1/(C_z \times R_z)}{s + 1/(C_z \times R_o)} \text{ for } R_o >> R_z
\]

From this transfer function, a proportional gain of \( g_m \times R_z \) is designed to get the desired loop gain crossover frequency. The crossover frequency is set to be less or equal to 20% of the switching frequency in order to avoid amplifying switching ripples. A zero located at \( \omega_z = 1/(C_z \times R_z) \) compensates the dominant pole of loop gain approximately at \( \omega_p = 1/(R_{load(\text{max})} \times C) \). If the switching frequency \( f_{\text{switching}} \) is 330 kHz, the crossover frequency is designed to be 40 kHz. In order not to affect the phase margin, the low frequency zero \( f_z \) should be located at least less than 1/10 of the crossover frequency, i.e., \( f_z = 4 \) kHz. For \( R_z = 10 \) k\( \Omega \), the capacitor needed \( C_z \) is about 4 nF which is an off chip component that increases the cost of the converter.

### III. PROPOSED ANALOG-MIXED PI CONTROL FOR CURRENT MODE BUCK CONVERTERS

The analog PI system level is shown in Figure 3. The block diagram can be separated in two paths:

1) Path ‘A’ which represents the proportional component \( (V_{ep} = K_p \times V_c) \) of the PI circuit used to set the crossover frequency of the control-to-output loop gain.

2) Path ‘B’ which represents the integral component \( (V_{e\text{integ}}) \) in the PI circuit with gain \( (K_i/K_p) \).

The transfer function of the ideal system versus the transfer function of the circuit level assuming infinite output resistance is given by:

\[
\frac{\hat{v}_{out}}{\hat{v}_{in}} = g_m \times R_z \frac{s + 1/(C_z \times R_z)}{s} = K_p \frac{s + K_i/K_p}{s}
\]

From equation 3, the zero corner frequency depends on the value of the capacitor \( C_z \) which is located in path ‘B’. The proposed solution is to implement the proportional path ‘A’ in analog amplifier and to implement the integral path ‘B’ using a digital integrator. Figure 4 shows the integral path with a certain gain to have a response comparable to the analog integrator. Hence, the off chip capacitor \( C_z \) will not be used.

The integral path consists of an ADC, a digital integrator and a DAC. First, the ADC is realized by a discrete-time single bit \( \Sigma \Delta \) modulator. The \( \Sigma \Delta \) modulator is selected to simplify the design and reduce the silicon area. Since the signal-of-interest is the error signal \( v_e(t) \) which is a low frequency
A single bit ΣΔ modulator is used with a sampling frequency of 5.28 MHz. This sampling frequency is used to achieve a high resolution after decimation. The decimation ratio is 256 and the number of bits at the output is 8 bits. Hence, the integrator response time equals to 45 µs which results in an acceptable transient response for the system.

Figure 7 shows the output voltage at minimum load current with only proportional amplifier and with PI compensator.

### TABLE I: DC-DC buck converter specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>5 – 15 V</td>
</tr>
<tr>
<td>$I_{load}$</td>
<td>0.05 – 0.6 A</td>
</tr>
<tr>
<td>$T_{switching}$</td>
<td>330 kHz</td>
</tr>
<tr>
<td>Inductor value</td>
<td>105 µH</td>
</tr>
<tr>
<td>Capacitor Value</td>
<td>33 µF</td>
</tr>
<tr>
<td>Inductor series resistance DCR</td>
<td>50 mΩ</td>
</tr>
<tr>
<td>Capacitor series resistance ESR</td>
<td>35 mΩ</td>
</tr>
</tbody>
</table>
Fig. 7: Steady-state output voltage at (I_{load} = 0.05A) (a)Proportional amplifier only, (b) Analog PI compensation, (c) proposed analog-mixed PI compensation

Fig. 8: Load step response I_{load} = 0.05A to 0.5A showing the effect of changing the digital integrator gain

PI compensator eliminates the steady-state error voltage and keeps the error in output voltage within 3%. The proposed circuit shows idle pattern oscillation due to the presence of relatively low DC voltage at the input of the ΣΔ ADC. This pattern is limited to a very small value that can be tolerated by the system.

For the proposed solution, the integrator gain (K_i/K_pT) can be changed to control the settling time of the output voltage. In Figure 8, the output voltage response due to a pulse change in the load resistance from 50Ω to 5Ω for different integrator gains. As the integrator gain reduces, the settling time increases.

In order to estimate the area of the proposed system, VHDL code for the digital part is generated directly from the Simulink using the HDL coder tool. Then, it is synthesized and laid out using 0.35 µm HV CMOS technology. The estimated area is about 0.05 mm² and the reported number of gates used is 180 gates, with an estimated power consumption of 0.35 mW at a supply voltage of 5 V. An estimation for the area of the sigma-delta ADC is 0.017 mm² and the DAC area is about 0.034 mm². Hence, the total estimated area is about 0.1 mm². These metrics highlight the simplicity and the integration potential of the proposed control loop.

V. CONCLUSION

An integrated analog-mixed PI compensation circuit has been proposed for automotive applications. The proposed system attempts to alleviate the usage of an external capacitor in the pure analog compensation circuit along with relaxing clock speed constraints of the digital circuit in the fully digital PI solutions. Simulation results prove the functionality of the proposed system. The digital circuit occupies an area of 0.05 mm² in the system and its power consumption can be neglected. The whole solution area is estimated to be approximately 0.1 mm². The proposed solution can be easily mapped to different DC-DC buck converters specifications.

ACKNOWLEDGMENT

This work has been sponsored by the European commission under the European FP7 AUTOMICS project.

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