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A thermal-Aware Laser Tuning Approach for Silicon Photonic Interconnects

Hui Li, Alain Fourmigue, Sébastien Le Beux, Ian O’Connor, and Gabriela Nicolescu

1 Lyon Institute of Nanotechnology, INL-UMR5270
Ecole Centrale de Lyon, Ecully, F-69134, France
2 Computer and Software Engineering Dept.
Ecole Polytechnique de Montréal, Montréal (QC), Canada

Abstract—Optical interconnect is an emerging technology considered as one of the key solutions for future generation on-chip interconnects. However, silicon photonic devices are highly sensitive to temperature variation. Under a given chip activity, this leads to a lower laser efficiency and a drift of wavelengths of optical devices (on-chip lasers and Microring Resonators (MRs)), which results in a higher Bit Error Ratio (BER). In this paper, for the first time, we propose to tune the laser injection current in order to align the wavelength of the emitted signals with the resonant wavelengths of the MRs. Our approach allows significant improvements of the power consumption with regard to the related approaches.

Keywords: silicon photonics interconnect, thermal simulation.

I. INTRODUCTION

Technology scaling down to the ultra-deep submicron domain enables the integration of hundreds of cores. In order to enhance connecting many cores, chip-level communication needs a new interconnect solution to bring down the power budget. On-chip silicon photonic interconnects are an emerging technology considered as one of the key solutions for future generations of many cores, providing high bandwidth and low latency. They are composed of CMOS-compatible on-chip laser sources, Microring Resonators (MRs), waveguide and photodetector. However, silicon photonic devices are highly sensitive to temperature variation induced by thermal effect over the chip, which is a major concern for the laser wavelength and MRs resonant wavelength. Consequently, the Signal to Noise Ratio (SNR) of the signals received by the photodetector decreases, which leads to a higher Bit Error Ratio (BER). This is further accentuated by the significant reduction of on-chip lasers efficiency as the temperature increases.

This paper proposes a thermal-aware tuning approach to overcome the wavelength variation induced by temperature variation, while achieving the targeted BER. The novelty of the approach relies on the tuning of the laser driver current, which ideally complements traditional methods such as MRs tuning and channel remapping [2][3].

II. PROPOSED LASER TUNING APPROACH

Figure 1 illustrates our approach in the context of a MWSR-(Multiple Writer Single Reader) architecture [1] with a single laser source, 2 writers and one reader. In [5], the authors explore the placement of shared on-chip lasers on a layer located on top of the optical interconnect. In our work, we work on distributed lasers that are located in the same layer with MRs, waveguide and photodetectors. For this purpose, we assume the use of CMOS-compatible laser sources such as Vertical-Cavity Surface-Emitting Lasers (VCSELs), for which the size is similar to the one of MRs [9]. As illustrated in Figure 1-a, ONI_m communicates with ONI_l: the MR in the intermediate ONI is turned OFF while the MR in ONI_m is in the modulation state (state OFF and ON to modulate data ‘1’ and ‘0’ respectively).

![Figure 1](image-url)

Figure 1: a) a MWSR channel with one wavelength and two writers, b) transmission without thermal variation (ideal scenario), c) transmission with MR tuning only (reference approach), d) transmission with MR and laser tuning (our approach).
Figure 1-b illustrates the ideal transmission of a data ‘1’ that occurs when there is no temperature variation along the communication path. The optical signal injected by the laser (which is characterized by a power \(P_{\text{laser}}\) and a wavelength \(\lambda_{\text{laser}}\)) crosses ONI\(_a\) and ONI\(_b\), propagates along the waveguide until ONI\(_c\) where it will be dropped to the photodetector (as illustrated by the blue transmission lines in the Figure 1-b). The power of the optical signal decreases along the path due to the waveguide propagation losses and the MRs crossing losses (blue line in Figure 1-b). From the received power \(P_{\text{pd,ideal}}\), the receiver sensitivity and the crosstalk (induced by other transmitting signals at different wavelengths, not illustrated here for sake of clarity but taken into account in our models), the BER is estimated.

1) Traditional tuning approach: In case of temperature gradient over the communication path, the resonant wavelength of the MRs will drift (see the red transmission lines in Figure 1-c) while the wavelength of the emitted signal \(\lambda_{\text{laser}}\) remains the same in case off-chip lasers are considered. Without compensating effect of this drift, the misalignment between the signal wavelength and the MRs resonant wavelengths leads to significantly increased BER. To overcome this effect, the MRs along the waveguide are tuned back to their initial positions (the grey transmission lines in Figure 1-c) using thermal tuning or voltage tuning. The post-tuning signal transmission is illustrated by the blue line in Figure 1-c: the received optical power is slightly lower than in the ideal scenario due to marginal wavelengths misalignment. The MRs tuning power depends on their temperature drift \(\Delta T_{\text{MR}}\) and the thermal sensitivity coefficient \(\rho_{\text{MR}}\). The total power consumption of the link is given by the sum of the laser power consumption \(P_{\text{laser}}\) and the MRs tuning power \(\sum P_{\text{MR}}\).

2) Proposed tuning approach: In order to reduce the total link power consumption, we consider tuning the driver current \(I_{\text{laser}}\) in the context of on-chip lasers. As illustrated in Figure 1-d, the laser power consumption will move from \(P_{\text{laser}}\) to \(P'_{\text{laser}}\) and the emitted signal is tuned from \(\lambda_{\text{laser}}\) to \(\lambda'_{\text{laser}}\). Therefore, under the same temperature gradient considered in Figure 1-c, the MRs wavelengths need to be tuned to \(\lambda'_{\text{laser}}\), instead of \(\lambda_{\text{laser}}\), to keep the BER at an acceptable level. Since the distance is lower, the MRs tuning power is lowered. As a drawback, the power of the emitted signal is reduced, meaning that a tradeoff needs to be defined in order to reach the target BER while decreasing the total power consumption of the channel. It is worth noticing that, although the approach is illustrated with a 1-wavelength channel, it is generic and it can be applied to WDM channels (we investigate 4-wavelength channels in the results section). Moreover, it is complementary to related approaches providing channel remapping [2][3] that we have adapted to minimize the tuning power instead of the tuning distance.

III. RESULTS

We evaluate our approach with a MWSR network used to interconnect 12 interfaces (i.e. 12 channels with 11 writers and 1 reader per channel) and 4 wavelengths (i.e. 4 on-chip lasers per channel and 4 MRs per writer). Following the method described in [9], the silicon photonic interconnect is placed on top of the SCC chip and thermal simulations are performed using lCTherm [6]. From the resulting thermal map, the proposed laser tuning approach is applied in order to i) evaluate the BER using the transmission models from [9] and ii) evaluate the total link power consumption \(P_{\text{tuning}}\) (including the laser power consumption \(P_{\text{VCSEL}}\) and the MR tuning power \(P_{\text{MR}}\)).

![Figure 2: Tuning power (P_tuning) and BER for a MWSR interconnect with 12 interfaces, 4 wavelengths per channel, with FSR=59nm, m=16, thermal efficiency of the voltage tuning TE_{VCSEL}=0.13mW/nm, thermal efficiency of the thermal tuning TE_{IcTherm}=0.24mW/nm [7][8].](image)

We first run thermal simulations under a homogeneous 25% chip activity, with a laser power consumption \(P_{\text{VCSEL}}\) ranging from 1mW to 20mW (obtained by tuning the laser injection current \(I_{\text{laser}}\)). From the thermal map, we evaluate the total power required to align the MRs resonant wavelengths with the emitted signals and we evaluate the worst-case BER among all the channels in the network, as illustrated in Figure 2. For small laser injection current (i.e. \(P_{\text{VCSEL}}\) ranging from 1mW to 4mW), the optical power of the emitted signal is too low to compensate the channel losses, which results in a high BER. Then, the communication quality improves as the laser injection current increases: the BER reaches its optimal value at \(P_{\text{VCSEL}}=9mW\). By considering a static design method, the corresponding injection current will be selected to ensure the best communication quality. Above 9mW, the laser efficiency decreases due to the increase of the local temperature, leading to a higher BER. The channel power consumption is also given in the figure. It is composed of the laser power consumption (simply reported from the x-axis) and the MRs tuning power.

| Table 1: Power consumption reduction: with laser tuning wrt. w/o laser tuning |
|---------------------|---|---|---|
| Chip activity | Target BER 25% | 20% | 10% |
| \(10^{-12}\) | 21% | 42% | 52% |
| \(10^{-13}\) | 32% | 42% | 62% |

We evaluate the potential gain of the proposed laser tuning approach with the traditional one (for which only MRs tuning is possible). For this purpose, we first set the laser power consumption to 9mW in order to reach a targeted 10\(^{-12}\) BER for the highest considered chip activity (30% in this example). We then reduce the chip activity to 25%, 20% and 10%, and we evaluate the achievable power reduction while still
reaching $10^{12}$ BER. As illustrated in Table 1, up to 52% reduction is obtained for a 10% chip activity. In case a $10^{-9}$ BER turns to be acceptable (i.e., in order to match the requirements of an application to be executed), the power consumption can be further decreased. These results demonstrate the significant power reductions achievable by using chip activity-aware methods.

IV. CONCLUSION

In this paper, we propose a laser tuning approach in fully integrated silicon photonic interconnects. The proposed approach allows drastic reductions of the power consumption when the chip activity decreases and when the application BER requirements are lowered. In future work, we will investigate run-time approaches to calibrate the laser injection current.

REFERENCES


BIOGRAPHY OF THE SPEAKER

Ian O’Connor (IEEE S’95-M’98-SM’07) is Professor for Heterogeneous and Nanoelectronics Systems Design in the Department of Electronic, Electrical and Control Engineering at Ecole Centrale de Lyon, France. He is currently head of the Heterogeneous Systems Design group at the Lyon Institute of Nanotechnology. Since 2008, he also holds a position of Adjunct Professor at Ecole Polytechnique de Montréal, Canada. His research interests include novel computing architectures based on emerging technologies, associated with methods for design exploration. He has authored or co-authored around 200 book chapters, journal publications, conference papers and patents, has held various positions of responsibility in the organization of several international conferences and has been workpackage leader or scientific coordinator for several national and European projects. He also serves as an expert with the French Observatory for Micro and Nano Technologies (OMNT), IFIP (International Federation for Information Processing) WG10.5 (Design and Engineering of Electronic Systems), and ALLISTENE (Alliance for digital science and technology).