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An athermal measurement technique for long time constants
traps characterization in GaN HEMT transistors

A. Divay*, M. Masmoudi*, O. Latry*, C. Duperrier**, F. Temcamani*
*Normandie Université, University of Rouen, GPM UMR CNRS 6634, 76300 Saint Etienne du Rouvray, France , **University of Cergy, ETIS UMR 8051 CNRS, ENSEA, 95000 Cergy-Pontoise, France

Introduction
- The trap characterization techniques generally used on GaN HEMT transistors are limited by self-heating (DLTS, DLOS, ...) [1].
- An athermal method is proposed in order to measure long time constant traps in GaN HEMT transistors.
- Defects with time constants ranging from several ms to 1000s are observable with limitation of self-heating effects.

Principle of the measurement technique

- The drain bias is fixed (ohmic or saturation region).
- The gate bias is pulsed between two levels (0.2% duty cycle), the lower one being changed after an initial filling (trapping).
- The drain current is measured during the relaxation of traps between these two states.

Validation of the method using modeling

- Modeling of the electro-thermal source of the device using ADS (Advanced Design System).
- A generic trap activation energy is included in the model.
- The concept is validated even for high current densities (around 0.42 A/mm).
- The simulated temperature rise is ∆T = 0.4°C.

Measurements on AlGaN/GaN HEMTs on SiC substrate

- Different polarization protocol were used in order to characterize the trapping state in GaN HEMT transistors : in saturation and ohmic region.
- Time constants are found to be slower in the ohmic region.
- A trap at Ea = 0.65 eV is found at every protocol (not dependent on voltage) and is linked to gallium vacancies [2].
- Other defects are retrieved at 0.45, 0.86, 0.69 and 0.76 eV which are dependent on voltage and temperature.

Conclusion
- The measurement concept is validated by the simulation, the temperature rise during the measurement is estimated around 0.4°C.
- The various polarization protocols allow the measurement of traps in different localization and have shown several activation energies.
- A good precision on the extracted activation energies is obtained : ± 0.02-0.04 eV.

References