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# Modeling and Simulation of an Instrumentation Amplifier in High Temperature Using a VHDL-AMS Op-amp Model

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*Abstract*—**In this paper, an "architectural" description of an instrumentation amplifier (in-amp) is used to simulate its common mode rejection ratio (CMRR) and voltage offset (VOS) in high temperature (HT). The simulations are achieved by using two different models of an industrial op-amp: the familiar SPICE macro-model and a customized VHDL-AMS model. By simulating these two parameters in HT, we evaluate in this work dependency between the op-amp model and the in-amp model. This dependency is described first by reviewing theoretical equations. We compare finally the VHDL-AMS simulation accuracy to the SPICE simulation accuracy in HT.**

*Index Terms*—**Model, simulation, VHDL-AMS, SPICE, instrumentation amplifier, operational amplifier, high temperature, Common Mode Rejection Ratio, Voltage Offset**

## I. Introduction

Many industries (automotive, oil, aerospace, etc.) require electronic circuits and systems that operate in high temperature [1], [2]. Most of these industries need specifically instrumentation and measurement circuits in order to evaluate some industrial, physical or environmental parameters (such as temperature, pressure, position speed, etc.). For each parameter, there is a specific sensor that converts it to an electrical signal.

In the output of the sensor, an electrical signal will be conditioned by a set of analog and mixed-signal (AMS) electronic circuits (Fig. 1). This circuitry is called Analog-Front-End (AFE).

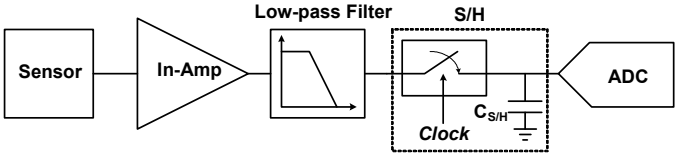



Figure 1. AFE architecture for instrumentation and measurement applications

It is well known that in HT range (temperature below 125°C); the behavior of AMS integrated circuits (ICs) can change considerably. Even if some specific AMS circuits dedicated to HT become more and more available on markets, most of industries still rely on the use of conventional electronics (electronics functioning in ambient temperature or in the standard temperature range of [-40°C, 125°C]). This can be explained by the high cost of the integration of new dedicated HT electronics and a lack of their technology master comparing to the conventional electronics. In order to not measure an erroneous or imprecise parameter, some circuits should be added to the AFE to compensate major temperature effects. Simulation will predict performance of AFE and the measurement accuracy after adding the compensation circuits. However, in order to obtain reliable simulation results, we should be sure that used models are accurate. Unfortunately, most of available models of industrial electronics belonging to conventional electronics are not accurate in HT. For instance, in [3], it was shown that an industrial op-amp SPICE model is not valid in HT. Instead, a VHDL-AMS was developed using a set of performances parameters in different temperatures. In [4], we have affirmed that a behavioral or mixed modeling can be a promising solution to overcome high temperature electronics modeling challenges. In this work, we use the already-validated op-amp model in [4] and [5] to simulate a 3 op-amp in-amp circuit. As it was shown in [5], by referring to the measurement results in HT, the VHDL-AMS simulation reproduces a lower mean error in HT compared to that caused by SPICE simulation [3]. That is why; we expect that VHDL-AMS in-amp simulation will lead to a more accurate result than the one by SPICE. The difference between the two errors is defined as the improvement of the simulation error. The simulations are dealing mainly with the CMRR parameter. However, some simulation results of the differential gain, the voltage offset and the saturation voltages are also given.

The organization of the paper is as following. In Section II, we remind the architecture of a 3 op-amp in-amp and review relations between op-amp parameters and in-amp parameters. The effect of the impedance and resistor mismatch is also described. In section III, we remind briefly the results of the validity study of op-amp SPICE and VHDL-AMS models in HT. In Section IV, we describe and comment the simulation results of the SPICE and VHDL-AMS in-amp models. Finally, in Section V, we conclude and give some prospects.

## II. 3 op-amp Instrumentation Amplifier

An instrumentation amplifier is a differential amplifier that is used in many instrumentation applications (industrial, biomedical, etc.) in order to amplify weak signals that outcome

from the sensor [6], [7], [8], [9]. The op-amp is the component key of an instrumentation amplifier. An in-amp is actually an interconnection network of at least one op-amp to some other components (mainly resistors). The number of used op-amps and the way with it op-amps were linked to other devices define the in-amp "architecture". Three architectures are especially frequently cited in the literature: mono-op-amp amplifier (called also differential amplifier), 2-op-amps in-amp and finally 3-op-amps in-amp. It was proofed in academic and industrial references that the 3-op-amps in-amp has the best performance especially for its high values of common mode rejection ratio, impedance and sensitivity to resistor mismatch. That's why we were interested in this study in modeling and simulating of this in-amp structure performance.

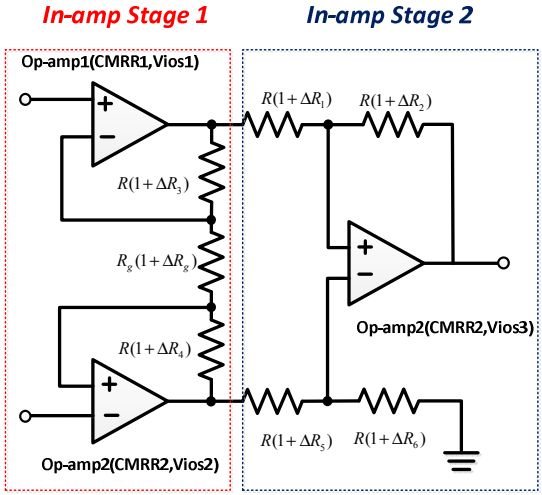



Figure 2. A 3 op-amp instrumentation amplifier architecture

First, we remind here that, by assuming that the used op-amp has ideal properties (mainly infinite gain), the differential gain $A_{d,INA}$ of the 3-op-amp in-amp depends only on the resistances values as show in equation (1).

$$A_{D,INA} = 1 + 2\frac{R}{R_g} \quad (1)$$

The in-amp common mode rejection ratio $CMRR_{INA}$ is not ideally infinite (and then the common mode gain $A_{CM,INA}$ does not equal zero). Three factors limit its value: the finite common mode rejection ratios of the three op-amps ($CMRR_1$, $CMRR_2$ and $CMRR_3$), the resistors mismatch and finally a mismatch in the sensor output and amplifier input impedances. We denote here $A_{CM,\Delta R}$, $A_{CM,\Delta Z}$ and $A_{CM,OP}$ the common mode gains caused respectively by each of these factors. Similarly, symbols $CMRR_{\Delta R}$, $CMRR_{\Delta Z}$ and $CMRR_{OP}$ represent the common mode rejection ratio that is caused respectively by the mentioned factors. The total common mode gain and the common mode rejection ratio of the in-amp are calculated in (2), (3) and (4).

$$A_{CM,INA} = A_{CM,\Delta R} + A_{CM,\Delta Z} + A_{CM,OP} \quad (2)$$

$$\frac{1}{CMRR_{INA}} = \frac{1}{CMRR_{\Delta R}} + \frac{1}{CMRR_{\Delta Z}} + \frac{1}{CMRR_{OP}} \quad (3)$$

$$\frac{1}{CMRR_{INA}} = \frac{A_{CM,INA}}{A_{D,INA}} \quad (4)$$

Recording to references [7] and [8], expression of $CMRR_{\Delta R}$ is calculated for the worst case (equation 5). Similarly, $CMRR_{\Delta Z}$ is calculated in the worst case (equation 6). Terms $Z_c$, $Z_s$, $\Delta_c$, $\Delta_S$ represent respectively common impedance, sensor impedance, common mode impedance error and sensor impedance error.

$$CMRR_{CM,\Delta R} = \frac{A_{D,INA}}{2\Delta R} \quad (5) \qquad CMRR_{CM,\Delta Z} = \frac{Z_C(1-\Delta_C^2)}{2Z_S(\Delta_C + \Delta_S)} \quad (6)$$

We suppose in this work that op-amp are similar ($CMRR_1$=$CMRR_2$=$CMRR_3$) and that there is a good impedance matching in the input of the in-amp. Moreover, we assume ideally that there is not a resistor mismatch (this means $\Delta R_1$=$\Delta R_2$=$\Delta R_3$=$\Delta R_4$=$\Delta R_5$=$\Delta R_6$=$\Delta R_g$=0). In fact, the last assumption is not easy to be guaranteed in HT. Actually, resistors, even if they are similar in ambient temperature, could have different values in HT.

In the ideal conditions, the op-amp 1 and op-amp 2 outputs are ideally symmetric. Consequently, the common mode rejection ratio of the stage 1 $CMRR_{stg1}$ has no effect on the total CMRR ($CMRR_{INA}$). $CMRR_{INA}$ depends rather on the common mode rejection ratio of the second stage $CMRR_{stg2}$ whose expression is given by equation (7) giving the final expression of $CMRR_{INA}$.

$$CMRR_{OP} = CMRR_{Stg2} = A_{D,INA}CMRR_3 \quad (7)$$

Besides, calculating the output in-amp $V_{OOS,INA}$ takes into account two contributions (equation 8): the contribution of 3 op-amps input voltages offset (denoted $V_{OOS,INA1}$) and the contribution of op-amp input offset and bias currents (denoted $V_{OOS,INA2}$). The details of each contribution are described in equations (8), (9), (10) and (11). $V_{OOS,INA}$ and $V_{IOS,INA}$ are respectively the in-amp output and the input voltages offset.

$$V_{OOS,INA} = V_{OOS,INA1} + V_{OOS,INA2} \quad (8)$$

$$V_{OOS,INA1} = A_{d,INA}\left(V_{IOS,1} + V_{IOS,2}\right) + 2V_{IOS,3} \quad (9)$$

$$V_{OOS,INA2} = \left(RI_{B2-} - R_{S2}I_{B2+} - RI_{B1-} + R_{S1}I_{B1+}\right) + I_{OS}R \quad (10)$$

$$V_{IOS,INA} = \frac{V_{OOS,INA}}{A_{D,INA}} \quad (11)$$

The input voltages offset of op-amp1, op-amp2 and op-amp3 are respectively $V_{IOS,1,}$ $V_{IOS,2}$ and $V_{IOS,3}$ . We define also the parasitic currents of op-amp1 and op-amp2 ($I_{B1+}$, $I_{B1-}$ positive and negative op-amp 1 bias currents, $I_{B2+}$and $I_{B2-}$: positive and negative op-amp2 bias currents, $I_{os}$: the op-amp 3 input offset current). The sensor resistances are $R_{s1}$ (connected to op-amp1) and $R_{s2}$ (connected to op-amp2). The parasitic currents contribution is given by equation 10. When the three op-amps are supposed to be similar, parasitic currents are similar ($I_{B1+}$=$I_{B2+}$= $I_{B+}$; $I_{B1-}$=$I_{B2-}$=$I_{B-;}$ $V_{IOS,1}$=$V_{IOS,2}$= $V_{IOS,3}$=$V_{os}$). Voltages $V_{OOS,INA1}$ and $V_{OOS,INA2}$ are given by equations (12) and (13).

$$V_{OOS,INA1} = 2V_{OS}\left(A_{D,INA} + 1\right) \quad (12)$$

$$V_{OOS,INA2} = I_{B+}\left(R_{S1} - R_{S2}\right) + I_{OS}R \quad (13)$$

After reviewing the 3-op-amp in-amp structure and dependency of its performances to those of op-amps, we remind in the Section III the validity of the SPICE and VHDL-

AMS op-amp model. These two models will be used in Section IV in the in-amp simulation in HT.

## III.SPICE AND VHDL-AMS OP-AMP MODELS IN HT

The used op-amp belongs to the conventional electronics family as it specification indicates that it operates between -40°C and 80°C. The SPICE model is provided by the device manufacturer. In this macro-model which is presented in a netlist format, only two transistors are present. The effect of the temperature is not well developed: only described by two transistors parameters (XTB and XTI).

The simulation results of the VOS and the CMRR by the SPICE model were already detailed in [3]. They are compared to the measurement results in order to evaluate the accuracy of the SPICE model, especially in HT. Measurement and simulations conditions were also detailed in [4]. SPICE simulation predicts a linear evolution of the voltage offset as function of temperature in HT. However, measurement results indicate an almost-exponential evolution in the range [130°C, 220°C]. Moreover, the op-amp SPICE simulation of CMRR shows a constant value in [20°C, 220°C]. However, the measured CMRR in dB decreases from 116.856 at 20°C to 80.8 at 220°C. By referring to measurements results, some values of CMRR simulation errors (in percentage and numerical values) are detailed in Tab. 1.

TABLE I. COMPARISON OF MEASURED AND SIMULATED OP-AMP CMRR VALUES

| *CMRR* | | | | | |
|---|---|---|---|---|---|
| *Temp.* | *SPICE* | | *VHDL-AMS* | | *Meas.(dB)* |
| | *Value (dB)* | *Error (dB and %)* | *Value (dB)* | *Error (dB and % )* | |
| 20 | 101,95 | 14,91dB (12.75%) | 116.613 | 0.5 0.21% | 116.86 |
| 80 | 101.94 | 10.02 dB (8.94%) | 112.222 | 0.262 0.234% | 111.96 |
| 120 | 101.94 | 2.91 dB (2.77%) | 104.693 | 0.157 0.149% | 104.85 |
| 180 | 101.94 | 22,37dB (28.24%) | 79.4502 | 0.2402 0.302% | 79.21 |
| 220 | 101.94 | 21.14 (26.16%) | 81.118 | 0.318 dB (0.393%) | 80.8 |

Thus, it is clear that the industrial SPICE op-amp model is not accurate enough. Instead, a VHDL-AMS model was developed. The modeling methodology was detailed in [4] and [5]. This model is developed in two steps. First, a non-dependent temperature model was developed and validated. This model is a mixing of a structural description and behavioral one. For example, an electrical description models the voltage offset as a voltage source. The voltage offset caused by the common mode and the frequency properties of the CMRR are behaviorally modeled. The second step consists in describing parameters evolution in temperature with exponential and polynomial functions. Finally, the modeling of each parameter is validated by an appropriate test-bench circuit in the different temperature points [5].

## IV. VHDL-AMS IN- AMP MODELING AND SIMULATION IN HT

Once validated, the VHDL-AMS op-amp model was stored in a specific library to reuse it in the design of further based op-amp circuits. We used it here in order to simulate and validate the performances of a 3-op-amp in-amp in HT. It enables to review the effects of the op-amp performances in those of the in-amp. Furthermore, by achieving a SPICE simulation, the improvement of the accuracy of the VHDL-AMS model is also evaluated.

### *A. Voltage offset, saturation voltage and differential gain*

Fig. 4 shows the simulated in-amp circuit in Cadence environment. Resistors models are taken from Cadence library "*analoglib*". The op-amp model is a VHDL-AMS one. A DC analysis of the total circuit enables us to know the values of three parameters: the voltage offset the saturation voltages and the differential gain. Their values are deduced by reading the characteristic curve of the in-amp. Simulations were achieved in two temperatures: 20°C and 220°C. We have done the same analysis with PSpice tool by using a SPICE model. Simulations results are detailed in Tab. II.

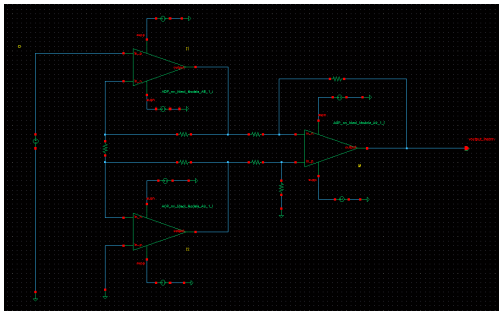


Figure 3. DC Analysis of a 3-op-amp instrumentation amplifier

TABLE II. COMPARISON OF SPICE AND VHDL-AMS IN-AMP SIMULATIONS RESULTS TO THEORY

| | ***Parameters*** | | | | | |
|---|---|---|---|---|---|---|
| | *VHDL-AMS(µV)* | | *SPICE(µV)* | | *Theoretical (µV)* | |
| | *20°C* | *220°C* | *20°C* | *220°C* | *20°C* | *220°C* |
| ***Differential gain*** | 1998,3 | 1993,5 | 1997.2 | 1994.1 | 2001 | 2001 |
| ***Voltage Offset*** | 127.77 | 2358.56 | 189.19 | 587,15 | 128.69 | 2359.65 |
| ***High saturation voltage*** | 14,21 | 14.01 | 14,38 | 14.15 | - | - |
| ***Low saturation voltage*** | -14.95 | -14.61 | -15,02 | -14.9 | - | - |

Tab. II compares SPICE and VHDL-AMS simulations results to theoretical values found by the developed equations in Section II (expecting for saturation voltages). We notice here that the used values of $I_{os}$ to calculate the theoretical value of VOS (equation 13) are respectively 1.9447nA at 20°C and 783.9859 nA at 220°C. These values were found by experimental way when characterizing the op-amp. The resistances are supposed to keep the same value in 20°C and 220°C ($R_g$=1KΩ and $R$=1MΩ). It is clear that the VHDL-AMS simulation leads to closer results to theoretical values than the SPICE simulation, especially for the VOS. We can also define and calculate the simulation error (in percentage) for each model as the difference between simulation results and theoretical values. For example, the mean voltage offset error does not exceed 2% for the VHDL-AMS. However, SPICE simulation of the same parameter error reaches higher values in HT (between 60% and 105%).

### B. Common Mode Rejection Ratio

In this part, we have checked the values of the considered in-amp CMRR. In Cadence environment, a symbol was generated from the schematic description of the 3-op-amp in-amp and used in the VHDL-AMS simulation of the test-bench circuit. SPICE simulation was done also in PSpice by sweeping temperature from 20°C to 220°C. All op-amps were considered perfectly identical. Consequently, their parameters values are equal. Then, the resistors have been assumed to be ideally matched. Furthermore, we have supposed that the temperature effects on the resistors are neglected in HT domain. There is no impedance mismatch that reduces the common mode performance of the in-amp. Simulation results are depicted by Fig.4.

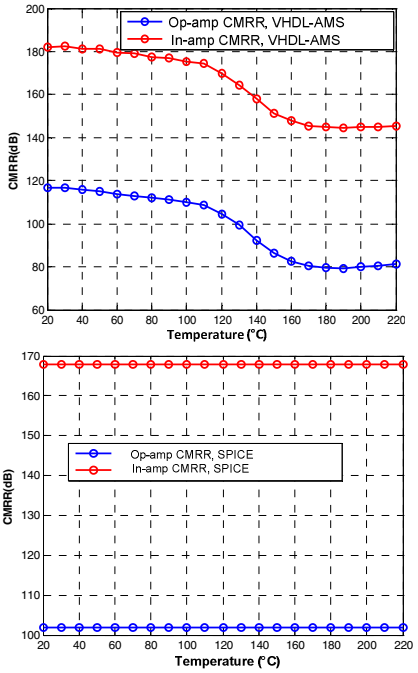



Figure 4. Comparison of op-amp and in-amp CMRR values

As the two op-amp of the stage 1 are similar, the CMRR is totally defined by the second stage op-amp. That is why we can see clearly in Fig. 4 that both the two simulations verify the equation relating the differential gain and the third op-amp CMRR (equation 7). Actually, Fig.4 indicates that independently of the used model, the in-amp CMRR curve is almost 60dB below the op-amp CMRR curve. This means that the differential gain (which is the difference in dB between op-amp CMRR and in-amp CMRR) predicted by the simulation of the two models keeps a high value which is almost equal to 60 dB. These values were already found by the first DC analysis (Tab. II). This is mainly due to the high value of the op-amp open-loop gain $A_{OL,OP}$ which was found by SPICE and VHDL-AMS simulation even in HT [5], [7].The two in-amp simulations show the importance to predict accurately the value of op-amp CMRR as the error (simulation-theory) will be multiplied by the differential gain of the in-amp (equations 7). Similarly, the in-amp output voltage offset depends on the op-amp input voltage offset and the op-amp current offset. In addition, $I_{os}$ is multiplied by the resistance value and $V_{os}$ is multiplied by the differential gain (equations 12 and 13). Usually $R$ and $A_{D,INA}$ values are high. If the op-amp model cannot predict the voltage offset especially in HT (it reaches some mVs) or the current offset (it reaches some µAs), the in-amp voltage offset will be high and in-amp could saturate. This can be for example the result of relying on inaccurate SPICE simulation in HT without checking and reviewing it.

## V. Conclusion

In this paper, we have simulated a 3-op-amp in-amp circuit by using two model types: an industrial SPICE macro-model and a behavioral VHDL-AMS model. In the first part of the paper, relations between in-amp and op-amp parameters are reviewed. We were interested especially in two parameters: the voltage offset and the common mode rejection ratio. In Section III, the validity of the VHDL-AMS and SPICE models were reminded. In this part, some numerical values of simulations errors were given. Moreover, some details about the structure and the development of the SPICE and VHDL-AMS models were reminded. Finally, in Section IV, in-amp simulation results of two models were described. The relations between op-amp parameters and in-amp parameters were again checked. We have proofed the importance to have an accurate op-amp model that enables to predict precisely the voltage offset values as these parameters are multiplied by the high values of the gain and the resistances. In this work, we have neglected the effect of resistors mismatch and impedance mismatch. In addition, we have supposed that the 3 op-amps were identical. It will be interesting to extend our work to model the contribution of such factors in the values of the CMRR or the voltage offset. Moreover, making measurements of the in-amp CMRR and VOS will be a good manner to confirm simulations and theoretical results.

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