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Estimation of analog/RF figures-of-merit using device design engineering in gate stack double gate MOSFET

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In this paper, the analog performance as well as some new RF figures of merit (FOMs) are reported for the first time of a gate stack double gate (GS-DG) metal oxide semiconductor field effect transistor (MOSFET) with various gates and channel engineering. The comparison is made through various performance metrics between single material (SM) GS-DG, dual material (DM) GS-DG, and dual material single halo (DM-SH) GS-DG MOSFETs. The key idea behind this investigation is to provide a physical explanation for the improved analog and RF performances exhibited by the device. The major figures of merit (FOMs) such as transconductance (g_m), output conductance (g_d), transconductance generation factor (TGF), early voltage (V_{EA}), intrinsic gain (A_V), cut off frequency (f_T) are analyzed in this paper. The V_{EA} and TGF for p-MOSFET with above technologies are also systematically investigated with the help of extensive device simulation, i.e. TCAD (Technology Computer Aided Design). The DM-DG devices are known to have significantly better performances as compared to SM counterparts. The analysis shows an opportunity for realizing high performance analog and RF circuits with the device proposed in this paper. The DM-DG configurations can be preferred over SM-DG as they show 48.53% improvement in f_T , 25.54% in A_V and more than 90% in V_{EA} .

1. Introduction

The transistor density and the rise of performances, due to the methodical downscaling, lead to higher chip functionality and higher frequencies. Due to close proximity between source and drain, the gate electrode loses the control of the potential distribution and current flow in the channel region which results in undesirable effects called short channel effects (SCEs) [1,2]. Various approaches like channel engineering using halo implantation, gate work-function engineering, gate stack (high-k gate oxide with interfacial

layer SiO_2), multi-gate devices, etc., have been proposed to alleviate the short channel effects. As per the International Technology Roadmap for Semiconductors (ITRS), the semiconductor industries migrate from geometrical scaling to equivalent scaling. Equivalent scaling targets to improve the performances through innovative designs, which typically allow for non-digital functionalities (e.g. Analog and RF communication) in circuit design [3].

The Silicon-on Insulator (SOI) technology allows digital CMOS scaling based on multi-gate architecture, and also provides a unique platform for analog and RF integration due to its impressive isolation and high frequency performance functionality [4]. The DG-MOSFETs due to their improved performances over the SG-MOSFET are becoming the subject of intense very large scale integration (VLSI) [4], [5] researches. As CMOS scaling approaches the limit, the DG-

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MOSFETs have the ability to be scaled to sub-100 nm with better performances, excellent SCEs immunity, higher drain current, volume inversion (VI), higher transconductance and steeper subthreshold slope as reported by various studies [6–8]. Scaling down improves cut off frequency due to the reduction of supply voltage. However, the analog performances degrade due to heavy SCEs. Efficient gate engineering and channel engineering for sub-100 nm devices are a major challenge reported by Ray et al. and Yu et al. [9,10]. In the past few years, the local high doping concentrations in the channel near source/drain junctions have been implemented via lateral channel engineering, e.g. halo or pocket implants. Single halo MOSFET structures have been introduced for bulk as well as for SOI MOSFETs [11–13] to adjust the threshold voltage and to improve the immunity towards SCEs. However, the continual gate oxide scaling requires high-k gate dielectrics, for suppressing the leakage current induced by the thin gate oxide layer. Similarly, the concept of gate oxide stack (i.e. a thick layer of high-k oxide is sandwiched over a thin layer of SiO₂) has been proposed by Hu and Wong [14,15]. The high-k gate stack also improves SCEs like drain induced barrier lowering (DIBL), hot carrier effects (HCEs), channel length modulation (CLM) and increases the drive current to leakage current ratio (I_{on}/I_{off}) in sub-100 nm DG-MOSFETs as reported in various studies [16, 17]. In a recent work [18], a detailed investigation on the role of high-k gate dielectric on various parameters by considering both single layer and gate stack configurations has been presented with the aim to optimize the high-k gate dielectric. Similarly, the DM gate devices, in which two different work functions are used to form the gate, show promising results in the reduction of SCEs [19,22]. The novel attributes of DM devices are the improved carrier transport efficiency, the transconductance, the reduced DIBL and the drain conductance [21].

The SCEs tend to degrade analog FOMs such as transconductance (g_m), early voltage (V_{EA}), g_m/I_d ratio which is the transconductance generation factor (TGF) and the intrinsic dc gain (g_m/g_d). Moreover, V_{EA} and TGF which are the key analog FOMs of a technology show the efficiency of the devices to convert DC power into AC frequency and the gain performance [10]. To resolve this issue, the role of asymmetric channel doping like single halo (SH) and double halo (DH) on various performance metrics has been reported [17]. In continuation to this previous work, this paper systematically represents the effect of dual metal with the addition of SH doping profile on various performance metrics.

Now a days Ultrathin Body (UTB) SOI technology is becoming a contender for low-power system-on-a-chip (SoC), including microwave applications. So, an investigation of the impact of device options on the analog and RF performance of SOI MOSFETs is needed. As the semiconductor industry migrate towards multi-gate technology with different device engineering for enhancement of performance, a systematic estimation of analog and RF performance measure is presented here for GS-DG-MOSFET.

The presented work in this paper is organized as follows: Section 2 shows the device architecture of DG-MOS transistors with different gate materials and different channel doping profiles. Section 3 describes the simulation

procedure using the TCAD device simulator ATLAS™ [23]. Section 4 proposes the investigation of the impact of dual material gate technology with lateral asymmetric channel (DM-SH) on various parameters such as the surface potential, electron mobility, electron velocity, electric field, transconductance (g_m), output conductance (g_d), transconductance generation factor (TGF), early voltage (V_{EA}), intrinsic gain (A_v), gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), cut off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and gain transconductance frequency product (GTFP) for the n-MOSFET. This section also comprises the TGF and V_{EA} variations because of DM and DM-SH for p-MOSFET. Finally the conclusions are presented in Section 5.

2. Device structures

A device is considered with high-k material as gate stack and an extensive study is made by taking dual material gate and DM-SH techniques to verify the effects on electrostatic parameters as well as various analog/RF FOMs. Two different materials are considered as gate electrode to improve the carrier mobility and the channel is differently doped near the source and drain regions to reduce the width of the depletion region in the vicinity of the junctions. Actually, this reduces the leakage current and increases the output conductance.

Fig. 1 shows the schematic of cross-sectional view of the DG-MOSFETs (n-channel) with a channel length (L) considering 40 nm Source/Drain length (L_S/L_D). The silicon thickness (t_{Si}) is about 10 nm and the source drain doping is uniform with N_D density of 10^{20} cm^{-3} . The Equivalent Oxide Thickness (EOT) is about 1.1 nm. The thicknesses of SiO₂ and equivalent HfO₂ are about 1.0 nm, 0.1 nm respectively. The work function for the gate electrode is assumed

Fig. 1. Schematic structures of DG-MOSFETs of SM-GS-DG, DM-GS-DG and DM-SH-GS-DG with different device cases named as D1, D2, and D3.

as 4.77 eV for single material structures and 4.8 eV and 4.6 eV for dual material structures. The channel engineering concept is applied in the structural model with a ratio of 1:4 as shown in Fig. 1. According to channel engineering, the comparative study and the performance evaluation have been done between three different cases of the calibrated model [24] as summarized in Table 1. The default value for the z-direction is considered as 1 μm for the simulations.

3. Simulation setup

The technology parameters and the supply voltages used for the device simulations are according to the analog ITRS roadmap [3] for sub-100 nm gate length devices. The value of threshold voltage (V_{th}) used for the n- and p-channel devices is +0.375 V and -0.375 V respectively considering V_{DS} of 0.1 V, i.e., below the threshold voltage. The work functions of the metal gates are adjusted to achieve the desired V_{th} value. The 2-D numerical device simulator [23], ATLAS, is used to simulate the DG-MOSFET with high-k/metal gate. According to the ITRS roadmap, the drain bias is fixed at $V_{DD}=1.0$ V [3]. To study the analog performances, the simulation is carried out with drain to source voltage $V_{DS}=0.5$ V ($V_{DD}/2$) [18] with a range of V_{GS} from 0 V to 1.0 V. The threshold voltage is extracted using constant current ($I_D=10^{-6}$ A/ μm) definition from the I_D - V_{GS} transfer characteristic at $V_{DS}=0.1$ V. The threshold voltage is used to find out the gate overdrive voltage (V_{GT}) as defined below

$$V_{GT} = V_{GS} - V_{th} \quad (1)$$

The gate over drive voltage is a key parameter of an amplifier circuit because it decides the region of operation. The increment of V_{GT} increases in drain current until saturation. Hence in this work, all the analog and RF analyses have been done as a function of V_{GT} [25,26]. The numerical simulation uses the drift diffusion approach [27] and the models activated in the simulation comprise of field dependent mobility, concentration dependent mobility and velocity saturation model. Model parameters used from look up table are $\mu_{no}=1076$ $\text{cm}^2/\text{V s}$, $\mu_{po}=460.9$ $\text{cm}^2/\text{V s}$, $\tau_n=\tau_p=1 \times 10^7$ s. The modification of parameters in carrier transport at high field is done due to thin SOI layer. The saturation velocity v_{nsat} , v_{psat} and the empirical parameter β_n , β_p were adjusted as 2.2×10^7 cm/s, 1.5×10^7 cm/s, 1, 0.65 respectively. This adjustment in the drift diffusion model shows a good agreement with Monte Carlo (MC) simulation for $L_g > 10$ nm in a DG-MOSFET [28,29].

The MOSFET mobility can be interpreted by scattering parameters. The Berkeley Short-Channel IGFET Model (BSIM) combines the scattering parameters into an effective mobility using Mathiessen's rule. The four scattering parameters: phonon scattering μ_{ph} , surface roughness scattering μ_{sr} , bulk charge Coulombic scattering μ_{cb} , and interface charge Coulombic scattering μ_{int} calculate effective mobility μ_{eff} [30].

$$\frac{1}{\mu_{eff}(T, E_{eff})} \propto \frac{1}{\mu_{ph}(T, E_{eff})} + \frac{1}{\mu_{sr}(T, E_{eff})} + \frac{1}{\mu_{cb}(T, E_{eff})} + \frac{1}{\mu_{int}(T, E_{eff})} \quad (2)$$

The physical models accounting for temperature and electric field dependence of mobility are invoked in the simulation. The inversion layer mobility models CVT (Lombardi) [31], along with Shockley-Read-Hall (SRH) [31], [32] and Auger recombination models are included. The inversion-layer Lombardi mobility model calculates the mobility degradation which normally occurs due to higher surface scattering near the semiconductor to insulator interface which also includes Coulomb and phonon scattering. It considers the effect of transverse fields along with doping and temperature dependence parameters of mobility. The SRH and Auger recombination models are used for minority carrier recombination. The impact ionization and band-to-band Auger recombination model are included in the simulation. The gate, source and channel parasitic distributed resistances are assumed in the MOSFET. The model statement SCHRO enables the self-consistent coupled Schrödinger-Poisson model for electrons. The solution for quantum effects in MOSFET is done self-consistently through 2-D Poisson and Schrodinger solver.

In 45 nm technology node and beyond the high-k dielectrics (mostly HfO_2) are used in gate stacks to achieve a low equivalent oxide thickness (EOT) with the aim to reduce the gate leakage current, the threshold voltage and supply voltage [3]. However, one of the key issues is the process induced defect which degrades device mobility resulting in poor performance and reliability [33]. So in this simulation, the interface trapped charge density at the semiconductor to insulator interface is set to $4 \times 10^{11} \text{ cm}^{-2}$. The typical concentration of trapped charge density ranges between 10^{10} cm^{-2} and 10^{11} cm^{-2} in thin interface layers [34]. The electron and hole surface recombination velocity is defined around 1×10^4 cm/s. Based on the TCAD simulations of DG-MOSFETs, the behavior of electrostatic parameters, the possible device scalability, the analog and high frequency performances are discussed through the extracted and calculated data presented in the following graphs and tables.

Table 1
Device structures considered.

Device case	Name	N_A (p-type) (cm^{-3})	Channel engineering (Halo doping) ratio	Gate metal work function (eV)
SM-GS-DG	D1	10^{16}	1 (40 nm)	$\phi_{m1}=4.77$
DM-GS-DG	D2	10^{16}	1 (40 nm)	$\phi_{m1}=4.8, \phi_{m2}=4.6$
DM-SH -GS-DG	D3	$10^{18}; 10^{16}$	1:4 (10 nm:30 nm)	$\phi_{m1}=4.8, \phi_{m2}=4.6$

4. Results and discussion

4.1. Electrostatics parameters

The surface potential, electron mobility, electron velocity and electric field along the channel from D1 to D3 with $V_{DS}=0.1$ V, 0.5 V and $V_{GS}=0$ V to 1 V in step of 0.025 V are shown in Fig. 2. In all figures, the position along the channel (from the Source to the Drain) is plotted in the x-axis direction where “0.06 μm ” indicates the center of the channel.

The difference in the value of work function of the two gate materials in the DM gate devices results in an additional peak which influences the transport phenomena. Fig. 2 (a) shows the surface potential of the device. This parameter can be controlled by adjusting the work function of the gate metal and the doping concentration, which consequently leads to control the threshold voltage. The additional peaks of electron mobility and electron velocity near the source side for DM devices impact the carrier transport efficiency, as shown in Fig. 2 (b) and (c) respectively. In Fig. 2 (d), the peak value of the electric field near the drain side is somewhat reduced for the DM devices as compared to SM counterpart. Again, the halo effect, in addition to DM i.e. D3 device, shows a small increase in potential due to the abrupt change of doping profile compared with D1. The increase in surface potential, at the abrupt doping profile junction, reduces the electric field resulting in smaller DIBL and HCEs, which is the major effect in the case of the short channel devices. Moreover, the lower potential at the drain side in D3 implies the reduction of drain conductance (g_d), which in turn improves the analog circuit performance of the device.

4.2. Device scalability

The I_D - V_{GS} transfer characteristics in linear and log scales are shown in Fig. 3 for D1, D2 and D3 configurations. Fig. 3 (a) and (b) shows the drain current responses at $V_{DS}=0.1$ V and 0.5 V respectively. V_{th} is maintained at a constant value for all the device cases at $V_{DS}=0.1$ V as a consequence of the leakage current is quite constant. In Fig. 3 (a), it is interesting to note that the leakage current (I_{off}) is varying in between 10^{-11} A/ μm and 10^{-13} A/ μm for all devices. However, in Fig. 3 (b), the device D2 gives higher drive current because of the additional peaks in electron mobility and electron velocity. In the device cases of high-k with interfacial oxide (SiO_2) layer, the gate leakage current is reduced. The high-k gate dielectric material increases the capacitive coupling, which decreases the leakage current. The CMOS standby power is affected by the subthreshold current. MOSFETs designed for low power consumption and high speed nanoscale digital applications work at subthreshold regime. The subthreshold current affects the dynamic circuits. A steep subthreshold slope (SS) is required for switching operation. This parameter is mathematically given below [35]

$$SS = \left[\frac{\partial \log_{10}(I_D)}{\partial V_{GS}} \right]^{-1} \quad (3)$$

The inset SS values of Fig. 3 are somewhat higher in case of DM devices i.e. 64–65 mV/decade, which are acceptable as the ideal value of SS is 60 mV/decade. D2 and D3 devices show higher SS which provides larger amounts of drive

Fig. 2. Simulated parameters for n-MOSFET along the channel position (from the Source to the Drain, from the left to the right) for the device cases at $V_{DS}=0.1$ V and 0.5 V (a) Surface potential, (b) Electron mobility, (c) Electron velocity, and (d) Electric field.

Fig. 3. Drain current (I_D) of n-MOSFET in both linear and log scale as a function of gate to source voltage (V_{GS}) for (a) $V_{DS}=0.1$ V and (b) $V_{DS}=0.5$ V.

Fig. 4. (a) Transconductance generation factor (TGF) and Transconductance (g_m) of n-MOSFET as a function of Gate Overdrive Voltage (V_{GT}) for $V_{DS}=0.5$ V (b) Drain current (I_D) and Output transconductance (g_d) as a function of V_{DS} at $V_{GS}=0.5$ V.

current in saturation regime, due to an improved carrier transport efficiency.

4.3. Analog and high frequency performance

After the study on the scalability of the devices, the other important FOMs for analog/RF integrated circuit are: transconductance (g_m), output conductance (g_d), DC intrinsic gain (A_v), early voltage (V_{EA}), transconductance-to-drain current ratio otherwise known as transconductance generation factor (TGF), cut off frequency (f_T), and some new RF figures of merit (FOMs) which is investigated in this work [36].

The different analog performance parameters for SM, DM and DM-SH n-channel devices are investigated. The variations of the transconductance and transconductance generation factor with V_{GT} for 0.5 V are shown in Fig. 4 (a) for the three devices. The g_m and TGF parameters are defined and calculated as follows:

$$g_m = \partial I_D / \partial V_{GS} \quad (4)$$

$$\text{TGF} = g_m / I_D \quad (5)$$

It is evident from Fig. 4(a) that the g_m is higher in subthreshold regime for the DM devices than the SM device. However, the device with lateral asymmetric channel (LAC) shows a lower g_m because of the higher doping

concentration reduces the surface mobility which consequently reduces the drain current. In Fig. 4(a), the variation of TGF can also be observed for all the device cases. The ideal value of TGF is limited to $\approx 40 \text{ V}^{-1}$ at minimum SS of 60 mV/decade of the device. The variation of TGF occurs at subthreshold region of operation for the three studied devices. A slight reduction (10–12%) in the value of TGF can be observed for the DM devices. This reduction is due to the higher value of I_D . However, it will not affect drastically the performances in the subthreshold regime. Because TGF can be termed as the available gain per unit value of the power dissipation and the power dissipation is lower in the subthreshold regime.

The drain current and output conductance as a function of V_{DS} for different cases at $V_{GS}=0.5$ V are presented in Fig. 4(b). The output conductance g_d is defined and calculated as follows:

$$g_d = \partial I_D / \partial V_{DS} \quad (6)$$

Fig. 4 (b) shows that the SM structure leads to higher value of g_d than the DM structures. In a DM device, as V_{DS} is increased beyond pinch-off, the additional voltage is absorbed under gate metal towards drain end ($\Phi m2$) rather than under gate metal near source end ($\Phi m1$). Hence, the channel region under $\Phi m1$ i. e., the source end of the channel is effectively screened from variations in the drain potential. As a result, V_{DS} hardly has any influence on I_D

beyond saturation thereby producing a very small value of g_d . Moreover, the width of the drain depletion region becomes less in DM devices resulting in a further reduction in output conductance in such devices as compared to the SM device.

CMOS analog circuits require transistors with low output conductance in order to achieve high gains. High g_d means low output resistances which result in an increase in I_D with V_{DS} in saturation regime. The components are associated with this increase, namely channel length modulation (CLM) and DIBL. Moreover, a low g_d induces a higher early voltage of the device as furnished in Eq. (7). Fig. 4(b) shows a good control of CLM and DIBL owing to low g_d value for the D3 device.

$$V_{EA} = I_D / g_d \quad (7)$$

Fig. 5(a) shows the variation of the Early Voltage (V_{EA}) and intrinsic gain (A_V) as a function of V_{GT} which is calculated and defined by Eqs. (7) and (9) respectively. For better analog performances, the V_{EA} and A_V should be as higher as possible. The D2 and D3 devices, i.e. DM configurations, show better values than D1 device (SM). The improvement in V_{EA} leads to improve the output resistance because of reductions of short channel effects in the DM devices. As before, a significant improvement in the device gains is evident in Fig. 5(a) for the DM devices in comparison to the SM device. Such improvement in the device gain for the DM devices is mainly due to the reduced g_d and partially due to the improved g_m in such devices, as observed in Fig. 4. The intrinsic capacitances C_{gs} and C_{gd} as a function of V_{GT} for both subthreshold and above threshold or strong inversion regions are shown in Fig. 5(b). The extraction of intrinsic capacitances C_{gs} and C_{gd} is done through AC small signal analysis after post-processing operation of DC solution. The capacitances between each pair of electrodes are calculated by single AC frequency (1 MHz) solution during a DC ramp voltage from 0 V to 1 V with a step of 0.025 V. To obtain the convergence in the inversion/deep depletion region, the DIRECT parameter is added for more robust solution.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (8)$$

Fig. 5. (a) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for n-MOSFET at $V_{DS}=0.5$ V. (b) Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}).

$$A_V = g_m / g_d = (g_m / I_D) \times V_{EA} \quad (9)$$

The C_{gs} values are considerably lower for DM devices than the SD device. This is due to the lower electron concentration at source side of the device. Because of higher electron concentration at the drain side, the DM devices (D2 and D3) show higher value of C_{gd} . It is observed that both capacitances C_{gs} and C_{gd} start increasing with V_{GT} increase until saturation. After saturation, both values become constant as expected because the additional V_{DS} cannot affect the junction. Cut-off frequency (f_T) is one of the most important parameters for evaluating the RF performances of the device. Generally, f_T is the frequency when the current gain is unity. The f_T is defined by Eq. (8).

Fig. 6(a) shows the variations of f_T as a function of V_{GT} for the three device cases. Fig. 6(a) emphasizes that the DM devices provide higher f_T in the above threshold voltage region than the SM device. The difference in f_T is mainly due to the difference in g_m , as observed in Fig. 4(a). This is partially due to the higher value of total capacitance ($C_{gs} + C_{gd}$) as observed in Fig. 5(b). The maximum value of the peak of f_T corresponds to the point between the minimum gate-drain/source capacitance and the peak of transconductance. Higher transconductance and lower parasitic gate capacitances are found for the device D2 as compared to other devices considered in this study. Moreover, Fig. 6(a) reveals that f_T is higher for D2 reflecting superior gate controllability due to dual metal gate.

A unique FOM for analog/RF performances is the gain transconductance frequency product (GTFP) as given in Eq. (11) and plotted in Fig. 6(a). The peak value of GTFP is achieved at $V_{GS}=0.525$ V for all the configurations, where the level of drain current is quite low, i.e. $I_D \approx 10^{-5}$ A/ μm . It is interesting to note that the voltage corresponds to V_{GS} just above 150 mV of the threshold voltage of the device. This allows the circuit designer to determine the best region of operation by trading off among gain, transconductance and speed. Here the device D2 shows higher GTFP as compared to other configurations because of higher f_T , g_m and lower g_d . The product of g_m / I_D and f_T i.e. TFP is calculated by Eq. (12) and represents a tradeoff between power and bandwidth. TFP is also utilized in moderate to high speed designs. Similarly, gain frequency product i.e. GFP, as given in Eq. (10), is also a very

Fig. 6. RF FOMs as a function of gate over drive voltage (V_{GT}) at $V_{DS}=0.5$ V of n-MOSFET (a) Cut off frequency (f_T) and gain transconductance frequency product (GTFP) and (b) Gain frequency product (GFP) and transconductance frequency product (TFP).

Fig. 7. (a) TGF as a function of V_{GT} for p-MOSFETs at $V_{DS} = -0.5$ V and (b) V_{EA} as a function of V_{GT} for p-MOSFETs at $V_{DS} = -0.5$ V.

Table 2

Analog performance of different n-channel devices for $V_{DS}=0.1$ V and 0.5 V.

Device	Transconductance, g_m (S)		Output conductance, g_d (S)	Early voltage, V_{EA} (V)	Gain, A_V (dB)	TGF (V^{-1})	
	$V_{DS}=0.1$ V	$V_{DS}=0.5$ V	$V_{DS}=0.5$ V	$V_{DS}=0.5$ V	$V_{DS}=0.5$ V	$V_{DS}=0.1$ V	$V_{DS}=0.5$ V
D1	1.69×10^{-3}	3.40×10^{-3}	6.96×10^{-6}	6.175	53.785	38.549	39.514
D2	1.84×10^{-3}	3.63×10^{-3}	3.11×10^{-6}	11.82	61.350	37.288	37.328
D3	1.72×10^{-3}	3.57×10^{-3}	1.50×10^{-6}	13.82	67.514	35.816	35.757

important parameter for operational amplifiers in high frequency application. The GFP and TFP parameters as a function of V_{GT} for $V_{DS}=0.5$ V are plotted in Fig. 6(b). It appears that GFP and TFP start linearly increasing with the increase of V_{GT} in subthreshold region and hold an optimum value then start decreasing in saturation region. The DM devices show better GFP and TFP values than the SM device. This is due to the high g_m and f_T values of DM devices.

$$GFP = (g_m/g_d) \times f_T \quad (10)$$

$$GTFP = (g_m/g_d) \times (g_m/I_D) \times f_T = A_V \times TFP \quad (11)$$

$$TFP = (g_m/I_D) \times f_T \quad (12)$$

In a CMOS amplifier, the n-channel devices will act as driver and the p-channel device as load. Hence the TGF and V_{EA} parameters of the p-channel devices also play a decisive role in determining the circuit performances. The plots of TGF and V_{EA} as a function of V_{GT} for the p-channel DM, DM-SH and SM devices are shown in Fig. 7. Fig. 7 presents that the parameters of p-channel DM devices follow the similar trend to its n-channel counterpart as expected. The maximum values of g_m , g_d , V_{EA} , A_V , TGF are summarized in Table 2. By comparing all the extracted parameters in Table 2, the DM device with LAC doping i.e. device D3, shows a better result in terms of gain, and V_{EA} .

As stated the TGF is slightly lower in case of DM device, but that will not hamper the device performance much.

Table 3RF performance of different n-channel devices for $V_{DS}=0.5$ V.

Device	C_{gs} (fF)	C_{gd} (fF)	f_T (GHz)	GFP (GHz)	TFP (GHz/V)	GTFP (GHz/V)
D1	1.651	0.251	286.75	1.535×10^4	3.584×10^3	1.535×10^5
D2	1.064	0.307	425.91	2.603×10^4	5.162×10^3	2.662×10^5
D3	1.031	0.324	421.33	2.843×10^4	4.071×10^3	2.247×10^5

Similarly, the peak values of RF FOMs like f_T , GFP, TFP and GTFP are compared for various DG configurations at $V_{DS}=0.5$ V in Table 3. From the data given in the table, the f_T , TFP and GTFP values are better in case of DM-GS-DG case, i.e. D2 device. Because of the high doping profile near the source in case of DM-SH-GS-DG, i.e. D3, device shows somewhat lower values of previously enumerated parameters than D2 device. However, the GFP is maximal for the D3 device because of a higher gain, as illustrated in Fig. 6 (a) and Table 1.

5. Conclusions

The different device performance parameters in below and above threshold voltage regimes of operation have been systematically investigated for the DM-GS-DG and DM-SH-GS-DG n-MOS and p-MOS devices for Analog/RF applications. The n-MOS and p-MOS electrical characteristics with analog/RF FOMs have been successfully studied using the TCAD device simulation software ATLASTM with the aim to provide useful guidelines to device designers.

The study investigates the main analog/RF figures of merit such as V_{EA} , A_v , f_T , TFP, GFP and GTFP for three different device configurations. Improvements in these electrical parameters have been obtained and emphasized for the n-channel devices. The DM-GS-DG device, i.e. D2, shows an interesting improvement in early voltage by 91.41%, gain of the device by 14.06%, cutoff frequency f_T by 48.53%, GTFP by 73.42%, GFP by 69.57% and TFP by 44.02% over its counterpart SM-GS-DG i.e. D1 device. Moreover, the DM configuration with addition of LAC doping i.e. D3 device shows optimum values in case of A_v and GFP. Finally, the DM p-MOS transistors have been found to outperform with their SM counterparts in terms of V_{EA} . Only a decrement of 5.8% in TGF for DM devices as compared to SM device will not hamper that much to the device performance. Therefore, the DM devices can be very attractive for ultralow power high frequency analog/RF applications.

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