

Digital distortion compensation for wideband direct digitization RF receiver

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Abstract—This paper deals with the study of a new correction structure for the distortion compensation in direct digitization receivers. In that purpose, a modified post-distortion algorithm including an efficient adaptive filter is used. Performance have been demonstrated on measurements from a state of the art wideband TI-ADC and from an entire direct-digitization RF receiver. On the TI-ADC, with a two-tone input signal, the algorithm has improved the SFDR by $\sim 25dB$. Besides, Besides, on the entire receiver, the algorithm has been able to achieve $\sim 16dB$ of improvement on the SFDR.

Index Terms—Linearization techniques, nonlinear distortion, receiver nonlinearity, digital post-distortion.

I. INTRODUCTION

The development of the 5G mobile communication standard is ongoing and challenges are manifold. One key component of this network is the flexibility and behind this, there is the software defined radio concept with direct RF sampling receivers. This concept has become more and more true with the last CMOS technologies and very high speed ADCs with several Gb/s. Indeed the constant shrinkage of CMOS nodes allows to integrate more and more complex algorithms in ASICs. However, digitizing a wide signal band in the receiver implies the ability of dealing with potential interferers. In this context of multiple standards, the linearity and the SFDR constraints are key criteria for receiver performances. Indeed, in a nonlinear receiver, strong interferers produce intermodulation terms or harmonic distortion terms that can fall into the desired channel. Taking advantages of small CMOS nodes, digital corrections have become more and more advantageous. At the transmitter, a well-known technique to correct the PA distortions is the digital predistortion [1]. However, at the receiver side, the correction is more challenging. Indeed, the receiver input is unknown which supposes a non-aided (blind) correction in order to compensate for distortion. According to the system complexity, these corrections can be limited to infrastructures.

A significant component for the correction is the choice of a nonlinear model among those available in the literature [2]. In a first approximation, nonlinear systems can simply be modeled by a polynomial function. However, in wideband applications such a representation is not realistic, indeed, memory effects can arise. These memory effects shape the distortion in module and phase for each nonlinear order.

Several models, with different levels of complexity, exist to take into account these effects. Volterra series [3] is a well-known model for the analysis of weakly nonlinear systems, and is here in equation (1). In this equation, $h_d(l_1, \dots, l_d)$ is called p-order kernel, D is the maximum polynomial order and L is the memory depth.

$$y(n) = \sum_{d=1}^D \sum_{l_1=0}^{L-1} \cdots \sum_{l_d=0}^{L-1} h_d(l_1, \dots, l_d) x(n-l_1) \dots x(n-l_d) \quad (1)$$

In the literature many paper focus on the baseband correction in receivers [4] [5], nevertheless, they are limited to distortions created by nearby interferers. However, in direct digitization RF receivers, a channel can be corrupted from far interferers. Therefore, in this paper, we propose an architecture that can solve this issue by adding a broadband correction. In a first step this architecture is described, then the broadband correction block is explained. In a third step, the broadband correction is performed on measurements coming from two different systems, a wideband TI-ADC (Time-Interleaved ADC) and a wideband direct digitization RF receiver.

II. PROPOSED CORRECTION FOR DIRECT DIGITIZATION RF RECEIVER

In a direct digitization receiver, there is no mixer and the ADC is located just after the low noise amplification stage, hence the whole band is digitized. Then, each channel can be selected individually by a DDC (Digital Down Converter). This type of architecture improves the cost and the consumption compared to several heterodyne or homodyne receivers. In order to correct for each channel the distortions due to interferers, several baseband post-distortion techniques exist [4] [5]. However, these corrections are limited to scenarios where the interferers are nearby the desired channel. In a direct digitization receiver, distortions from far interferers can also fall into the desired channel. To tackle this issue we propose in this paper a new architecture described in Fig.1. In this architecture the distorted signal is downconverted by the DDC and a baseband correction is performed on each channel. After demodulation, the most corrupted channel is determined, then an additional processing is done on it by the broadband correction. Selecting the strongest interferers, the broadband correction estimates and compensates the distortions caused

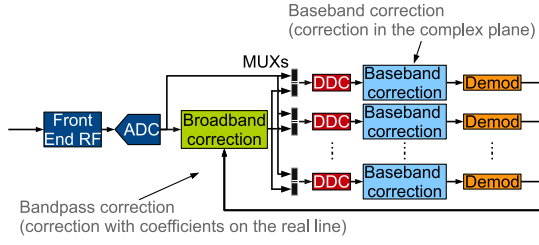


Fig. 1. Proposed architecture for wideband direct digitization receiver

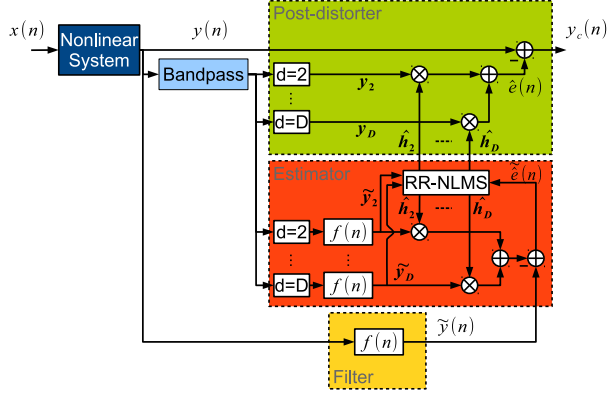


Fig. 2. Digital post-distortion schematic

by these interferers in the specified channel. In order to select the channel which uses the broadband correction, multiplexers are employed.

III. DIGITAL POST-DISTORTION

A. Description of the algorithm

In this section the post-distortion algorithm used for the broadband correction is described. The present algorithm is based on [6] to which we added three improvements. First, a bandpass filter has been added to enhance the convergence. Then, another adaptive filter has been chosen in order to be more robust against noise thanks to the regularization term. At last, the number of coefficients to estimate has been reduced by using the symmetry property of Volterra series [3]. Fig.2 shows the correction schematic and three main blocks can be distinguished : the post-distorter, the estimator and a linear filter. The linear filter $f(n)$ is used to isolate a free frequency band where only the distortion falls. In the estimator block, using a Volterra model, the distortion is reconstructed in this specific band by the RR-NLMS algorithm [7] in such a way that the error between the estimated and the real distortion tends to zero. The performance of the RR-NLMS algorithm are improved compared to the NLMS algorithm used in [6] thanks to the regularization parameter. A bandpass filter is also used to select the strongest interferers in order to reconstruct and to compensate distortions at best. The estimator block outputs (\hat{h}_2 to \hat{h}_D) are the coefficients of the estimated Volterra series. These estimated coefficients are fed into the post-distorter block in order to reconstruct the distortion which

is then subtracted to the nonlinear system output providing the corrected output.

B. Issue for strong distortions cases

In a strongly nonlinear system, distortion terms can be high enough to be used by the adaptive filter to recreate the distortion. Indeed, by example, suppose a one tone input $x(t) = A_1 \sin(2\pi f_1 t + \varphi)$ and a third order nonlinear system. At the system output, the components HD2 and HD3 at frequencies $2f_1$ and $3f_1$ will arise. Suppose that only the HD3 component is selected by the filter $f(n)$ and the SFDR is considered quite low, by example 35dB. The adaptive filter using a third order correction should converge with second order estimated coefficients around 0. However because of a low SFDR, the adaptive filter can use second order distortions to recreate a third order term by generating an IM2 term between the main signal and the HD2 term. Therefore to avoid this issue that can cause a misestimation, a bandpass filter should be used to select the main signal. The filter attenuation does not need to be strong, but high enough to keep a reasonable SFDR value. To recreate distortions at best, the filter should be also as flat as possible in the band.

C. Noise issue for real system estimation

The signal of interest for the adaptive filter is the distortion signal in the free frequency band. Considering distortion as a weak signal, the SNR can be low and estimation can become noisy. Indeed if we observe the NLMS algorithm [8] used in [6] :

$$\hat{\mathbf{h}}_d(n+1) = \hat{\mathbf{h}}_d(n) + \mu \frac{\tilde{\mathbf{y}}_d(n) \tilde{e}(n)}{\sum_{d=2}^D \|\tilde{\mathbf{y}}_d(n)\|^2}, \quad \text{with} \quad (2)$$

$$\tilde{e}(n) = \tilde{y}(n) - \sum_{d=2}^D \hat{\mathbf{h}}_d(n)^T \tilde{\mathbf{y}}_d(n)$$

where $\hat{\mathbf{h}}_d(n)$ is the d-order kernel to estimate, $\tilde{\mathbf{y}}_d(n)$ is the d-order input signal in the free frequency band, $\tilde{e}(n)$ is the error signal in the free frequency band, μ is the step size of the algorithm and $\sum_{d=2}^D \|\tilde{\mathbf{y}}_d(n)\|^2$ is the normalization term of the NLMS algorithm. If the input $\tilde{y}(n)$ is supposed to be weak, it will be the same for the normalization term, therefore, it will amplify the noise effect on the estimation. Consequently, the algorithm convergence speed can be slowed down, or the algorithm may never converge. However, in a real implementation, a constant is added to the normalization term to prevent a division by zero if the normalization term is equal to zero. This constant is called regularization term and is denoted ϵ . Moreover this regularization term, correctly chosen, can also mitigates the noise effect on the estimation. Algorithms like GNGD [9] and RR-NLMS [7] use this regularization term and make it adaptive in order to optimize its value at each iteration. In the correction Fig.2 the RR-NLMS algorithm is described by:

$$\hat{\mathbf{h}}_d(n+1) = \hat{\mathbf{h}}_d(n) + \mu \frac{\tilde{\mathbf{y}}_d(n) \tilde{e}(n)}{\sum_{d=2}^D \|\tilde{\mathbf{y}}_d(n)\|^2 + \epsilon_d(n)}, \quad (3)$$

where μ is the algorithm step size and $\epsilon_d(n)$ is updated as follow:

$$\epsilon_d(n) = \epsilon'_d(n-1) - \rho \text{sgn}[\tilde{e}(n)\tilde{e}(n)(n-1)\tilde{y}_d(n)\tilde{y}_d(n-1)] \quad (4)$$

$$\epsilon_d(n) = \begin{cases} \epsilon'_d(n), & \text{if } \epsilon'_d(n) \geq \epsilon_{min} \\ \epsilon_{min}, & \text{if } \epsilon'_d(n) < \epsilon_{min} \end{cases} \quad (5)$$

where ρ and ϵ_{min} are two constants chosen accordingly to the system. In the following they are both fixed to 1.10^{-6} .

D. Volterra symmetry and number of filters

1) *Use of the symmetry property of Volterra series:* Volterra series constitute a very general model for weakly nonlinear systems; nevertheless they have the drawback to need a tremendous number of coefficients if the memory depth and the polynomial order are too high. To mitigate this issue, the symmetry property of the Volterra series can be used to decrease the number of coefficients to estimate. If no symmetry is taken into account, the number of coefficients needed is:

$$N = \sum_{d=2}^D (N_d)^d, \quad (6)$$

Where D is the maximum polynomial order and N_d is the memory depth for the order d . However if the symmetry property is used we obtain [10]:

$$N = \sum_{d=2}^D \frac{(N_d + d - 1)!}{(N_d - 1)!d!} \quad (7)$$

A numerical example for $D = 5$ and $N_d = 2$ gives 60 coefficients when the symmetry is not used and 18 when it is.

2) *Filters number for real implementation:* In the estimator block, the number of linear filters $f(n)$ is equal to the number of coefficients to estimate. To illustrate that, an example is given for the filter output $\tilde{y}_2(n)$ with a memory depth of 2 in equation (8):

$$\tilde{y}_2(n) = \begin{bmatrix} f(n) * (y(n)^2) \\ f(n) * (y(n)y(n-1)) \\ f(n) * (y(n-1)y(n)) \\ f(n) * (y(n-1)^2) \end{bmatrix}, \quad (8)$$

where $*$ is the convolution product. This can be an issue in term of complexity, area and power consumption. It is also why the polynomial order and the memory depth should be kept to the bare minimum. Following the former example for $D = 5$ and $N_d = 2$, 18 filters will be needed. To decrease the number of filters, one filter can be shared between all the input signals, in keeping the same number of multipliers and with one delay line for each signal. However, this solution is limited to applications where the settling time is not critical.

IV. MEASUREMENT RESULTS

A. Wideband TI-ADC measurements and correction

In this section, the aforementioned post-distortion algorithm will be performed on measurement results of a state of the art TI-ADC [11]. The TI-ADC used is a wideband state of the art ADC designed by NXP Semiconductor. It has 4 quarters, of 16 SAR each, a 11 bits resolution and can run with a 2.7GHz clock. Due to practical reasons the ADC output is downsampled by a factor 5 and the number of points for one measurement is fixed to 2^{18} (262144).

Fig.3 shows the correction performances of the algorithm used with a third polynomial order and a memory depth of two, in the case of a two tones signal input, with the frequencies $f_1 = 500\text{MHz}$ and $f_2 = 501\text{MHz}$. Results shows that distortions have been completely canceled by the algorithm. The filter $f(n)$ plotted in red in Fig.3 allows to retrieve the signal band where the second and the third harmonic distortion terms are present in order to do the system estimation. We can notice a remaining spur in the corrected band, however, this is only due to ADC mismatches. Fig.4 shows on its left hand side, the convergence of the second and the third order kernel coefficients. On its right hand side, the convergence of the GTF (Generalized Transfer Function) [3] for the 3rd order kernel at the specific value $H_3(\omega_1, \omega_1, \omega_1)$ is pictured with $\omega_1 = 2\pi f_1$. This shows that the module and the phase of the GTF for the 3rd order have well converged.

B. Wideband receiver measurements and correction

In this section, an entire state-of-the-art $50\text{MHz} - 1\text{GHz}$ direct-digitization cable modem receiver [12] is used. The RF front-end described in Fig.5, is used as nonlinear system and consists of two cascaded single-ended LNAs with AGC, an anti-aliasing filter and a single-to-differential buffer. Furthermore, the RF front-end output is connected to the TI-ADC input. The ADC output after downsampling by 5 is stored and then processed off-line by our broadband correction algorithm. In our setup, the distortion of the RF front-end is intentionally degraded by increasing internal voltage swings and decreasing biasing currents, in order to set the distortion terms to $\sim 15 - 20\text{dB}$ above the noise floor. In this section a DVB-T channel centered on $f_c = 250\text{MHz}$ is used which allows to observe harmonic distortions terms up to the order four without being affected by the anti-aliasing filter of the

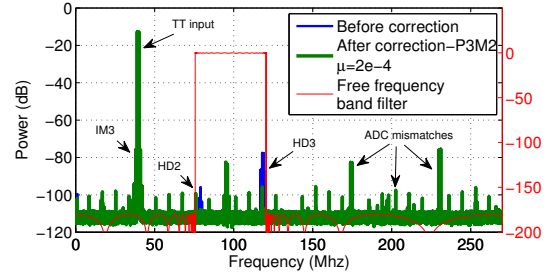


Fig. 3. PSD of the output ADC and of the output post-distortion algorithm

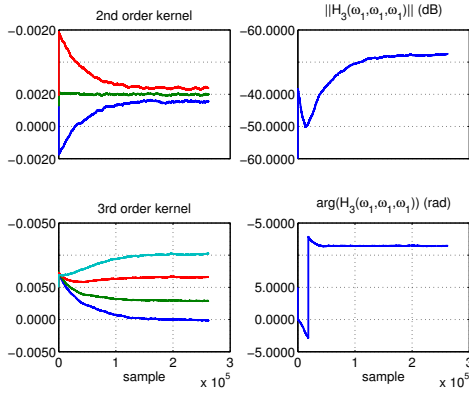


Fig. 4. Kernels convergence

receiver. Fig.6 shows the output receiver and the corrected output PSD for two different correction parameter. The first correction used, is a fifth order Volterra model with a memory depth of two and the second uses a ninth order Volterra model with the same memory depth. The frequency response of $f(n)$ which is used to isolate the free frequency band is plotted in light blue. Before the correction, we can observe that the HD3 component at the receiver output is higher than the IM3 component, which already highlights the memory effect of the system. The spectrum shows in Fig.6, a very nonlinear behavior with a SFDR $\sim 40dB$, therefore, in order to make a correct estimation, the input used to estimate the distortion is filtered by a bandpass filter, depicted in light blue in Fig.2, to keep only the interferer (DVB-T channel). The correction improves the SFDR by $\sim 12dB$ for the fifth order and by $\sim 16dB$ for the ninth order. After correction, the HD5 component and the IM3 have been increased due to the system memory. This illustrates the reason to use a multiplexer in the structure Fig.1. In Fig.7, convergence of the odd order kernels are shown, with the fifth order correction and we can notice that the estimation variance is higher than in section A. This is caused by two factors: a more complex nonlinear system and the usage of a more complex test signal.

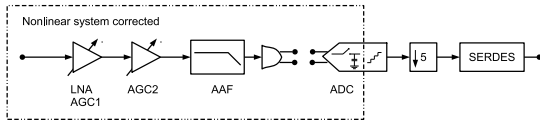


Fig. 5. Direct digitization receiver schematic

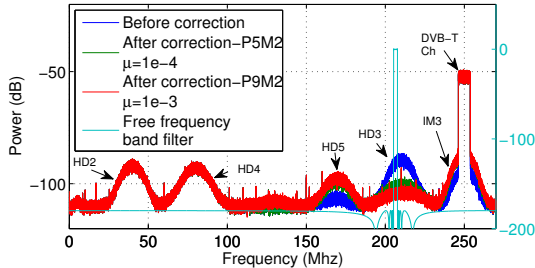


Fig. 6. PSD of the corrected output with 5th and 9th order correction

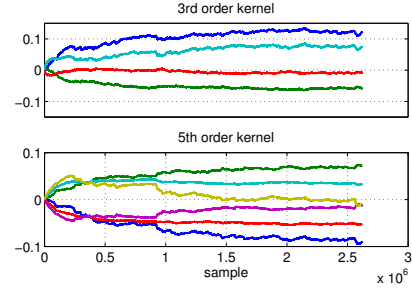


Fig. 7. Convergence of the odd order kernels

V. CONCLUSION

In this paper we have proposed a new correction architecture for nonlinear distortions in direct digitization receivers by adding a broadband correction. This broadband correction uses an efficient adaptive filter and a bandpass filter to improve parameters estimation in both high input noise and large interferer conditions. We have demonstrated the performance of this broadband correction on measurements data: A correction on a two tones signal with a wideband TI-ADC has been performed showing $\sim 25dB$ of SFDR gain, and a correction on a DVB-T channel with a wideband direct digitization receiver has been demonstrated, improving the SFDR by $\sim 16dB$. An FPGA implementation is also expected for this year in order to demonstrate the algorithm in real time.

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