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1 – 20 GHz k Ω -range BiCMOS 55 nm Reflectometer

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Abstract—Scanning microwave microscope (SMM) combines the high spatial resolution with the high-sensitivity electric measurement capabilities of a vector network analyzer (VNA). SMM is able to scan sample surface, and map real and imaginary part of sample reflection coefficient. Thus, this instrument has been pointed out as very well suited for nanotechnology devices characterization. In recent publications, SMM has demonstrated high performance while measuring k Ω -range impedances at low microwave frequency range (1–20 GHz). In spite of exceptional results of interferometry-based systems, such systems are so far hardly feasible as an integrated circuit due to physical constraints. In this work, an innovative design of integrated reflectometer based on BiCMOS 55 nm technology is proposed. Electrical simulation results have proved a linear tuner calibration from 0.9 to 1.4 fF with an 8-bits precision (i.e. 2.0 aF). Reflectometer performance has been considered under influence of temperature variation from -55 to 125 °C and process variability. Such results demonstrate a slight influence of temperature variation and process variability in the reflectometer calibration which is negligible for SMM applications.

I. INTRODUCTION

Scanning microwave microscope (SMM) is an instrument able to measure nanoscale devices, observing and/or controlling nanoscale physical phenomena interaction. The SMM is based on with a conductive atomic force microscope (AFM) probe which scans a sample surface and maps real and imaginary part of the sample reflection coefficient using a vector network analyzer (VNA) [1]. Due to such capability, the SMM has been pointed out as a backbone of nanotechnology research benefitting electronics [2], material science [3], biology [4], and medicine [5].

Scanning the dopant concentration in semiconductors [3] or researching bio-membranes in liquid environment [5], a SMM should have the ability to measure aF capacitances at low microwave frequency (1–20 GHz). For all these applications the impedance to be measured is in the k Ω -range. Unfortunately, VNA has its best sensitivity at impedances close to its normalized impedance (i.e. 50 Ω) and it is not accurate for more than ten times smaller or bigger impedances [6]. Under such conditions, SMM requires an instrumentation circuitry able to transpose the VNA sensitivity to the device-under-test (DUT) impedance vicinity.

Recent publications have presented interferometry-based systems as a potential solution to measure aF capacitances at low microwave frequency using a 50 Ω normalized VNA. Moertelmaier et al. [3] and Dargent et al. [7] have addressed accurate SMM solutions to measure of fF capacitors with an aF precision from 1 to 20 GHz. However, such systems are hardly integrable since physical constraints claim millimeter-sized devices.

In this scenario, an innovative reflectometer is implemented in BiCMOS 55 nm technology. In this work, the proposed reflectometer is optimized allowing to achieve the noticeable performance of interferometry-based systems. Electrical simulations have proved that such a reflectometer is able to measure 1 fF capacitances with aF precision using a 50 Ω normalized VNA from 1 to 20 GHz frequency range. Temperature stability of reflectometer performance have been demonstrated from -55 to 125 °C temperature range. Monte Carlo simulations have been carried on showing accurate reflectometer instrumentation under process variability.

This paper is organized as follows. Section II describes the SMM applications in the state-of-the-art. Section III presents a top-down system analysis of the proposed reflectometer. Section IV highlights design considerations to ensure reflectometer feasibility in BiCMOS 55 nm, calibration reliability, and measurement accuracy. Section V demonstrates reflectometer calibration and measurement step confirming accurate and reliable operation even under temperature variation and process variability. Finally, the conclusions are presented in Section VI.

II. STATE-OF-THE-ART OF SMM INSTRUMENTATION

SMM has presented remarkable results measuring nanoscale devices, observing and/or controlling nanoscale physical phenomena interaction. Applied to graphene-based electronics [2] and biological material [4], SMM has achieved high frequency, low impedance measurements.

T. Monti et al. have demonstrated non-contact measurements of sheet resistance of graphene-ITO electrodes for LED applications [2]. Monti's architecture is based on a direct measurements of S_{11} parameter of graphene-ITO using a coax cable and a near-field microwave probe. Accurate results were presented for 1–20 GHz instrumentation of sheet resistances of 60 Ω/sq .

K. Kim et al. have shown the first demonstration of an active broadband reflectometer for complex permittivity measurements of biological material [4]. Kim's architecture is based on directional coupler for incident/reflected power detection and a matching network of reconfigurable transmission lines and capacitors. Accurate measurements of 0.9 % saline sample were obtained from 0.5 to 26.5 GHz attaining 10 –100 Ω for real and imaginary part.

In order to obtain accurate high frequency characterization of k Ω -range impedance measurements, the state-of-the-art has reported interferometry-based architectures as the most appropriate and efficient solution. The interferometry principle is to generate an electromagnetic wave interference between the DUT and a tuner (TUN) resulting in a nil residue of reflection

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coefficient (Γ) as is

$$\Gamma_{residue} = \frac{\Gamma_{TUN} + \Gamma_{DUT}}{2} [8]. \quad (1)$$

Using interferometry principle, M. Moertelmaier et al. have presented accurate results for doping concentrations measurements in 1–20 GHz range [3]. In addition to the VNA, Moertelmaier’s architecture is based on directional couplers, data acquisition converters, microwave amplifiers, and mixers. Due to high precision on calibration, doping concentrations ranging from 10^{15} to 10^{20} atoms/cm³ have been measured for bipolar samples and nanoscale p-n junctions.

T. Dargent et al. have reported reconfigurable interferometer at 3.5 GHz for an RF input power of -30 dBm attaining precise measurements of 0.1 fF MOS capacitors [7]. Previously, K. Haddadi et al. have also demonstrated interferometer measurements of aqueous solution of dissolved sodium chloride at 2.45 GHz and observed 78 dB/(mol/l) sensitivity for 0 - 0.22 mol/l range [8]. In both works, Haddadi’s architecture is based on directional couplers for power division-recombination, and a mechanical impedance tuner able to validate Equation (1). Having a reduced complexity in comparison to Moertelmaier’s implementation, Haddadi’s interferometer achieve a comparable performance.

Despite interferometry-based systems achieve accurate high frequency, high impedance measurements, such circuitry retains a directional coupler as a mandatory building block. Actually, high performance couplers allow splitting and recombining electromagnetic microwaves which interfere to a nil $\Gamma_{residue}$ as defined in Equation (1). Such couplers are often millimeter sized which are hardly feasible in system-on-chip (SoC). Moreover, the interferometer principle described in Equation (1) implies that

$$\angle \Gamma_{TUN} \approx -\angle \Gamma_{DUT}. \quad (2)$$

In order to address capacitive DUT measurements, reconfigurable delay lines are mandatory for the TUN device as K. Haddadi and M. Moertelmaier have presented. Such a characteristic impedes a SoC implementation since reconfigurable high quality factor inductances are not feasible in advanced integrated circuit technologies. In absence of a SoC interferometer-based solution, this work innovates designing an integrated reflectometer in BiCMOS 55 nm technology, able to measure accurately at high frequency, high impedance devices for SMM applications.

III. REFLECTOMETER SYSTEM ANALYSIS

Being one of the most famous technique of impedance measurements, the Wheatstone bridge architecture was chosen as a potential candidate to an integrated reflectometer. Wheatstone bridge, illustrated in Figure 1, assesses the DUT reflection coefficient (Γ_{DUT}) using a voltage divider formed by Z_1, Z_2 and a tuner circuit (Z_{TUN}). Such tuner is responsible to transpose the VNA impedance (Z_{VNA}) from 50 Ω to a vicinity of a calibration device. Using a calibration device with an impedance similar to Z_{DUT} , the calibration residue can be defined as

$$\Gamma_{residue} = \frac{V_R}{V_I} = \frac{Z_2}{Z_1 + Z_2} - \frac{Z_{DUT}}{Z_{TUN} + Z_{DUT}}, \quad (3)$$

where V_I is the voltage formed by the incident wave (VNA port 1) in the input node of the reflectometer and V_R is the differential voltage from Z_{DUT} and Z_1, Z_2 voltage divider (see Fig. 1). Such V_R is buffered by the digital calibration circuitry to become the reflection wave (VNA port 2) in the output node of the reflectometer. For a known voltage divider factor $F = \frac{Z_2}{Z_1 + Z_2}$, the design equation of a tuner circuit is

$$Z_{TUN} = Z_{DUT} \frac{1 + \Gamma_{residue} - F}{F - \Gamma_{residue}}. \quad (4)$$

In order to improve impedance matching in the VNA port 1, we should design $Z_1 + Z_2 = Z_{VNA}$. If we chose $Z_1 = Z_2$, we have $F = 0.5$ while $\Gamma_{residue} \rightarrow 0$, therefore $Z_{TUN} \approx Z_{DUT}$. Thus, Z_{TUN} should be a reconfigurable capacitor used as a new impedance normalization from which the reflectometer will be referred to. In order to achieve a calibrated value, Z_{TUN} should be digital reconfigured. Such a digital calibration circuit is responsible to evaluate $\Gamma_{residue}$ while iterates to the best Z_{TUN} candidate, aiming a $\Gamma_{residue}$ minimization. With this goal, an instrumentation buffer accesses V_R , and an analog-to-digital converter (ADC) provides an estimation of $\Gamma_{residue}$ to an FPGA implemented algorithm. For specific digital calibration circuit, Z_{TUN} is implemented using a varactor diode biased by a digital-to-analog converter (DAC) through a choke inductor (1 mH).

If a $\Gamma_{residue}$ minimum is found (e.g. -60 dB for fF measurements), the reflectometer is assumed calibrated. After calibration, such reflectometer circuit verifies the equilibrium

$$Z_1 Z_{DUT} \approx Z_2 Z_{TUN}, \quad (5)$$

at a frequency of interest. Measurements can be drawn using the VNA port 2, as we have

$$S_{21} = \Gamma_{DUT}^e = \frac{Z_{DUT}^e - Z_{TUN}}{Z_{DUT}^e + Z_{TUN}}, \quad (6)$$

where Γ_{DUT}^e and Z_{DUT}^e are estimated DUT reflection coefficient and impedance respectively for a calibrated Z_{TUN} .

At this point, we may highlight some performance requirements for the digital calibration circuit. In order to measure accurately fF capacitors with an aF precision, DAC and ADC should have near 10-bits precision. However, high speed converters are not required because FPGA-based digital calibration has relaxed conversion time constraints. Due to designed BiCMOS 55 nm varactor characteristics (see Section IV for details), 8-bits ADC/DAC are established, which leads to 2.0 aF precision for a span from 0.9 to 1.4 fF. Furthermore, the FPGA algorithm should be based on a cost function from Equation (3). According to $\Gamma_{residue}$ characteristics (see Section V for details), the FPGA algorithm could be a gradient-based minimum research.

Since linearity and low noise are mandatory for calibration precision and measurements accuracy, Z_1, Z_2 should be low resistance value for low thermal noise, and Z_{TUN} should be operated in linear region. Such requirements are validated for the design considerations presented in Section IV. Thus, the buffer, part of the digital calibration circuitry, remains as the source of noise and non-linearity. In order to operate our reflectometer in comparable environment to Moertelmaier’s [3] and Dargent’s [7] solutions, we shall have an input RF power of -30 dBm, for a bandwidth from 1 to 20 GHz, $\Gamma_{residue} < -60$ dB,

and guarantee a buffer's low-noise high-linear operation. The digital calibration circuit design is out of the scope of this paper and from this point it will be considered as an ideal circuitry.

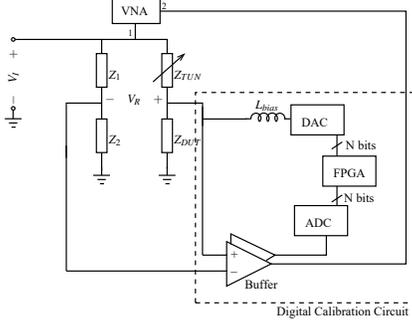


Fig. 1. Reflectometer System based on Wheatstone bridge technique: illustration.

IV. REFLECTOMETER CIRCUIT DESIGN

Reflectometer system based on Wheatstone bridge technique was described in Section III and illustrated in Figure 1. The proposed architecture is circuit-level designed for fF instrumentation with aF accuracy in 1 – 20 GHz frequency range. Moreover, such a reflectometer should respect reliability constraints due to process variability and temperature variation (from -55 to 125 °C). The reflectometer design is considered as follow: $\Gamma_{residue} \leq -60\text{dB}$, 8-bits precise digital reconfiguration, having VNA port 1 matched ($S_{11} \leq -20\text{dB}$ in Fig 1), and assuming an ideal digital calibration circuit (see Figure 1).

The proposed reflectometer is implemented in BiCMOS 55 nm technology. Such technology presents advantageous characteristics for microwave applications. First, this technology has reliable poly- and active-resistors which prevents drifts in voltage divider mesh and guaranteeing a stable voltage divider factor. Second, this technology combines thick and ultra-thin gate oxide with a minimum length of 55 nm, and thus fF varactors are available with aF precision. Finally, the ultra-thick metal layers are available in BiCMOS 55 nm technology which is essential for microwave transmission lines routing.

A. Voltage Divider Factor

Constituted of Z_1 , Z_2 , the voltage divider factor is designed with resistors. By choosing $Z_1 + Z_2 = Z_{VNA}$, the reflection coefficient is guarantee to $S_{11} \leq -20\text{dB}$ excepting any reliability degradation (i.e. process variability and temperature variation). In a simple manner, we designed $Z_1 = Z_2 = 25\Omega$ resistors. Furthermore, we minimize the sensitivity of $\Gamma_{residue}$ to F by choosing $F = 0.5$.

Regarding the resistor devices availability in BiCMOS 55 nm technology, we have performed a complete study of device sensitivity due to temperature variation, global- and local-variability. Global variability was evaluated by the variation of sheet resistance. Local variability was evaluated using mismatch parameters of a Pelgrom's modelling. Temperature dependence was estimated by the normalized temperature coefficient. Balancing the reliability trade-offs, we designed Z_1 and Z_2 as unsilicided p+ poly resistor having $5.67\mu\text{m}$ width and $0.9\mu\text{m}$

length. The voltage divider building block, including the required dummy devices, presents a layout area of $17.89 \times 22.25\mu\text{m}^2$.

B. Impedance Tuner

In order to accurately measure 1 fF DUT with aF precision, the impedance tuner (Z_{TUN}) is designed according to Equation (4). Thus, Z_{TUN} should be a variable capacitor. Regarding BiCMOS 55 nm technology options for a varactor design, thick gate oxide option has been chosen in association with the minimum gate length.

The n+ poly gate, n-well MOS capacitor having two cells of one finger MOS gate capacitor implements the impedance tuner. Each MOS capacitor cell has $1.35\mu\text{m}$ width and 55 nm length. Having chosen thick gate oxide, Z_{TUN} varactor can be operated from -2.5 V to 2.5 V bias. In order to guarantee a Z_{TUN} linear operation, we decided to bias the varactor from -0.5 V to 0.5 V. Under such bias point, Z_{TUN} minimum value is 0.9 fF, and maximum value is 1.4 fF. Consequently, the digital calibration code is fixed to 8 bits aiming aF Z_{TUN} reconfiguration (i.e. 2.0 aF). The impedance tuner building block presents a layout area of $3.15 \times 6.22\mu\text{m}^2$.

C. Reflectometer System Integration

Voltage divider and impedance tuner are integrated in monolithic reflectometer using BiCMOS 55nm. The final area consumption is $25 \times 25\mu\text{m}^2$. Assuming an ideal digital calibration circuit, behavioral modeling of the global system has been done for: buffer, ADC/DAC, and FPGA-based calibration. In Section V, simulation results are derived from the electrical modeling of voltage divider and impedance tuner.

V. REFLECTOMETER SIMULATION RESULTS

The reflectometer system is electrical simulated using silicon based models. In order to verify a proper operation, a calibration to 1 fF at 10 GHz has been considered. Then, we demonstrate how the reflectometer operates during a measurement step of $C_{DUT} \in [0.1\text{fF}, 10\text{fF}]$ at 10 GHz. Figure 2 shows the reflectometer calibration step when the digital calibration code is swept in $[0, 255]$ interval. The digital code is presented using a decimal representation. We highlight the fast convergence for a minimum $\Gamma_{residue} = -69.59\text{dB}$ at the code 64. From a $C_{TUN} = 1\text{fF}$ calibration, Figure 3 demonstrates the reflectometer measurement operation. While C_{DUT} is swept from 0.1 to 10 fF, the reflectometer is able to estimate DUT capacitor (C_{DUT}^e) using Equation (6).

In order to validate the reflectometer operation over low microwave frequency requirements, we evaluate minimum $\Gamma_{residue}$ calibration for 1–20 GHz frequency bandwidth operation. Figure 4 confirms a stable operation with minima $\Gamma_{residue} \approx -70\text{dB}$ at the code 64 while calibration frequency is changed. Near 1 GHz calibration, a $\Gamma_{residue} \leq -80\text{dB}$ at the code 63 is obtained.

The reflectometer stability is evaluated for temperature variation from -55 to 125 °C and process variability. For C_{TUN} calibrated to 1 fF, Figure 5(a) shows a slight variation from code 71, in low temperature, to code 51, in high temperature. Such a variation in digital calibration code is confirmed in Figure 5(b), as we can see minima shifting ($\Gamma_{residue} \approx -70\text{dB}$). Anyway, the digital calibration circuitry is always able to find a minimum

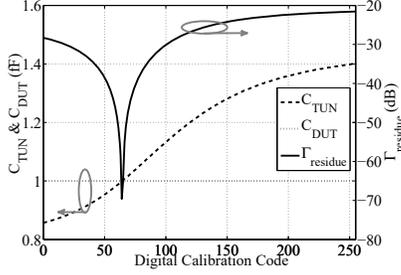


Fig. 2. Reflectometer calibration step for a 1 fF at 10 GHz (digital calibration code is in [0, 255] interval).

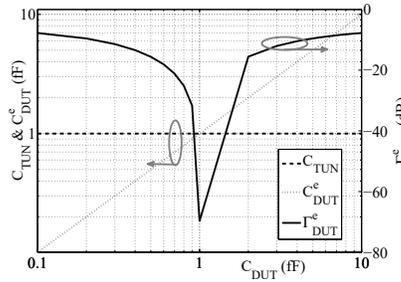


Fig. 3. Reflectometer measurement step for $C_{DUT} \in [0.1 \text{ fF}, 10 \text{ fF}]$, using a $C_{TUN} = 1 \text{ fF}$ calibration.

(see Figure 5). Accurate measurements could be fulfilled if temperature environment does not suffer huge changes.

Performance degradation due to process variability is estimated using 1k point Monte Carlo simulation. Voltage divider factor (F) mostly affected by mismatch variability has presented $\bar{F} = 0.5$ with $\bar{\sigma}_F = 483.2 \cdot 10^{-6}$. The varactor capacitor (C_{TUN}) calibrated to 1 fF at 10 GHz has presented $\bar{C}_{TUN} = 0.995 \text{ fF}$ with $\bar{\sigma}_{C_{TUN}} = 77 \text{ aF}$. The residue of reflection coefficient ($\Gamma_{residue}$) issued from a 1 fF at 10 GHz calibration has presented $\bar{\Gamma}_{residue} = -76.5 \text{ dB}$ with $\bar{\sigma}_{\Gamma_{residue}} = 8.8 \text{ dB}$. F , C_{TUN} , and $\Gamma_{residue}$ histograms are not presented. Owing to BiCMOS 55 nm technology process variability, reflectometer retains a reliable operation.

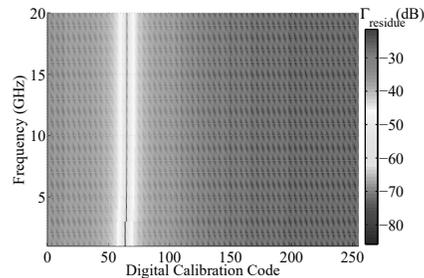


Fig. 4. Reflectometer calibration step for a 1 fF over low microwave frequency (1–20 GHz).

VI. CONCLUSIONS

An original reflectometer system has been designed to measure 1 fF capacitance at low microwave frequency (1–20 GHz)

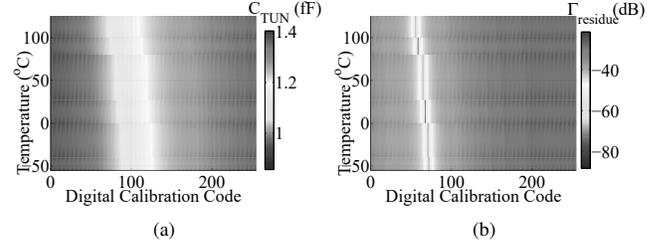


Fig. 5. Reflectometer calibration step for a 1 fF at 10 GHz under temperature variation: (a) C_{TUN} and (b) $\Gamma_{residue}$.

with aF precision. Using a Wheatstone bridge architecture, a fully integrated SoC reflectometer has been proposed and implemented in BiCMOS 55 nm technology. Electrical simulation results have proved a linear tuner reconfiguration from 0.9 to 1.4 fF, having an 8-bits precision (i.e. 2.0 aF). Operating with a calibrated $\Gamma_{residue} \approx -70 \text{ dB}$, the designed reflectometer can accurately measure devices-under-test from 0.1 to 10 fF. Even under temperature variation, a minimum $\Gamma_{residue}$ can always be found owing to the digital calibration circuitry. Estimated process variability slightly influences the reflectometer calibration which is negligible for such SMM applications.

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