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ABSTRACT

We briefly review the basic concepts of junction capacitance and the peculiarities related to amorphous semiconductors, paying tribute to Cohen and to his pioneering work. We extend the discussion to very high efficiency silicon heterojunction (SiHET) solar cells where both an amorphous semiconductor, namely hydrogenated amorphous silicon, and heterojunctions are present. By presenting both modeling and experimental results, we demonstrate that the conventional theory of junction capacitance based on the depletion approximation in the space charge region, cannot reproduce the capacitance data obtained on SiHET cells. The experimental temperature dependence is significantly stronger than that of the depletion-layer capacitance, while the bias dependence yields underestimated values of the diffusion potential, leading to strong errors if applied to the determination of band offsets using the procedure proposed precedingly in the literature. We demonstrate that this is not related to the amorphous nature of a-Si:H, but to the existence of a strongly inverted c-Si surface layer that requires minority carriers to be taken into account in the analysis of the junction capacitance.

1. Introduction

In recent years silicon heterojunctions (HET) combining crystalline silicon (c-Si) wafers with thin layers of hydrogenated amorphous silicon (a-Si:H) have received much attention in the world of photovoltaics due to their ability to build high efficiency solar cells. Indeed, many research groups have demonstrated cells with more than 22% conversion efficiency [1–5], and the new world record for silicon cells has been reached in April 2014 by Panasonic, with a value of 25.6% based on Si-HET and rear contacting concepts [6]. Despite these impressive results there is still a lot to learn about this kind of heterojunction cells. In particular, the assessment of the band diagram parameters at the heterojunctions, the role of the a-Si:H properties, the choice of the charge collection electrodes and the characterization of interfaces need to be further investigated in order to further improve the cell performance. This necessitates the collection and analysis of results from various characterization techniques. Space charge spectroscopy using capacitance and conductance measurements is one of the useful techniques that can be deployed to this purpose. Silicon HETs associate a very high quality and almost defect free crystalline semiconductor with a defect rich amorphous one. Space charges have different origins and different behaviors in these two very different materials.

The theory of junction capacitance in crystalline semiconductors can be found in textbooks on the physics of semiconductor devices (see for instance [7]) and is usually based on the depletion approximation. On the other hand, strong efforts have also been deployed to analyze capacitance measurements of junctions formed on a-Si:H. We want here to pay homage to the pioneering work of Cohen [8,9]. In this paper we briefly recall the fundamentals of capacitance spectroscopy in both crystalline and amorphous semiconductors. We then emphasize the failure of the usually accepted and almost universally used depletion layer approximation for the junction capacitance. This is demonstrated both for the use of the *C–V* method that could in principle be used to extract band offsets, and also for the temperature dependence. We provide the physical explanation of this failure that is not due to the amorphous nature of the emitter, but to the existence of a strong inversion layer at the c-Si surface.

2. Samples and procedures

We measured the capacitance on high efficiency ($\eta > 21\%$) solar cells coming from EPFL-IMT and INES that were fabricated on n-type crystalline silicon of similar doping density ($\approx 10^{15}$ cm^{-3}) [4,5]. These solar cells were not intended for bi-facial illumination

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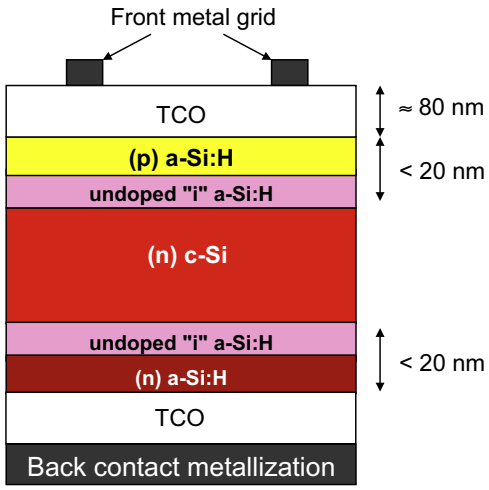

Fig. 1. Schematic view of the investigated silicon heterojunction solar cells (texturing has been omitted for simplicity).

so the non-illuminated side was metallized on the whole wafer area (Fig. 1). Small pieces (between a few mm^2 up to 0.5 cm^2) were cut inside larger area solar cells. We first measured the current–voltage characteristics in order to check that the samples were not affected after cutting in particular with regards to shunts from the edges. The capacitance was then measured using Agilent 4284A and E4980A precision LCR meters at different DC biases (from -2 V to $+0.5$ V) and frequencies (20 Hz–1 MHz). Measurements were performed in two different cryogenic systems: one under nitrogen gas exchange in the range 90–320 K and the other with a cold finger chamber pumped down to 10^{-6} mbar in the range 90–420 K. We verified that measurements performed in either cryostat were reproducible and repeatable, crosschecked measurements performed in both cryostats and found that the results were identical within 5%.

3. Elements of junction capacitance theory

3.1. What do we really measure?

It is well known that charges of opposite sign develop at equilibrium in each side of a p–n junction (defining the space charge region) due to the difference in work function of the two materials in contact. These charges are modified by an external bias applied to the junction through an external circuit. Following a slight positive change in applied bias $\delta V_a=\delta(\varphi_p-\varphi_n)$, φ_p and φ_n being the electrochemical potential on the p- and n-side, respectively, a small quantity of electrons will flow from the n-side into the space charge region, giving a charge variation δQ^e (which is thus negative for a positive change in applied bias considering the negative charge of electrons) while a small quantity of holes will enter the space charge region from the p-side, producing a charge variation δQ^h of opposite sign, $\delta Q^h=-\delta Q^e$, as depicted in Fig. 2.

The instrument used to measure the capacitance only "sees" the flow of electrons that circulate in the external circuit, and the capacitance is thus given by

$$C=-\frac{\delta Q^e}{\delta V_a}=+\frac{\delta Q^h}{\delta V_a}. \tag{1}$$

We emphasize that this is the general and correct definition of the measured capacitance. It is more often used that $C=-\delta Q_n/\delta V_a=+\delta Q_p/\delta V_a$, where δQ_n and δQ_p are the charge variations within the n- and p-side of the space charge region, respectively. This only corresponds to the correct expression if

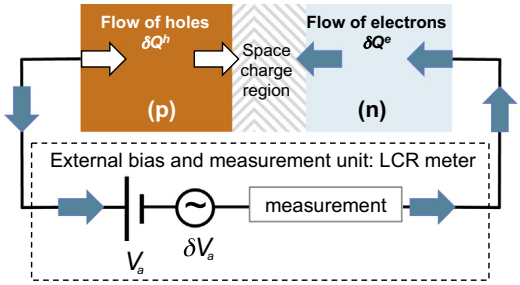

Fig. 2. Principle and schematic circuit of the capacitance measurement. Arrows indicate the charge flows following a small positive change in the bias applied to the p–n junction.

$\delta Q^e=\delta Q_n$ and $\delta Q^h=\delta Q_p$. These equalities are true in the depletion layer approximation that assumes that the density of both types of carriers can be neglected compared to that of dopants within the space charge region. Indeed, in that case after a small positive bias change electrons entering the space charge region from the n-side will just compensate some of the positively charged donors that determine Q_n; similarly holes entering the space charge region from the p-side will just compensate some of the negatively charged acceptors that determine Q_p. However these equalities do not hold for strongly asymmetrical p–n homojunctions (p^+–n or p–n^+) or in some cases of heterojunctions. For instance, as we will detail later, for p^+–n junctions and for the (p) a-Si:H/(n) c-Si heterojunction solar cells the flow of holes entering the space charge region from the p-side will also produce an increase in the charge of holes located on the n-side of the junction, very close to the junction interface where the density of holes may be larger than that of donors. Noticing that δV_a is equal to the variation in total electrostatic potential drop, $\delta V_a=\delta(V(-\infty)-V(\infty))$, and integrating twice Poisson's equation, we obtain

$$\delta V_a=-\int_{-\infty}^{\infty}\frac{x\delta\rho(x)}{\varepsilon(x)}dx, \tag{2}$$

where $\varepsilon(x)$ is the dielectric permittivity at position x, and $\delta\rho$ is the change in space charge density.

We express the variation in charge density

$$\delta\rho(x)=\delta\rho^h(x)+\delta\rho^e(x), \tag{3}$$

where $\delta\rho^h$ and $\delta\rho^e$ are the variations of space charge densities due to exchanges with holes and electrons, respectively. If we assume that the dielectric permittivity is the same in a-Si:H and in c-Si, $\varepsilon(x)=\varepsilon$, then a simple expression can be obtained for the junction capacitance

$$C=\frac{\varepsilon A}{\langle w\rangle}, \tag{4}$$

where A is the junction area and

$$\langle w\rangle=\langle x^e\rangle-\langle x^h\rangle, \tag{5}$$

is the separation between the first momentum of charge variation due to exchanges with electrons and that due to exchanges with holes

$$\langle x^e\rangle=\frac{\int_{-\infty}^{\infty}x\delta\rho^e(x)dx}{\delta Q^e}, \tag{6}$$

and

$$\langle x^h\rangle=\frac{\int_{-\infty}^{\infty}x\delta\rho^h(x)dx}{\delta Q^h}. \tag{7}$$

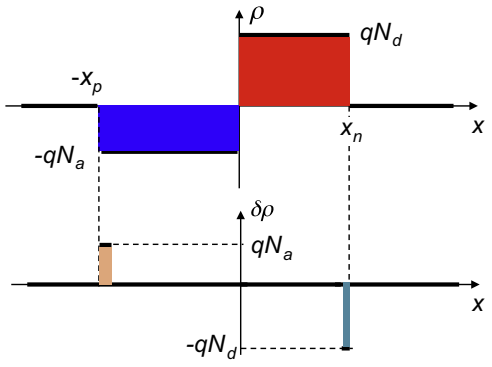

Fig. 3. Space charge density at a p–n homojunction within the depletion approximation (top) and changes following a small positive increment of the applied bias (bottom).

3.2. Application of the bias dependence of the capacitance in crystalline junctions

3.2.1. Crystalline silicon homojunctions and the depletion approximation

The illustration in case of an abrupt p–n homojunction on a crystalline semiconductor with doping densities N_a and N_d on the p- and n-side, respectively, is shown in Fig. 3 within the depletion approximation.

Due to the depletion of free carriers, the space charge extends over a distance x_n on the n-side and x_p on the p-side, and the charge density is constant on both sides within these regions, equal respectively to qN_d and $-qN_a$, q being the positive unit charge. Following a small positive change of applied bias, recharging of electrons occurs on the n-side in a very narrow region at the edge space region, and recharging of holes occurs in the same way in a very narrow region at the edge space region on the p-side. Therefore, $\langle w\rangle$ is equal to the total width of the space charge layer, $\langle w\rangle = x_n + x_p$, which leads to the expression of the widely used depletion layer capacitance

$$C = \frac{\varepsilon A}{x_p + x_n}. \tag{8}$$

Relating the potential drop across the junction to the extent of the space charge, one then obtains the dependence of the capacitance on the applied voltage

$$\frac{A}{C} = \sqrt{\frac{2}{q\varepsilon}\frac{N_a + N_d}{N_a N_d}\left(V_d - \frac{2k_B T}{q} - V_{app}\right)}, \tag{9}$$

V_d being the total diffusion potential (also called built-in voltage), k_B the Boltzmann constant and T the temperature. The term $2k_BT/q$ is a small correction to the simple theory and arises when the tails of the two majority carrier distributions near the edge of the depletion region are taking into account [7]. These are the basic equations of the capacitance–voltage technique or C–V method. For uniform doping a plot of $1/C^2$ versus applied dc voltage yields a straight line, the slope of which is determined by the doping densities. The technique has been extended to derive the profile of doping density or, more exactly, majority carrier density in non uniformly doped semiconductors using the slope of a $1/C^2 - V$ curve (see for instance [10] and references therein). In addition the intercept of the linear extrapolation to the voltage axis of such a curve is $V_d - 2k_BT/q$, which allows one to deduce the diffusion potential.

3.2.2. Heterojunctions and the depletion approximation

For heterojunctions, the same picture holds within the depletion approximation; one has just to take account of the values of permittivity, ε_p and ε_n on the p- and n-side, respectively, so that

$$\frac{A}{C} = \frac{x_p}{\varepsilon_p} + \frac{x_n}{\varepsilon_n}, \tag{10}$$

and

$$\frac{A}{C} = \sqrt{\frac{2}{q}\left(\frac{\varepsilon_p N_a + \varepsilon_n N_d}{\varepsilon_p \varepsilon_n N_a N_d}\right)\left(V_d - \frac{2k_B T}{q} - V_{app}\right)}. \tag{11}$$

Like for homojunctions, in case of uniform doping a plot of $1/C^2$ versus applied dc voltage yields a straight line, the slope of which is determined by the doping densities (and electrical permittivities), and the intercept of the linear extrapolation to the voltage axis yields the diffusion potential V_d.

In heterojunctions the C–V profiling method was further extended to the determination of band offsets. This was proposed and detailed by Kroemer for isotype n–N or p–P heterostructures (the lower-case and upper-case letters referring to the narrow and wide band gap semiconductors, respectively) [11,12] using the depletion through a Schottky contact. However band offsets can also be inferred in p–N or P–n heterojunctions from the measurement of V_d as proposed by Forrest [13].

Let us consider a P–n heterojunction. From the analysis of the band diagram at equilibrium (Fig. 4), it is found that [13]

$$qV_d = E_{gn} - \delta_p - \delta_n + \Delta E_V, \tag{12}$$

$\delta_p = (E_F - E_V)_p$ and $\delta_n = (E_C - E_F)_n$ being the position of the Fermi level in each semiconductor relative to the majority carrier band edge, E_{gn} the band gap of the n-type narrow gap semiconductor, and ΔE_V the difference in the bottom of the valence band between the small band gap and the wide band gap semiconductors. Since δ_p and δ_n are in principle known from the doping of the semiconductors (in amorphous semiconductors the position of the Fermi level is not known directly from the doping but can be inferred from measurements of the dark conductivity or from photoemission spectroscopy), the measurement of V_d from the intercept of $1/C^2$ versus V_{app} allows one to deduce the valence band offset from the knowledge of E_{gn} using Eq. (12). For an N–p heterojunction E_{gn} and ΔE_V have to be replaced by E_{gp} (band gap of the p-type narrow gap semiconductor) and ΔE_C (conduction band offset), respectively, in Eq. (12). Thus for an N–p heterojunction the conduction band offset can be deduced from the measurement of V_d and from the knowledge of δ_p, δ_n, and of the band gap of the narrow gap semiconductor.

It has to be emphasized that expressions (8)–(11) of the capacitance are based on the depletion approximation. This assumes that the charge of both types of free carriers is negligible compared to that of the ionized donors or acceptors close to the junction interface. However for highly asymmetric homojunctions or depending on the band offsets in heterojunctions the density of

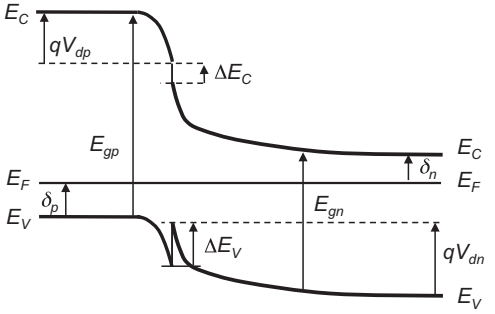

Fig. 4. Equilibrium band diagram at a P–n heterojunction (wide gap p-type semiconductor and small gap n-type semiconductor), showing the definitions of material and interface parameters. The band offsets are counted positively as indicated in this figure.

minority carriers close to the junction interface in one of the semiconductors can be very large and even exceed that of ionized doping atoms (i.e. that of majority carriers in the semiconductor bulk). In that case a strong inversion layer builds up at the interface and the charge due to these minority carriers has to be taken into account in the calculation, as will be considered in Section 3.4.

3.3. Specificity of a-Si:H

Compared to their crystalline counterpart amorphous semiconductors like a-Si:H generally contain a much higher density of electronic defects resulting in a large density of states (DOS) distributed across the whole band gap. Thus the space charge in a-Si:H at the vicinity of a junction is not directly related to the doping atoms but rather to the DOS and in particular its value at the Fermi level. Another striking difference for the electrical properties in a-Si:H compared to c-Si concerns the dynamic behavior. Indeed, in defect-free crystalline semiconductors the junction capacitance given by Eqs. (8)–(11) does not depend on frequency in the normally used measurement frequency range (up to a few MHz). This is because the dielectric relaxation time is much lower than the period of the ac signal. On the contrary in a-Si:H the capacitance can be frequency dependent. Indeed, electrical transport is less efficient than in c-Si due to lower carrier mobility and lower carrier densities even for doped a-Si:H, thus yielding a much longer dielectric relaxation time. Moreover, since the space charge is related to band gap states and to their occupation, free carriers that flow into (or out of) the space charge region must be captured (or released) by those gap states. These capture/release processes also have characteristic inverse times that may be comparable to the measurement frequency. These phenomena have been studied by several workers in the 80's mainly to quantify the density of states in a-Si:H from frequency and temperature dependent capacitance measurements in Schottky diodes using either an equivalent electrical diagram approach [14,15] or analytic calculations [16,17]. However we want to pay special tribute to Cohen, because he and his co-workers have produced a pioneering work to explain the dynamical behavior of junction space charges in a-Si:H and to provide theoretical analyses of space charge spectroscopy for the determination of material properties [8,9].

Here we only briefly recall the main aspects and results by considering the space charge region in n-type a-Si:H at a Schottky barrier at equilibrium. The charge density in the space charge region is mainly determined by states at and close to the bulk Fermi level. To a first approximation it has a typical exponential spatial dependence (this is the exact dependence if the DOS is constant). The characteristic width of this exponential dependence is the Debye length, L_D, of the material that is given by [9,18]

$$L_D^2 = \frac{\varepsilon}{q^2 g(E_F)}, \tag{13}$$

where $g(E_F)$ is the DOS at the bulk Fermi level.

Regarding the dynamic behavior, since only states close to the Fermi level may change their occupation upon a small change in applied bias, the characteristic response time τ_c for charge variation reads

$$\tau_c(x) = \frac{1}{2\nu_n \exp\left[-((E_C - E_F)(x)/k_B T)\right]}, \tag{14}$$

ν_n being the attempt-to-escape frequency, and E_C the bottom of the conduction band. The characteristic response time is the inverse of the sum of capture and emission frequencies of both electrons and holes. Since we consider here a Schottky barrier formed on n-type a-Si:H, capture and emission frequencies of holes are neglected compared to that of electrons. Moreover, at the Fermi level emission and capture frequencies of electrons are identical, which leads to the factor of 2 in the denominator in Eq. (14) [18], that had often been omitted [9,16] with no direct consequence since the value of the attempt-to-escape frequency is not well known. For a Schottky barrier on p-type material, a similar expression would hold with ν_p, the attempt-to-escape frequency of holes and $E_F - E_V$ instead of ν_n and $E_C - E_F$, respectively. This response time depends on the distance to the junction due to the band bending. Considering that the capacitance is measured by applying a small ac voltage at a given angular frequency ω, this leads to the definition of a cut-off abscissa x_ω defined as the abscissa where the product $\omega\tau_c(x_\omega)$ is equal to 1. In a simplified approach, one can assume that states at the Fermi level located at $x < x_\omega$ (closer to the junction) are too deep in the band gap and thus have a too long characteristic time to be able to follow the ac signal while those located at $x > x_\omega$ are fully able to follow the ac signal. Therefore changes in space charge occur only at $x > x_\omega$ with a distribution that has a characteristic width L_D. This is schematically depicted in Fig. 5.

As a consequence, the mean position $\langle x^e \rangle$ of the variation in space charge density is $\langle x^e \rangle = x_\omega + L_D$. In p-type a-Si:H, equivalent relations hold with exchanges of holes and $\langle x^h \rangle$ instead of $\langle x^e \rangle$. Since x_ω depends on both frequency and temperature, the capacitance exhibits a temperature and frequency dependence that can be summarized as a capacitance "step" on a C versus T plot, the step being shifted to higher temperatures when the measurement frequency is increased [18,19]. Regarding the variation of space charge and capacitance with DC bias, the amorphous nature of the material also implies a deviation from the linear dependence of $1/C^2$ that prevails in crystalline junctions [20].

3.4. Calculation of the a-Si:H/c-Si heterojunction capacitance

In n-type c-Si, the charge density at any point x (we take $x = 0$ as the a-Si:H/c-Si interface) is given by

$$\rho(x) = q[p(x) - n(x) + N_d], \tag{15}$$

where N_d is the doping density that is uniform in the high quality c-Si wafers that are used for very high efficiency solar cells, of the order of 10^{15} cm^{-3}.

The total space charge in c-Si can be expressed as

$$Q^{c-Si} = Q^{h,c-Si} + Q^{depl,c-Si}, \tag{16}$$

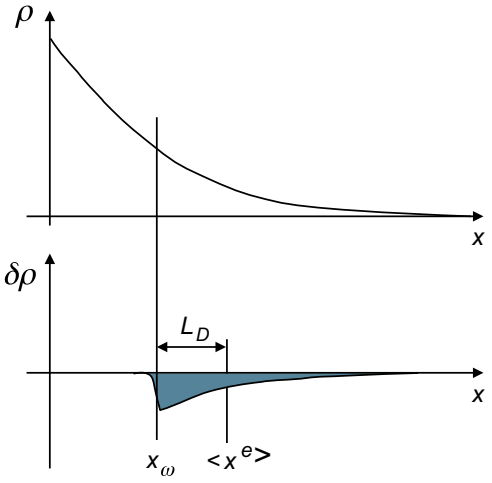

Fig. 5. Static space charge density at an n-type a-Si:H Schottky barrier and changes in space charge density following a small positive increment of the applied bias on a timescale $1/\omega$.

where $Q^{h,c\text{-}Si}$ is the charge due to holes and $Q^{depl,c\text{-}Si}$ is the depletion charge, given respectively by

$$Q^{h,c-Si} = q\int_0^\infty p(x)dx, \tag{17}$$

$$Q^{depl,c-Si} = q\int_0^\infty [N_d - n(x)]dx. \tag{18}$$

The c-Si wafer has a given thickness $d^{c\text{-}Si}$ (of the order of 150 μm) that is much larger than the thickness of the space charge layer, and the back contact can be considered as having negligible impact on the measured capacitance so we will neglect it here and the c-Si wafer can be regarded as semi-infinite. The total charge in (n) c-Si is balanced by a charge of opposite sign on the p-side. However, since the thickness of a-Si:H in HET cells in only of the order of a few nanometers, and also due to time constants that can be much longer in a-Si:H to refill the space charge with holes, one has to take account of the charge at the collecting electrode on the a-Si:H, $Q^{p\text{-}electrode}$, so that the global charge neutrality reads

$$Q^{c-Si} + Q^{a-Si:H} + Q^{p-electrode} = 0 \tag{19}$$

Recently we have developed a complete analytical calculation of the a-Si:H/c-Si heterojunction capacitance [21]. We have solved Poisson's equation in both c-Si and a-Si:H, taking into account the overall charge neutrality from Eq. (19). It is noteworthy that this calculation takes into account the contribution of holes in c-Si in Eq. (15) and the charge of holes ($Q^{h,c\text{-}Si}$) which are neglected in the depletion approximation approach. Then the capacitance has been calculated from the derivative of the charge of extracted or refilled electrons at the n-side with respect to applied voltage as described by Eq. (1), with $\delta Q^e = \delta Q^{depl,c\text{-}Si}$. This calculation of the a-Si:H/c-Si heterojunction capacitance has been improved by adding the (i) a-Si:H buffer layer existing in a real solar cell and by introducing the finite thickness of the (p) a-Si:H layer. Of course, it is also possible to suppress the contribution of holes in our calculation. We have checked that this leads to very similar results as the simplified depletion approximation calculation.

4. Results and discussion

4.1. Bias dependence

Since the DOS at the Fermi level of doped a-Si:H can reach very high values (10^{18}–10^{20} cm^{-3} eV^{-1}), the Debye length in a-Si:H is only a few nanometers. One can thus think the (p) a-Si:H/(n) c-Si junction to behave like a p+/n junction. In that case, according to the depletion theory, the voltage drop on the p+ side is negligible compared to that on the c-Si n-side, and the non-crystalline character of a-Si:H should not play a significant role in the determination of the capacitance that can thus be expected to exhibit a linear dependence of $1/C^2$ versus DC voltage with almost no frequency dependence.

Such a linear dependence is indeed observed experimentally under reverse bias and moderate direct bias in a wide temperature range as shown in Fig. 6. However the intercept voltage, V_{int}, of these linear portions appears to be quite low. As an example, at $T=300$ K, the intercept voltage is 0.56 V. The Fermi level position in bulk c-Si is 0.25 eV. The position of the Fermi level in (p) a-Si:H is estimated at about 0.3 eV from temperature dependent conductivity measurements performed on (p) a-Si:H layers deposited on glass substrates. If one assumes that the intercept voltage is equal to the diffusion potential (corrected by $2k_BT/q$) and applying Eq. (12), one then obtains that the valence band offset is almost zero. This is much less than values reported recently in the literature: about 0.4 eV obtained from planar conductance measurements performed on (p) a-Si:H/(n) c-Si interfaces coming from various institutes [22] and similar values (or even larger for higher hydrogen content and thus larger band gap of a-Si:H) obtained from photoelectron spectroscopy [23]. In addition, we can note that the value of $V_{int}=0.56$ V is much lower than the open circuit voltage measured under normalized AM1.5G conditions, $V_{oc}=725$ mV. The low value of V_{int} obtained from the C–V analysis will be explained in Section 4.3.

4.2. Temperature dependence

The temperature dependence measured at 0 V on the high efficiency silicon heterojunction solar cell from EPFL is shown in Fig. 7.

One can see that above 300 K the capacitance exhibits a frequency independent behavior (so-called quasistatic behavior) and increases significantly with temperature. The small frequency dispersion of C–T curves at low temperatures has also been observed by other authors [24,25], and is related to hole response and collection at the p-side, but we will not go further into these details here. The overall capacitance increase with temperature is very similar to that previously observed on the high efficiency cell from INES [21].

4.3. Discussion

The depletion approximation does not allow one to reproduce the large increase of capacitance observed experimentally. This is shown in Fig. 8, where the capacitance calculated within the depletion approximation is compared to experimental data.

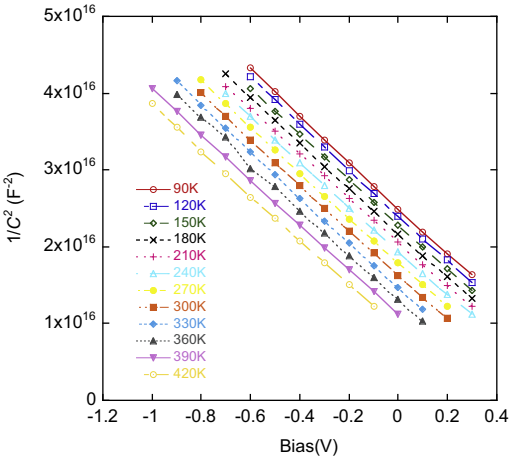

Fig. 6. Plot of $1/C^2$ as a function of applied DC bias at various temperatures from experimental data measured on a high efficiency Si HET cell from EPFL. Lines are linear fits to the data.

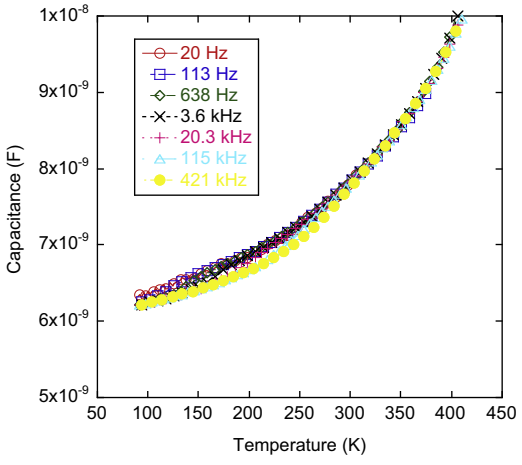

Fig. 7. Temperature dependence of the capacitance at various frequencies measured on a high efficiency Si HET cell from EPFL at zero DC bias.

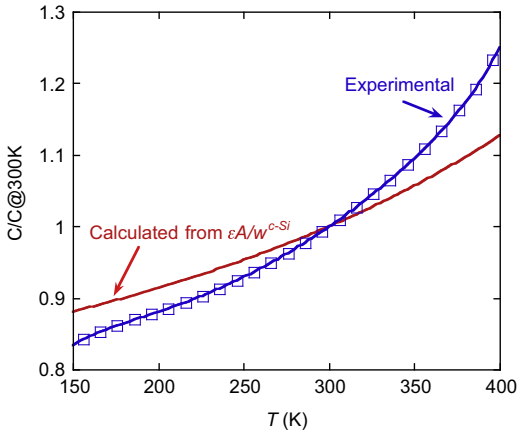

Fig. 8. Comparison of the temperature dependence of the capacitance (normalized to its value at 300 K) calculated from the depletion approximation and measured on a high efficiency Si HET cell from EPFL.

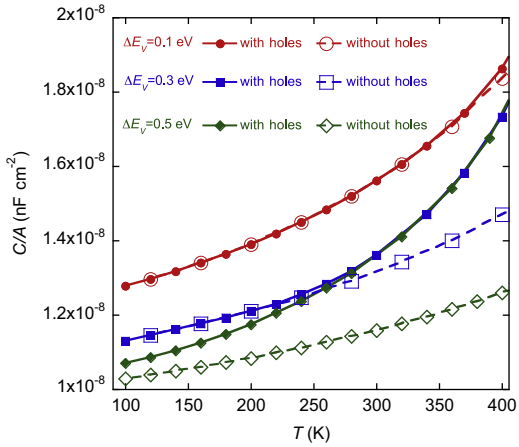

Fig. 9. Temperature dependence of the capacitance from the full analytical calculation. We increased the band bending in c-Si by increasing the valence band offset from 0.1 to 0.5 eV. The full symbols show the result of the full calculation that takes into account the holes in the space charge density, while the open symbols correspond to the calculation where the contribution of holes has been suppressed.

One might argue that strong temperature dependence of physical parameters like the position of the Fermi level in a-Si:H or the valence band offset might be able to reconcile calculated and experimental data. This is not the case and we have shown that even with unreasonable temperature dependences of these parameters the calculated capacitance still exhibits weaker temperature dependence than observed experimentally [21]. This emphasizes the failure of the existing theory of the depletion capacitance that neglects minority carriers in the calculation of the space charge in c-Si. Indeed, the capacitance calculated without neglecting the term due to holes in the space charge exhibits a stronger temperature dependence than the one calculated by neglecting the holes' contribution to the space charge (which was shown to coincide with the depletion capacitance calculation) if a strong inversion layer is present at the c-Si surface. Such a strong inversion layer exists if the band bending in c-Si is large enough so that the hole concentration at the silicon surface becomes larger than the doping density. In our calculations we increased the band bending in c-Si by increasing the valence band offset, without changing the bandgap in a-Si:H and the position of the Fermi level in (p) a-Si:H referred to the valence band ($\delta^{a\text{-}Si:H}$). The results are shown in Fig. 9.

One can see the strong correlation between these curves and the charges $Q^{h,c\text{-}Si}$ and $Q^{depl,c\text{-}Si}$ defined by Eqs. (17) and (18) that are shown in Fig. 10.

Indeed, for ΔE_V=0.5 eV, $Q^{h,c\text{-}Si}$ is larger than $Q^{depl,c\text{-}Si}$ in the whole temperature range and the two capacitances calculated with or without including the holes in the space charge density calculation are different. On the opposite, for ΔE_V=0.1 eV, $Q^{h,c\text{-}Si}$ is smaller than $Q^{depl,c\text{-}Si}$ in the whole temperature range and the two capacitances calculated with or without including the holes are identical. Finally, the case ΔE_V=0.3 eV is intermediate since strong inversion occurs above 300 K, where indeed the two capacitances are different while they coincide at low temperature where no strong inversion exists.

In order to clarify the role of holes in the calculation of the capacitance we refer to Section 3.1. Indeed, when no strong inversion at the c-Si surface exists, the static charge density and the variation in charge density following a small positive change in applied bias are depicted in Fig. 11.

The mean position of the negative charge variation $\langle x^e \rangle$ is given by the width of space charge in c-Si, $w^{c\text{-}Si}$, while the mean position of the positive charge variation $\langle x^h \rangle$ is related to the charge response in a-Si:H, leading to a capacitance given by

$$C = \frac{\varepsilon A}{w^{a-Si:H} + w^{c-Si}}. \tag{20}$$

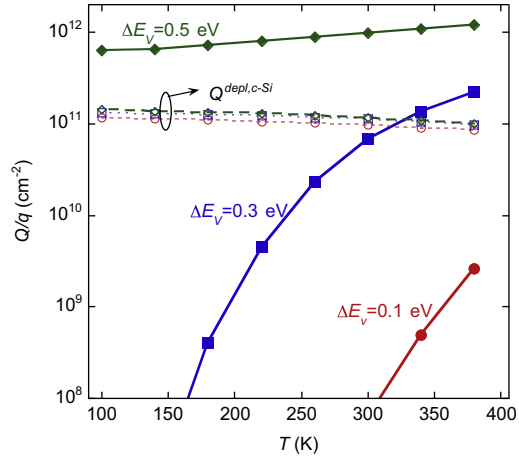

Fig. 10. Calculated temperature dependence of the charge due to holes in (n) c-Si (full symbols) in the Si HET cell for the three values of valence band offset. Also shown is the depletion charge (open symbols), much less sensitive to ΔE_V.

Actually, if the thickness of a-Si:H is of the order or smaller than L_D, part of the charge is confined at the hole collecting electrode, i.e. at the TCO/a-Si:H contact, meaning that $w^{a\text{-}Si:H}$ cannot be larger than $d^{a\text{-}Si:H}$. Since $w^{a\text{-}Si:H} \ll w^{c\text{-}Si}$, a good approximation of the capacitance is simply

$$C \approx \frac{\varepsilon A}{w^{c-Si}} \tag{21}$$

However, if strong inversion exists at the c-Si surface and the flow of holes from the p-side essentially contributes to increase the strong hole charge located in c-Si (that is much larger than the charge in a-Si:H), the mean position of positive charge variation $\langle x^h \rangle$ is shifted into c-Si and becomes close to the strong inversion layer extent, x_{inv}, as depicted in Fig. 12.

The capacitance is then given by

$$C = \frac{\varepsilon A}{w^{c-Si} - x_{inv}}. \tag{22}$$

So far we have demonstrated that in the presence of a strong inversion layer the capacitance calculated without neglecting the holes is different from the depletion capacitance calculation and that it exhibits a stronger temperature dependence. However the physical reason for this stronger increase is still not explained. To explain it, let us focus on the temperature dependence for zero

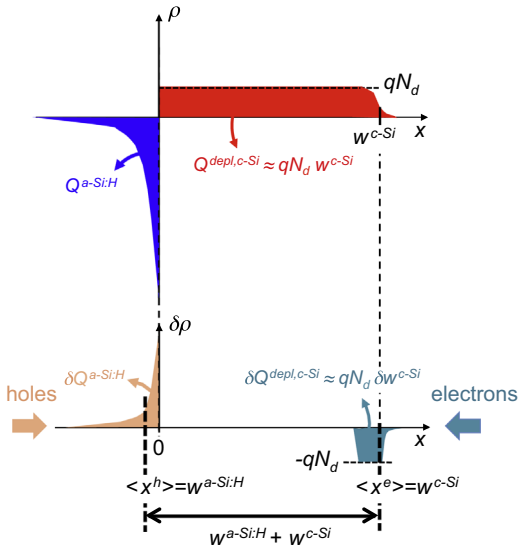

Fig. 11. Space charge density at the Si heterojunction, and the changes due to electrons and holes flowing into the space charge region following a small positive increment in applied bias if no strong inversion layer exists at the c-Si surface.

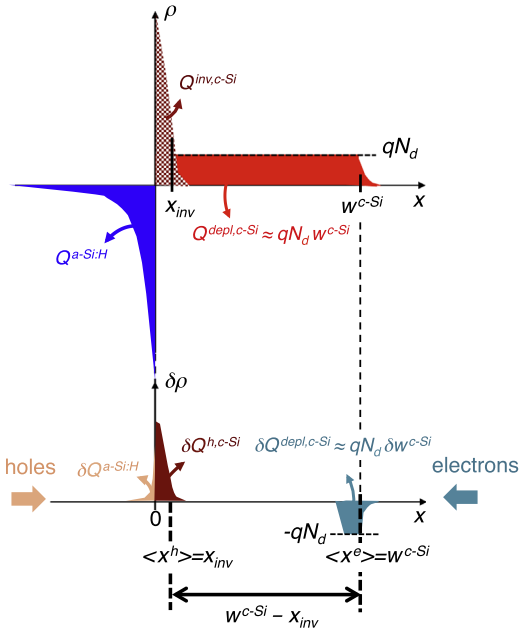

Fig. 12. Space charge density at the Si heterojunction, and the changes due to electrons and holes flowing into the space charge region following a small positive increment in applied bias if a strong inversion layer exists at the c-Si surface.

applied DC voltage. For the first case (no strong inversion) the temperature dependence of the capacitance is given by that of $w^{c\text{-}Si}$, related to the potential drop in c-Si, namely,

$$w^{c-Si}(T) = \sqrt{\frac{2\varepsilon}{qN_d}\, V_d^{c-Si}(T)}, \tag{23}$$

with

$$qV_d^{c-Si}(T) = E_g^{c-Si}(T) + \left[\Delta E_V - \delta^{a-Si:H} - qV_d^{a-Si:H}\right](T) - k_B T \ln\frac{N_C(T)}{N_d}. \tag{24}$$

For the second case (with strong inversion) the capacitance depends on $w^{c\text{-}Si} - x^{inv}$, which represents the width of the actual depletion layer limited by the strong inversion region. This width

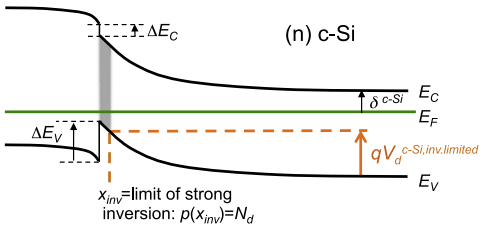

Fig. 13. Equilibrium band diagram at the (p) a-Si:H/(n) c-Si heterojunction if a strong inversion region exists at the c-Si surface, showing the limit of the strong inversion region and the potential drop in the depleted region that is limited by the strong inversion region.

is thus simply related to the potential drop within this region

$$[w^{c-Si} - x_{inv}](T) = \sqrt{\frac{2\varepsilon}{qN_d}\, V_d^{c-Si,inv.limited}(T)}, \tag{25}$$

$V_d^{c\text{-}Si,inv.limited}$ being designated as the strong inversion limited depletion layer potential drop as illustrated in Fig. 13, given by [21]

$$qV_d^{c-Si,inv.limited}(T) = E_g^{c-Si}(T) - 2k_B T \ln\frac{\sqrt{N_C(T)N_V(T)}}{N_d}. \tag{26}$$

As we already mentioned above the temperature dependence of the central term $(\Delta E_V - \delta^{a\text{-}Si:H} - V_d^{a\text{-}Si:H})$ in Eq. (24) is weak compared to that of the two other terms. Therefore, if we compare the temperature dependencies of the two potential drops in Eqs. (24) and (26), we can observe that the one of $qV_d^{inv.limited}$ is enhanced by the factor of 2 in the last term. This enhanced temperature dependence results in the stronger increase of capacitance with temperature in presence of a strong inversion layer.

It is noteworthy that the presence of the (i) a-Si:H buffer layer does not modify the explanation for the stronger temperature dependence. The (i) a-Si:H layer modifies the total charge in a-Si:H that includes the contributions of both (p) a-Si:H and (i) a-Si:H. Increasing the (i) a-Si:H layer thickness will increase the weight of a-Si:H in the charge balance and thus increase the potential drop in a-Si:H and decrease the band bending in c-Si, resulting in a decrease of $Q^{h,c\text{-}Si}$. This is illustrated in Fig. 14 where we compare the temperature dependence of $Q^{h,c\text{-}Si}$ calculated for three values of (i) a-Si:H buffer layers (d_i=0, 10, 40 nm) and for three values of valence band offsets (ΔE_V=0.1, 0.3, 0.5 eV). Thus, for thick (i) a-Si:H layer the strong inversion layer may disappear. However, as long as strong inversion exists the average position of the charge variations due to refilling of holes from the p-side and of electrons from the n-side is as depicted in Fig. 12, with the consequence of the stronger increase of capacitance with temperature as compared to the depletion approximation.

Finally, we emphasize the link between the strong temperature dependence of the capacitance and the low value of the intercept voltage V_{int} observed in Section 4.1. Indeed, when a strong inversion layer of holes exists at the c-Si surface, application of a DC bias, V_a, will result in a shift of $V_d^{c\text{-}Si,inv.limited}$, Eq. (24) being modified by substracting V_a in the right hand side. Thus the intercept voltage, V_{int}, obtained from $1/C^2$ versus V_a plot is not equal to the total diffusion potential but is equal to $V_d^{c\text{-}Si,inv.limited}$. As one can see from the band diagram in Fig. 13 this potential can be smaller than the diffusion potential. This in turn will yield underestimated values of the valence band offset when Eq. (12) is applied with V_{int} used as V_d. Actually, if strong inversion exists at the surface, the intercept voltage being equal to $V_d^{c\text{-}Si,inv.limited}$ does not depend any more on the band offset as evidenced in Eq. (26). This had already been observed on (n) a-Si:H/(p) c-Si where ΔE_C appears instead of ΔE_V in Eq. (12), while computer simulations had shown that the intercept voltage of the linear extrapolation of $1/C^2$ versus V_a saturates at a given value when increasing ΔE_C

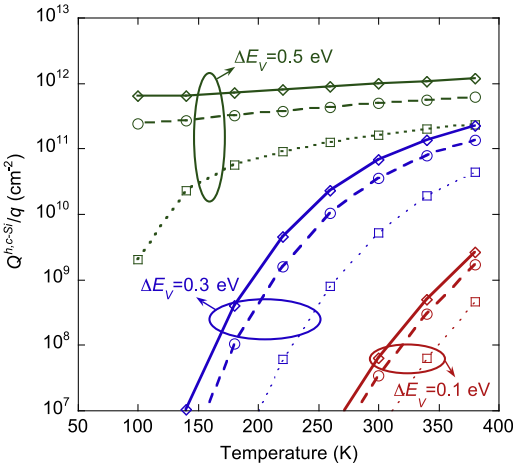

Fig. 14. Influence of the (i) a-Si:H layer thickness, d_i, on the hole inversion charge in c-Si: d_i=0 nm (◇), d_i=10 nm (○) and d_i=40 nm (□), calculated for three values of valence band offset (ΔE_V=0.1 eV, 0.3 eV, and 0.5 eV).

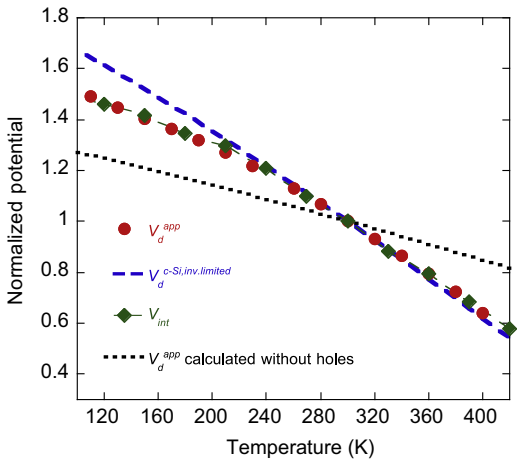

Fig. 15. Temperature dependence of V_d^{app} (●) for capacitance data measured at zero DC bias and V_{int} (◆) deduced from the $1/C^2$ plots of Fig. 6. The dashed line corresponds to $V_d^{c\text{-}Si,\ inv.\ limited}$ calculated from Eq. (26), while the dotted line corresponds to V_d^{app} obtained from the numerical calculation of the capacitance for ΔE_V=0.5 eV without taking account of holes in the space charge. All quantities have been normalized to their value at 300 K.

instead of increasing linearly as would be expected if V_{int} would follow V_d [26]. The same origin of the stronger temperature dependence and low intercept voltage value of $1/C^2$ can be further evidenced if one considers the apparent diffusion voltage, V_d^{app}, obtained from capacitance data as defined in [21]:

$$V_d^{app}(T) = \frac{qN_d\varepsilon}{2}\left(\frac{A}{C}\right)^2. \quad (27)$$

Indeed, one can see in Fig. 15 that the temperature dependences of the experimental V_{int} and V_d^{app} quantities are the same. Moreover, we can observe that above 240 K this temperature dependence is very well reproduced by that of $V_d^{c\text{-}Si,inv.limited}$ calculated from Eq. (26). As explained above, the slope is markedly stronger (by about a factor of 2) than the one obtained from the numerical calculation of the capacitance for ΔE_V=0.5 eV (where strong inversion conditions prevail) if one neglects the contribution of holes to the space charge density in the space charge region. Comparing our experimental data to $V_d^{c\text{-}Si,inv.limited}$ we can conclude that strong inversion conditions prevail above 240 K. At lower temperatures there is a slight deviation indicating that the hole inversion layer becomes weaker. As we have shown from our calculations, such a behavior can be expected for a valence band offset in the range 0.3–0.5 eV. However in the low temperature range one has to take care of transport in a-Si:H and to the TCO/a-Si:H interface that can also have an impact on the transition temperature above which the regime fully determined by strong inversion prevails. Note that the obtained range for the conduction band offset agrees with the values determined in our group from planar conductance measurements [22] and in other groups using other techniques [23]; to pay again tribute to Cohen, we can notice that he also published early results on the a-Si:H/c-Si band offsets from capacitance measurements, however not directly on solar cells and using another experimental method and procedure (namely from a voltage filling pulse method) and he also concluded that most of the band offset between a-Si:H and c-Si occurs at the valence band [27].

The depletion layer approximation had been first criticized by Gummel and Scharfetter from calculations on p^+n step homojunctions where these authors showed that the intercept voltage in highly dissymmetric junctions is not as expected from the simple depletion approximation [28]. However only very few papers in the literature dealt with this inversion layer related problem [29–31], and to our best knowledge, no indication on the temperature dependence had been published. It is amazing that the peculiar temperature dependence could be evidenced from measurements on solar cells combining a-Si:H and c-Si since one could think that a-Si:H, as a very defective material could greatly influence the capacitance behavior. As a matter of fact, the very thin a-Si:H layer combined with the high DOS in a-Si:H make the (p) a-Si:H/(n) c-Si junction behave as a p+n junction with a limited influence of the a-Si:H side, except for the creation of the strong inversion layer of holes at the c-Si surface. Moreover, the low deposition temperature and low deposition time of a-Si:H ensure that the junction is really abrupt and cannot suffer from diffusion of species during the junction formation which could modify the analysis. From this point of view one can say that the a-Si:H/c-Si heterojunction is a deal model system to reveal the weakness of the depletion layer capacitance theory and to emphasize that minority carriers have to be considered in the junction capacitance of heterostuctures where strong band bending produces a strong inversion layer.

5. Conclusions

We have reviewed the traditional depletion approximation theory for the capacitance analysis including the ingredients related to the continuum of gap states in amorphous semiconductors. We have shown that this theory is unable to describe the temperature dependence observed on high efficiency (p) a-Si:H/(n) c-Si heterojunction solar cells. Indeed, the increase of capacitance observed experimentally on solar cells is much stronger than predicted from the depletion capacitance theory. In addition, $1/C^2$ versus voltage plots do exhibit a linear behavior, which could make one confident in using the depletion approximation theory for the determination of band offsets assuming that the intercept of the linear extrapolation of the $1/C^2$ data with the voltage axis yields the diffusion voltage. However we have demonstrated that this intercept voltage is much lower than the actual diffusion potential, which leads to a strong underestimation of the valence band offset. So the depletion theory fails both in describing the temperature dependence and in determining the diffusion potential. We have shown that both failures can be attributed to the strong inversion layer of holes that builds up in such cells at the crystalline silicon surface, and we have detailed the physical explanation.

Acknowledgments

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