Single-Photon Avalanche Diodes (SPAD) in CMOS 0.35 μm technology

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Abstract:

Some decades ago single photon detection used to be the terrain of photomultiplier tube (PMT), thanks to its characteristics of sensitivity and speed. However, PMT has several disadvantages such as low quantum efficiency, overall dimensions, and cost, making them unsuitable for compact design of integrated systems. So, the past decade has seen a dramatic increase in interest in new integrated single-photon detectors called Single-Photon Avalanche Diodes (SPAD) or Geiger-mode APD. SPAD are working in avalanche mode above the breakdown level. When an incident photon is captured, a very fast avalanche is triggered, generating an easily detectable current pulse.

This paper discusses SPAD detectors fabricated in a standard CMOS technology featuring both single-photon sensitivity, and excellent timing resolution, while guaranteeing a high integration. In this work, we investigate the design of SPAD detectors using the AMS 0.35µm CMOS Opto technology. Indeed, such standard CMOS technology allows producing large surface (few mm^2) of single photon sensitive detectors. Moreover, SPAD in CMOS technologies could be associated to electronic readout such as active quenching, digital to analog converter, memories and any specific processing required to build efficient calorimeters[1] (Silicon PhotoMultiplier - SiPM) or high resolution imagers (SPAD imager). The present work investigates SPAD geometry. MOS transistor has been used instead of resistor to adjust the quenching resistance and find optimum value. From this first set of results, a detailed study of the Dark Count Rate

[1] SiPM is often used to measure the number of photons, proportional to the particle energy, which interacts with a scintillator. At the opposite, an imager gives both the number of hit pixels and there position. So, in particle physics, calorimetry corresponds to the energy measurement of particles even if any temperature measurement is done.

(DCR) has been conducted. Our results show a dark count rate increase with the size of the photodiodes and the temperature (at T=22.5°C, the DCR of a 10 µm-photodiode is 2020 count.s^{-1} while it is 270 count.s^{-1} at T=-40°C for a overvoltage of 800 mV). A small pixel size is desirable, because the DCR per unit area decreases with the pixel size. We also found that the adjustment of overvoltage is very sensitive and depends on the temperature. The temperature will be adjusted for the subsequent experiments.

1 Introduction

A Single-Photon Avalanche Diode (SPAD) is a semiconductor photon sensor operated in Geiger-mode where bias voltage is above the diode breakdown voltage (typical V_{br}=10 to 100 V) and associated to a quenching circuit [Ref 1]. A Silicon PhotoMultiplier (SiPM) is composed of hundreds of SPAD (about 10x10µm^2 up to 100x100 µm^2) realised on the same substrate and interconnected together to sum the photo-current coming from each of them. The typical density of SPAD is 100-10000 per mm^2. The first development started about 10 years ago in Russia [Ref 2]. Hamamatsu Photonics produces commercially SiPM-based circuits named Multi-Pixel Photon Counter (MPPC) since 2008. Currently, several technologies have also been developed by other companies such as Sensl, or Ketek. Micro-electronic CMOS technologies can also be used to develop specific SPAD and SiPM sensors with good performance [Ref 3][Ref 4]. We introduce in this paper our development of SPAD arrays using the CMOS-Opto “C35B4O1" technology proposed by CMP (Circuit Multi-Projects) in Grenoble and manufactured by AMS. This microelectronic technology has been chosen to design large arrays of high-resolution SPAD imagers for optical ultra low flux applications (for example, medical application [Ref 9] or high-energy astrophysics [Ref 8]). CMOS technologies allow integrating into the same substrate the SPADs and their specific readout electronic. In this paper, we present both the investigations on the SPAD design and resulting performance of the fabricated chips.

2 The Technology "CMOS-Opto C35B4O1", and breakdown voltage simulation

a) Characteristics of the AMS technology

The "AMS CMOS-Opto C35B4O1" process is made with a P epi-layer (thickness ≈14 μm) on a P type substrate. This 0.35μm CMOS-Opto process offers 4 metallization layers and 2 polysilicon layers. Figure 1 shows the cross-section.

AMS gives the value of 45 pA/cm^2 for the Dark current. P-epi wafers allow lower current leakage in the diode, then a lower dark current for a better sensitivity. This current is very low, which is ideal for the Geiger mode.

AMS gives the saturation current for PMOS: 240 μA/μm for L=0.35 μm and W=0.4 μm where L is the PMOS channel length and W the channel width. Depending on the electrical simulations of the transistor, we selected W=6 μm and L=0,7 μm. The aim is to have a resistive mode for V_{ds} = 0 to 1 V (V_{ds} is the drain-source voltage of the PMOS). The resistive mode range is from 10 kΩ to 100 kΩ depending on V_{gs} adjustment (V_{gs} is the gate-source voltage of the PMOS).

This technology is normally sensitive in the range 400-1000 nm [Ref 5] with optimal responsivity of 290 mA/W for a 550 nm wavelength and 330 mA/W for 850 nm.

b) The SIMS results

The first step was to study the different layers. There are 2 n_type layers, and 2 p_type layers of different doping levels to modify the field distribution across the structure. Figure 2 shows the summary table of SIMS results (Secondary ion mass spectrometry). These doping values have been found by SIMS, after components manufacturing.

c) Silvaco simulation: results

We use the doping profiles obtained by SIMS to determine the breakdown voltages. We expose here the simulation results with these profiles obtained. The Figure 3 presents a first simulation of the structure with the 4 zones and the doping correctly adjusted. The software "Silvaco" was used for these simulations. The result of these simulations at 22.5°C (Figure 4) gives us a breakdown voltage of 11.7 V and a guard ring of 40 V. At this point of our work, we can say that this technology is well suited to Geiger Mode.

3 Experimental results: Breakdown voltage

We present here the experimental results obtained for several isolated photodiodes of different diameters. The diameter of the photodiodes is between D=200 µm and D=2.7 µm. The size of the guard ring is 1.7 µm. The structural dimension is shown in Figure 5. The breakdown voltage values have been determined from the reverse current–voltage (I–V) characteristics, using a Keithley 2636A. A breakdown voltage of 11.7 V was measured at 22.5°C for photodiodes with a diameter greater than or equals to 10 µm. For photodiodes with a diameter lower than 10 µm diameter, we measured a higher breakdown voltage (near of guard ring 40 V) (Figure 6). Measurements have been repeated on a significant number of devices, showing a very good uniformity of the breakdown voltage values and confirming the reliability of the technology used for the Geiger mode. We measured on Figure 7 the temperature sensitivity for breakdown voltage: 9 mV.°C^{-1}. It is found that the temperature has a strong influence on breakdown voltage and therefore on the overvoltage.

4 Experimental results: Dark count rate

This is a first positive result concerning the dark count rate (DCR) using only one isolated photodiode. The behaviour of the quenching system is correct. At 22.5°C the dark count rate, for a photodiode of D=10 µm diameter, and an 800 mV overvoltage, is 2020 count.s^{-1} (Figure 8). At -40°C, the dark count rate, for a photodiode of D=10 µm diameter, and an 800 mV overvoltage, is 270 count.s^{-1} (Figure 9). These two results are presented in Figure 10. The Figure 12, summarises all these results. With a diameter lower than 10 µm, the DCR does not decrease anymore which confirms that the smallest diameter for this technology is about D=10 µm. The experimental set-up is presented in Figure 11. The Geiger pulses were measured with a universal counter "Hameg HM 8021-4" to the terminal of a resistor (100 Ω).

5 Conclusion

We introduced in the present document an investigation of the technology "CMOS-Opto C35B4O1" proposed by CMP (Circuit Multi-Projects) in Grenoble and manufactured by AMS for the Geiger mode. The main part of our work deals with the characteristics in the dark and allows us to find the size of the photodiode with the smallest DCR/um^2: 10µm. These values are comparable to those reported in literature for CMOS SPADs built in a similar technology [Ref 6] [Ref 7]. The first results that we have obtained are in good agreement with the challenge of the Geiger mode. Other results will be reported in a forthcoming paper.

6 References

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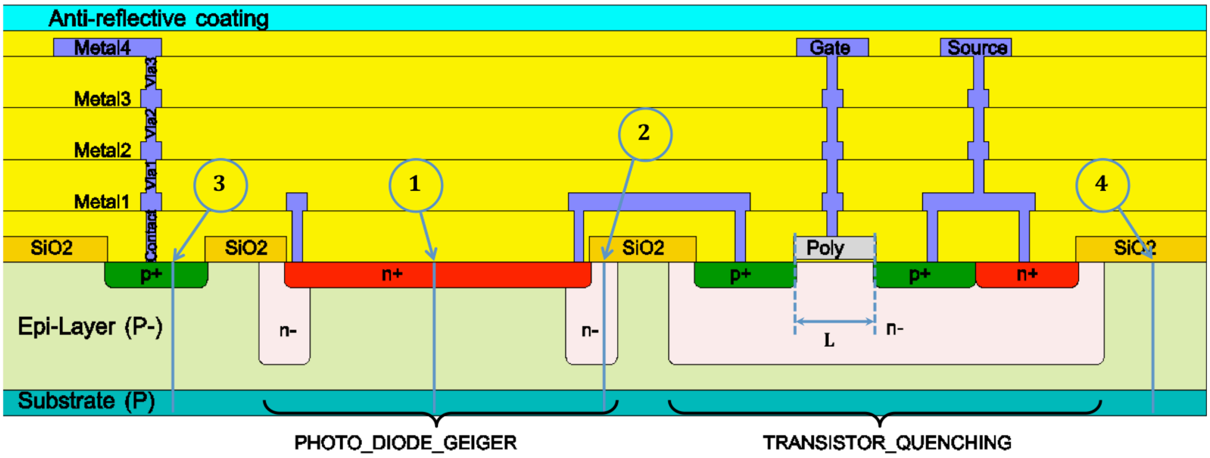

Figure 1: Cross-section of the Photodiodes design (SPAD) for Geiger mode in CMOS-Opto C35B4O1 and circuit.

	layer 1	layer 2	layer 3	layer 4
	A thin n+ type layer very sensitive to the light. This is the photodiode cathode	A n- type layer for the guard ring	A thin p+ type layer used for a good contact of the photodiode anode	A p- type epi-layer (on the substrat)
Thickness (µm)	0.2	2	0.2	14
Species	Arsenic	Phosphorus	Boron	Boron
Value of the surface doping (atom.cm^{-3})	$1x10^{21}$	$1x10^{17}$	$1x10^{20}$	$3x10^{17}$

Figure 2: SIMS Results.

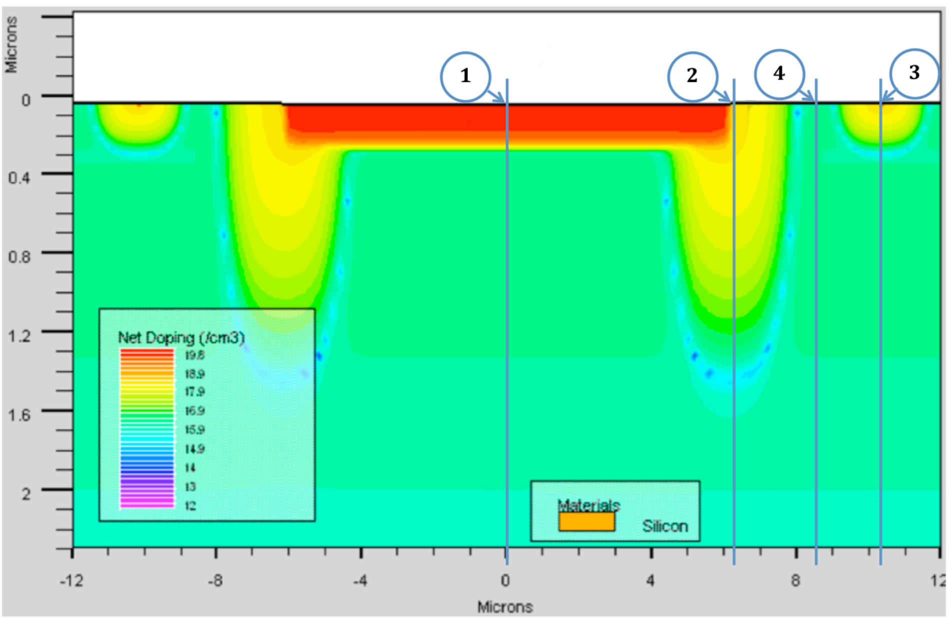

Figure 3: Cross-section, simulation "Silvaco" of the structure: N^{+}/P junction and guard ring N^{-} layer.

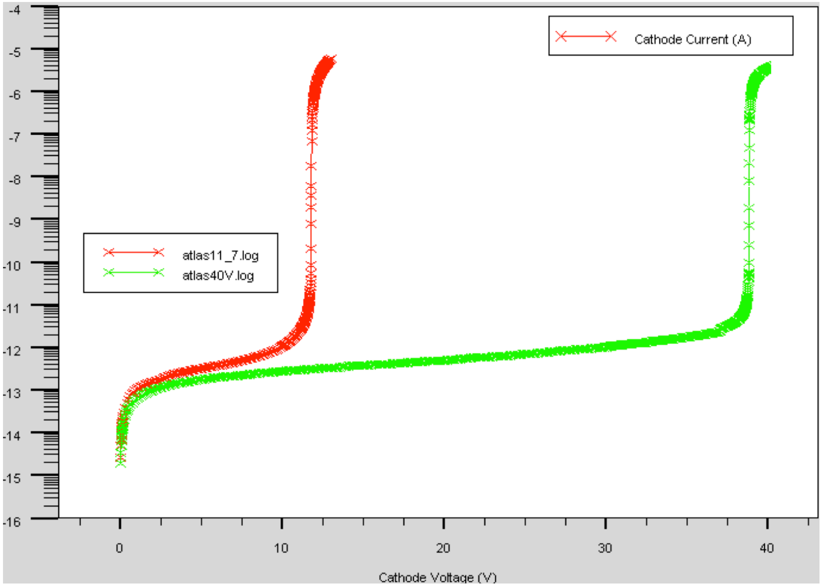

Figure 4: Breakdown voltage of the photodiode (11.7V) and breakdown voltage of the guard ring (40V) ; simulation results SILVACO obtained at 22.5°C

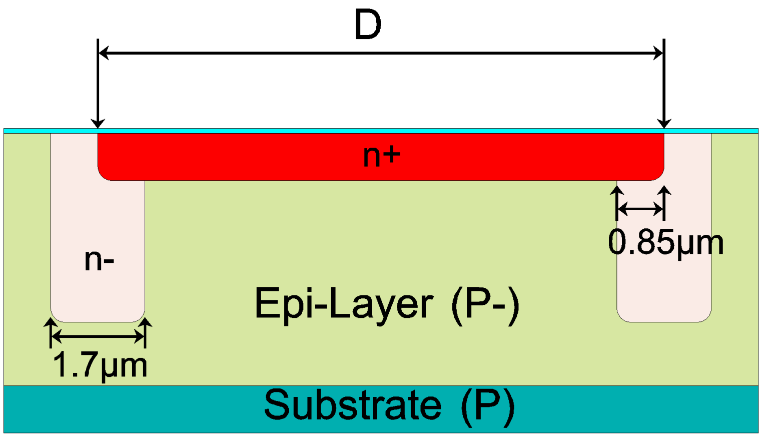

Figure 5: Schematic structure: Size of guard rings and size of photodiodes

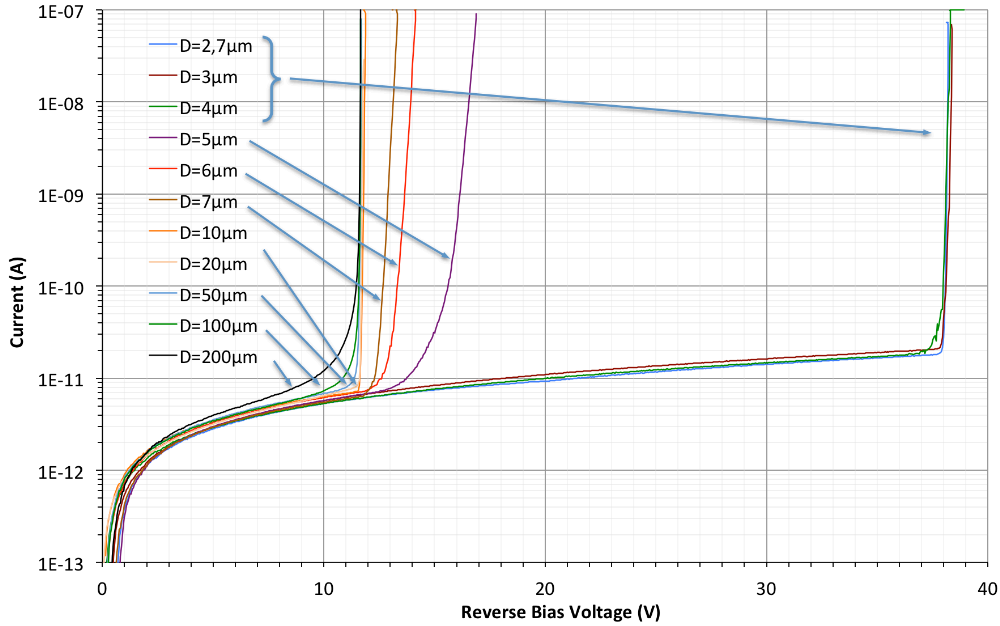

Figure 6: Breakdown voltage of the photodiodes; experimental results obtained at 25°C

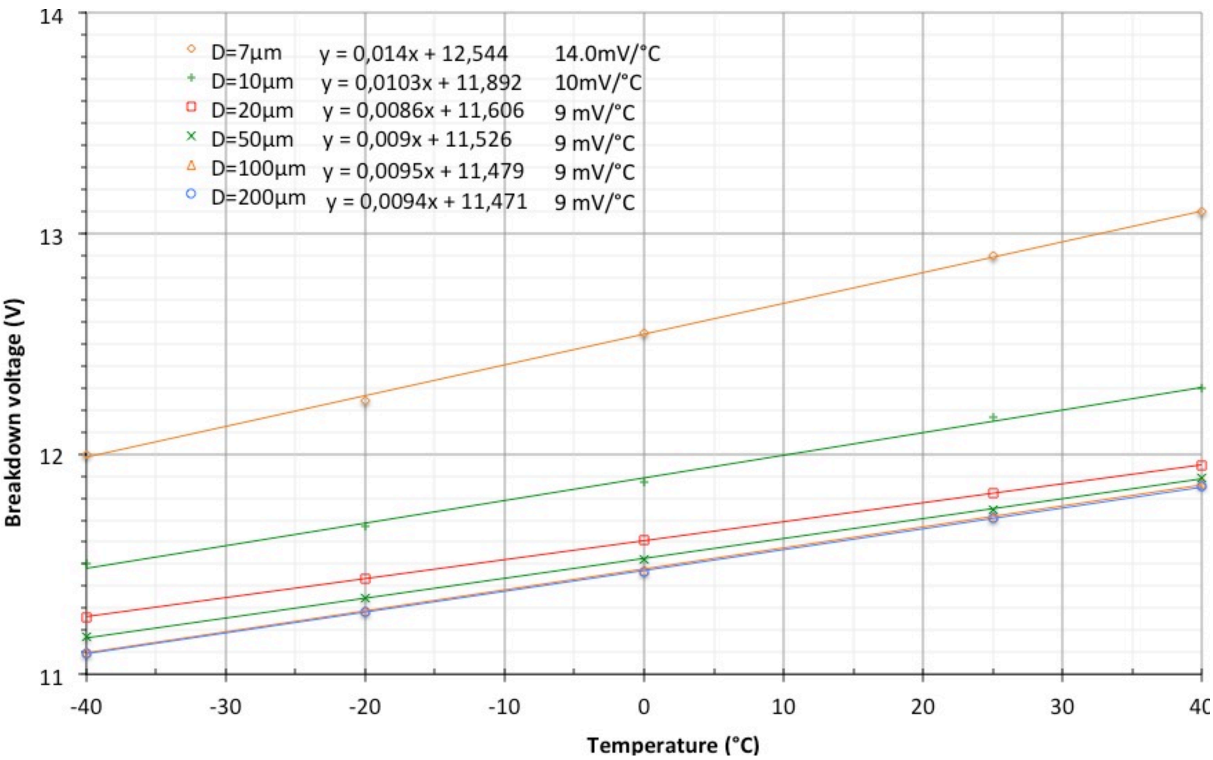

Figure 7: Breakdown voltage versus temperature for different size

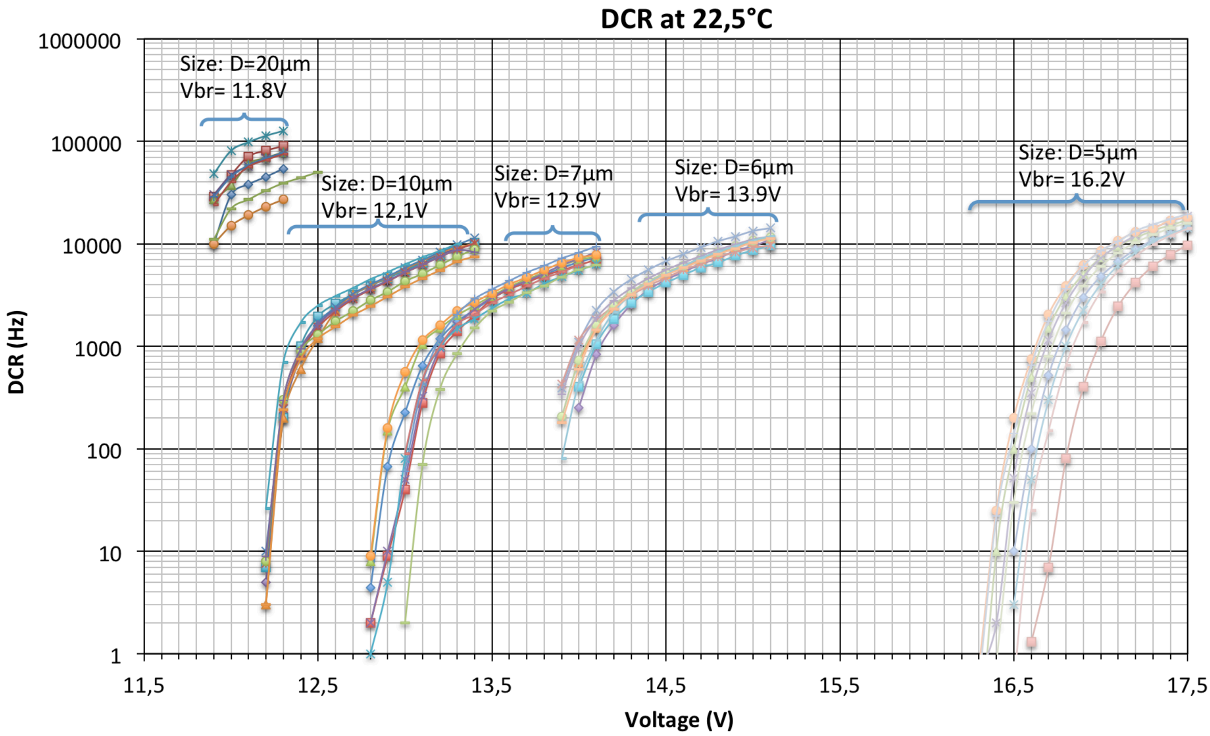

Figure 8: Dark count rate versus photodiode voltage at 22.5°C

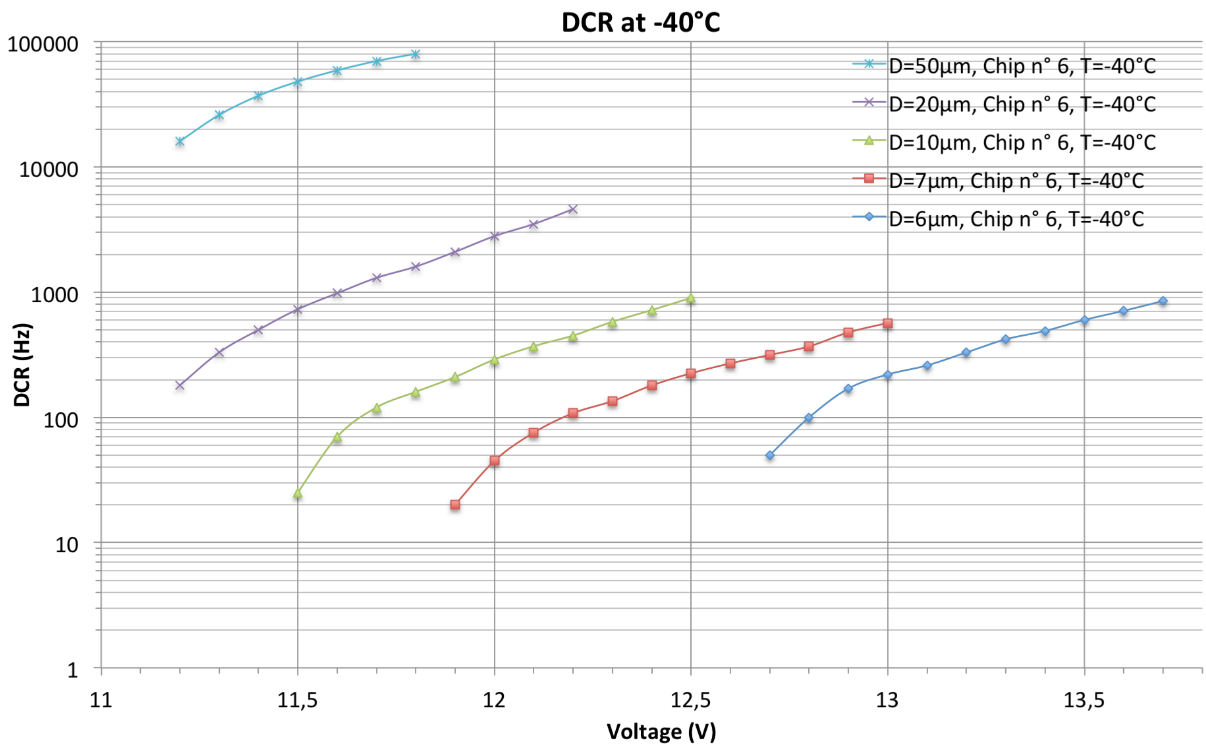

Figure 9: Dark count rate versus photodiode voltage at -40°C

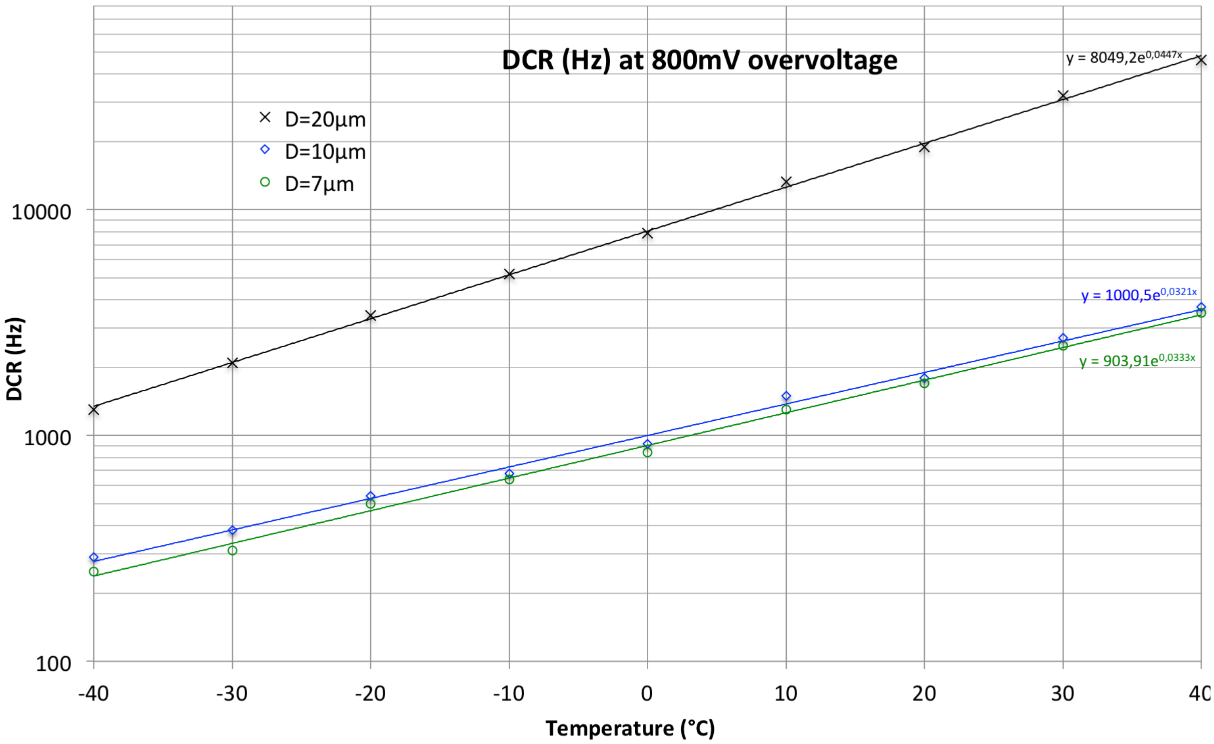

Figure 10: Dark count rate versus Temperature for three size at 800mV overvoltage

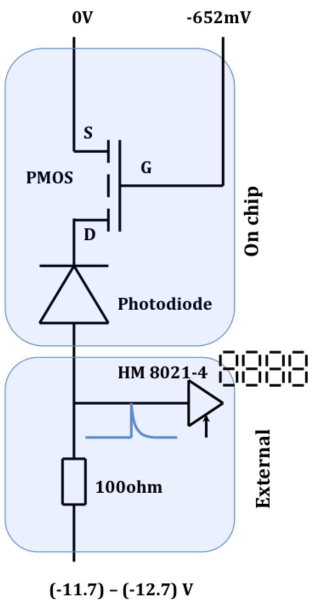

Figure 11: Electrical circuit used for dynamic characterizations, an exterior resistor (100 Ω for read) has been used.

D (µm)	22.5°C		−40.0°C	
	Vbr (V)	DCR at 800mV overvoltage (Count/s)	Vbr (V)	DCR at 800mV overvoltage (Count/s)
200	11.70	overflow	11.15	overflow
100	11.70	overflow	11.15	overflow
50	11.70	650000	11.15	45000
20	11.80	21000	11.18	1200
10	12.10	2020	11.49	270
7	12.90	1900	11.80	260
6	13.90	1900	12.40	260
5	16.20	1900	15.60	260

Figure 12: Summary table of our design