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**H. Achour[1,4], B. Cretu[2,3], J.-M. Routoure[1,3], R. Carin[1,3], A. Benfdila[4], E. Simoen[5] and C. Claeys[5,6]**

[1]University of Caen Basse-Normandie, UMR 6072 GREYC, F-14050, Caen, France
[2]ENSICAEN, UMR 6072 GREYC, F-14050, Caen, France
[3]CNRS, UMR 6072 GREYC, F-14032, Caen, France
[4]GRMNT, Mouloud Mammeri University of Tizi-Ouzou, Algeria
[5]Imec, Kapeldreef 75, B-3001 Leuven, Belgium
[6]E.E. Dept. KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium
**Corresponding author: bogdan.cretu@ensicaen.fr**

***Abstract*—The impact of cryogenic temperature operation on the short channel effects and analog performances was analysed on strained and unstrained p-channel SOI FinFETs. The main electrical parameters extracted from the saturation mode of operation are investigated and compared to those found at room temperature. Low frequency noise measurements at 10 K operation show that the carrier number fluctuations dominate the flicker noise in moderate inversion, while the access resistance noise contributions prevail in strong inversion.**

***Keywords*—FinFET; SOI; strain; DIBL; Early voltage; intrinsic gain; low frequency noise.**

## 1. Introduction

The multi-gate FinFET has been considered as a promising structure for the future technology nodes, in particular since the 3D geometry may offer an improved control of the short-channel effects through a better electrostatic control of the gate over the conduction channel, giving the possibility to achieve a higher $I_{ON}/I_{OFF}$ ratio, and providing an enhanced mobility due to the undoped channel. However, the FinFETs still need to reach a higher $I_{ON}$ to meet the technology requirements; for the enhancement of the device mobility without adding major process complexity, strain engineering techniques may be used [1,2].

This work is focused on the characterization of unstrained (standard) and strained SOI p-channel FinFETs at very low temperature operation in terms of short channel effects, analog operation parameters and low frequency noise. It is important to observe whether or not the strain-engineering is still useful for the p-channel devices at this cryogenic temperature.

## 2. Experimental

The investigated devices are p-channel tri-gate FinFETs processed in a 32 nm SOI technology. The gate oxide consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial $SiO_2$ resulting in an equivalent oxide thickness of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The devices have a fin width of 25 nm, fin height of 65 nm, 5 fins in parallel and a mask gate length ($L_G$) varying from 0.13 µm to 1 µm. The tested devices are p-channel FinFETs on standard SOI substrates (SOI) and on biaxial globally strained substrates sSOI combined with uniaxial local strain by CESL (Contact Etch Stop Layers) and using SEG (Selective Epitaxial Growth) in the drain and source regions (sSOI + CESL +SEG).

All measurements were performed directly at wafer-level using a Lakeshore TTP4 prober. Static measurements were performed using an HP4156B semiconductor parameter analyser. The transfer characteristics $I_D(V_{DS})$ were performed for different applied gate voltages $V_{GS}$ from 0.6 V up to 1 V. The saturation regime operation was investigated for all available gate lengths at room temperature, while at 10 K the measurements were focused only on three mask gate lengths of 0.13 µm, 0.25 µm and 0.7 µm.

The noise measurements have been made using two low noise DC voltage sources, an $I$ to $V$ converter and a low noise voltage amplifier. An HP3562 spectral analyser was used to obtain the noise spectral density $S_{VG}$ at the input of the device. The low frequency noise analysis was focused in linear operation only at 10 K operation on p and n-channel standard devices with mask gate length of 0.2 µm.

## 3. Results and Discussion

### A. *Saturation operation measurements*

Typical output transfer characteristics $I_D(V_{DS})$ for a standard and strained p-channel FinFET at room temperature and at 10 K operation for various gate lengths are shown in Fig. 1(a) and (b).

Reducing temperature leads to an increase of the saturation drain current $I_{Dsat}$ and a reduction of the saturation voltage $V_{Dsat.}$ However, one can observe that for a fixed gate length, the saturation drain current level is higher for the standard devices compared to the strained devices. This result could be surprising, but this trend may be related to the values of the mobility and of the threshold voltage, which were already extracted in [3] for the investigated devices.

The extracted values ($I_{Dsat}$ and $V_{Dsat}$) for the mask gate length of 1 µm are summarised in Table 1. The ratio $I_{Dsat}/V_{Dsat}^2$ for $L_G = 1$ µm is higher for the strained devices compared to the standard ones with a factor of 1.07 at room temperature and of about 1.24 at 10 K. As $I_{Dsat}/V_{Dsat}^2$ is directly proportional with the carrier mobility, this indicates that the mobility is slightly higher in strained devices compared to standard ones. Good agreement between the $I_{Dsat}/V_{Dsat}^2$ and the carrier mobility values could be observed (an increase of the low field mobility of about 1.08 at room temperature and of the effective mobility of about 1.21 at 10 K for the strained structure compared to the standard one).

**Table 1.** Summary of the extracted $I_{Dsat}$ and $V_{Dsat}$ *for* $L_G = 1$ µm; the values of the mobility are taken from [3]

| | T (K) | $I_{Dsat}$ (µA) | $V_{Dsat}$ (V) | $\mu$ (cm²/V/s) |
|---|---|---|---|---|
| **SOI** | 300 K | 44.68 | 0.65 | 124 |
| | 10 K | 60.97 | 0.57 | 218 |
| **sSOI+CESL+SEG** | 300 K | 37.33 | 0.57 | 134 |
| | 10 K | 60.38 | 0.51 | 264 |

The $I_{ON}$ currents, defined as $I_{ON} = I_{DS}$ @ $V_{DS} = V_{GS} = 1$ V are plotted in Fig. 2. A temperature reduction leads to an enhancement of the $I_{ON}$ current. This increase is more pronounced for long - channel transistors ($L_G = 1$µm): about 60% for strained devices and about 35 % for the standard ones, while for the short – channel devices ($L_G = 0.13$ µm) about 8% for strained devices and about 5 % for standard devices. This could be related to the edge effects, which may play a more important role in strained devices, in particular for the shortest channel lengths. One can note that at 10 K operation, the $I_{ON}$ current is almost the same for long-channel devices in both structures.

In subthreshold operation, the drain induced barrier lowering effect (DIBL) leads to enhanced source injection resulting in an increased leakage current. The DIBL effect is generally studied by the threshold voltage ($V_{TH}$) reduction by increasing the drain voltage ($V_{TH}(V_{DS}) = V_{TH} - \lambda \cdot V_{DS}$, where $\lambda$ is the DIBL parameter). As this short-channel effect results in a lowering of the source/substrate barrier by applying a high drain voltage, one can estimate the DIBL effect by using the following parameter: $DIBL = \left[\partial(\log I_{DS})/\partial V_{DS}\right]_{V_{GS}=const.}$. The *DIBL* and $\lambda$ parameters are linked by the subthreshold slope.

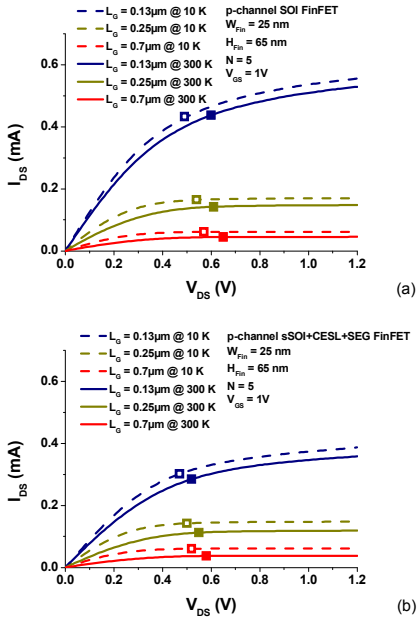


**Fig. 1.** Typical output characteristics $I_D(V_{DS})$ for standard a) and strained (b) p-channel FinFETs at 10 K and 300 K for various gate lengths. The square points represent the extracted $I_{Dsat}$ and $V_{Dsat}$ levels.

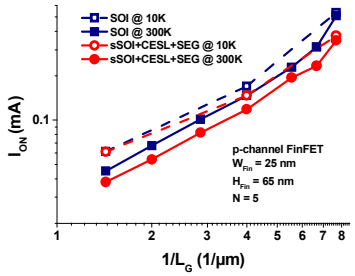


**Fig. 2.** $I_{ON}$ versus the mask gate length at 10 K and 300 K.

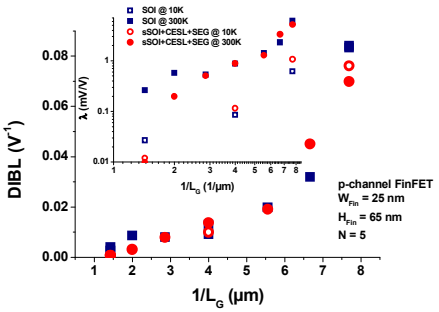


**Fig. 3.** The *DIBL* parameter versus the inverse of the mask gate length; in the inset are represented the calculated values of λ DIBL parameter.

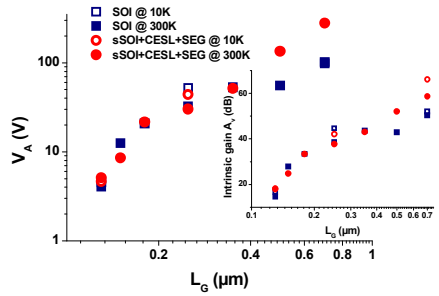


**Fig. 4.** The Early voltage $V_{EA}$ versus the mask gate length; in the inset are represented the intrinsic gain $A_V$ versus the mask gate length.

In Fig. 3 the extracted *DIBL* parameter at room temperature and at 10 K is plotted. For the shortest channel gate length (< 0.25 µm), an enhancement of the DIBL effect is highlighted by the deviation from the expected variation with the inverse of the channel length. This trend was already reported for advanced 50 nm nMOSFETs with 1.2 nm $SiO_2$ dielectric [6]. However, this increase is more pronounced for the standard devices than for the strain - engineered ones. Except for $L_G = 0.15$ µm, it can be observed that the strained devices suffer less from the DIBL effect compared to the unstrained ones.

The DIBL parameter $\lambda$, which can be calculated taking into account the extracted values for the subthreshold swing [3] and the *DIBL*, is represented in the inset of Fig. 3. The amelioration of the DIBL effect, which can be observed at 10 K operation, seems to be more significant for standard devices (reduction of $\lambda$ with a factor of about 10 for all investigated channel lengths) than for the strained ones (reduction of $\lambda$ with a factor of about 5). Because this parasitic effect is essentially electrostatic, one expects that the DIBL parameter should be nearly temperature insensitive [5]. However, reduction of the DIBL at lower temperatures was already reported for small geometry devices [6].

The obtained values of the absolute Early voltage $V_{EA}$ parameter, defined as $V_{EA} \cong I_{DS}/g_{DS}$, ($g_{DS}$ being the drain conductance measured in saturation at $V_{DS} = V_{GS} = 1$ V) for our devices are shown in Fig. 4. At room temperature operation, $V_{EA}$ is higher in strain-engineered devices compared to standard ones. This benefit is more important for long-channel devices than for short-channel devices: an increase with a factor of about 2.8 for $L_G = 0.7$ µm compared to a factor of about 1.3 for $L_G = 0.13$ µm can be observed. For $L_G < 0.5$ µm linear dependences of the $V_{EA}$ with the mask gate length can be observed, resulting in a ratio of about 200 V/µm for both structures. At cryogenic temperature operation, the same behaviour is observed: the benefit of using a strained channel is pronounced only for long-channel devices (with a factor of about 5 for $L_G = 0.7$ µm compared to a factor of about 1.1 for $L_G = 0.13$ µm). The operation at 10 K leads to an enhancement of the Early voltage for both structures.

Another common analog figure of merit is the transistor intrinsic gain $A_V$, defined as $A_V = V_{EA} \cdot g_m / I_{DS}$. Using the obtained values of $V_{EA}$, the intrinsic gain determined at 10 K and at 300 K is presented in the inset of Fig. 4 as a function of the gate length $L_G$. The obtained values are of the same order of magnitude as the ones already reported for a similar FinFET technology [7]. The intrinsic gain $A_V$ is higher for strain-engineered devices compared to the standard ones both at room temperature and 10 K. The benefit of using strained channels is more pronounced for long channel transistors ($A_V$ is about 8 dB higher for strained devices compared to unstrained ones for $L_G = 0.7$ µm) compared to short channel devices ($A_V$ is about 3.3 dB higher for strained devices compared to unstrained ones for $L_G = 0.13$ µm). The same trend is observed at 10 K operation: the increase of the intrinsic gain is about 14 dB for $L_G = 0.7$ µm compared to about 1.5 dB for $L_G = 0.13$ µm. The operation at 10 K leads to an enhancement of the intrinsic gain; this is more pronounced for long-channel devices.

### *B. Low frequency noise at 10 K*

In Fig. 5 is represented an example of the gate voltage noise spectral density at 10 K for a standard p-channel device. The total noise can be

perfectly modelled by considering three noise sources: white noise, *1/f* and Lorentzian noise (see equation in the inset of Fig. 5), and each contribution can be identified.

The extracted *1/f* noise level ($K_f$) variations with the applied gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$) are illustrated in Fig. 6 for unstrained p and n- channel devices with a mask gate length of 0.2 µm.

At 10 K operation, the extracted *1/f* noise level is found to be independent on the variations of the applied gate overdrive in moderate inversion. This suggests that carrier number fluctuations dominate the *1/f* noise [8] for both p and n-channel devices. The increase of the noise in strong inversion can be modelled by taking into account only parasitic access resistance contributions. The solid line in Fig. 6 represents the *1/f* noise model which takes into account carrier number fluctuation and parasitic access resistance contributions (see equation in the inset of Fig. 6).

In Table 2 are summarized the main extracted noise parameters. As expected, the flat-band noise level is lower in p-channel devices than in n-channel devices even at 10 K operation. The quality of the gate oxide interface was evidenced by the relatively small values of the oxide trap density $N_{it}$ deduced from the $1/f^{\gamma}$ noise contribution in flat-band operation.

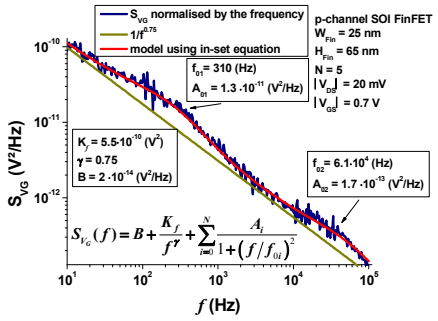


**Fig. 5.** Typical gate voltage noise spectral density for a standard device at 10 K operation.

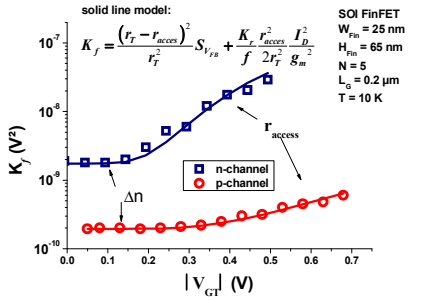


**Fig. 6.** The extracted *1/f* noise level $K_f$ versus the applied gate overdrive.

**Table 2.** Summary of the extracted noise parameters for standard devices at 10 K

| SOI structure T = 10 K $L_G$ =0.2 µm | $S_{VFB}\cdot10^{-10}$ ($V^2$/Hz) | γ | $N_{it}\cdot10^{17}$ ($cm^{-3}eV^{-1}$) | $K_r\cdot10^{-8}$ |
|---|---|---|---|---|
| **p-channel** | 2.9 | 0.75 | 57 | 0.55 |
| **n-channel** | 17.5 | 1 | 610 | 1500 |

## 4. Conclusions

The benefit of the use of strain engineering techniques is kept at very low temperatures for the p-channel FinFETs in terms of lower DIBL effect, enhanced Early voltage and intrinsic gain. This gain is more pronounced for the long-channel devices where the edge effects, which can play more in strained devices with channel length reduction, could be neglected. In contrast, the $I_{ON}$ current and the drift velocity are highest in standard devices. However, cryogenic operation at 10 K leads to an increase of the $I_{ON}$ for the strained devices, in particular for long-channel devices, for which the values in standard and strained devices have similar levels.

The carrier number fluctuations explain the *1/f* noise in weak inversion even at cryogenic temperature of 10 K. In strong inversion, the access resistance contribution prevails on the total *1/f* noise. The relatively small values of the oxide trap density highlight the quality of the gate stack deposition process.

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