DreamCAM: A FPGA-based platform for smart camera networks

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***Abstract*—The main challenges in smart camera networks come from the limited capacity of network communications. Indeed, wireless protocols such as the IEEE 802.15.4 protocol target low data rate, low power consumption and low cost wireless networking in order to fit the requirements of sensor networks.**

Since nodes more and more often integrate image sensors, network bandwidth has become a strong limiting factor in application deployment. This means that data must be processed at the node level before being sent on the network.

In this context, FPGA-based platforms, supporting massive data parallelism, offer large opportunities for on-board processing. We present in this paper our FPGA-based smart camera platform, called DreamCam, which is able to autonomously exchange processed information on an Ethernet network.

I. Introduction

On-board processing is key issue for smart camera platforms. Most existing platforms are based on GGP units [1], [2]. This kind of architecture offers high level programming and modern embedded processors provide good performances but cannot meet real-time processing constraints when image resolution increases. On the other side, FPGA-based architectures, offering more massive computing capability have been the subject of tremendous attention for implementing image processing applications on smart camera nodes [3], [4]. However, if the introduction of FPGAs can address some performance issues in smart camera networks, it introduces new challenges concerning node programmability, hardware abstraction, dynamic configuration and network management.

In [5], we proposed an hardware and software architecture for smart camera addressing the aforementioned issues. This paper aims at detailing first development of this ambitious proposal, giving insights into the final hardware. We implement a simplified version of the hardware architecture and we don't use full communication stack (applicative layer is not integrated). Nonetheless, we show how processed information - histograms here - can be exchange between two camera nodes using an ethernet connection.

II. Platform

The platform used is a FPGA-based smart camera developed at our institute and called DreamCam [6], Fig 1. The DreamCam platform is equipped by a 1.3 Mega-pixels active-pixel digital image sensor from E2V, supporting subsampling/binning and multi Region of Interests (ROIs). The FPGA is a Cyclone-III EP3C120 FPGA manufactured by Altera. This FPGA is connected to 6x1MBytes of SRAM memory blocks wherein each 1MB memory block has a private data and address buses (hence programmer may address six memories in parallel). The FPGA also embeds a CMOS driver to control the image sensor and a communication controller (USB or Giga-Ethernet).

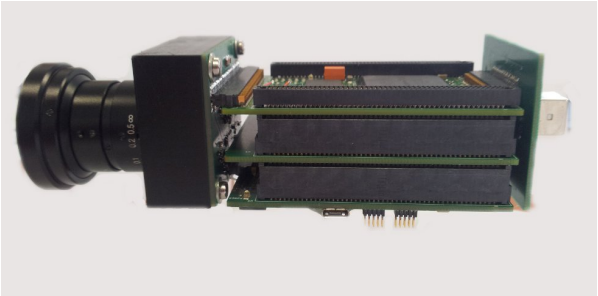

Fig. 1: Our smart camera system

III. Experiment

The proposed demonstration features two smart cameras exchanging information on an ethernet network, (see screenshot Fig 2.)

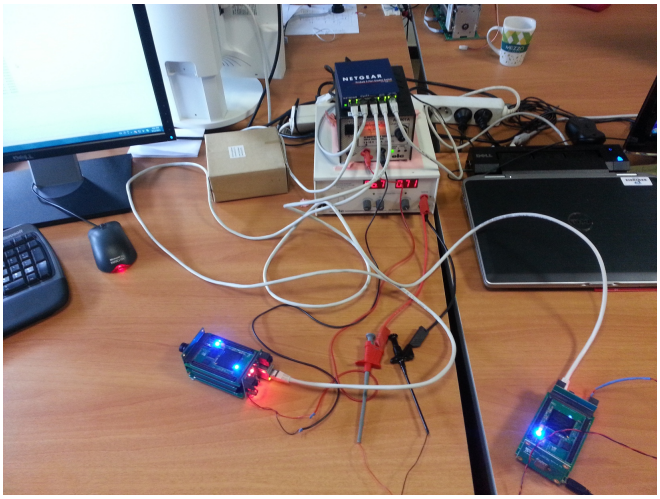

Fig. 2: Screenshot of the demonstration

The global system architecture is depicted in Figure 3. It includes two smart camera and a computer. The computer is used

to sniff Ethernet packet and check inter-node communication. In this application, each camera process input video stream on the fly (without frame buffering), calculates corresponding image histograms and send them to other cameras at the frame rate. This first simple application is the basis of a color-based object tracking in smart camera network [7].

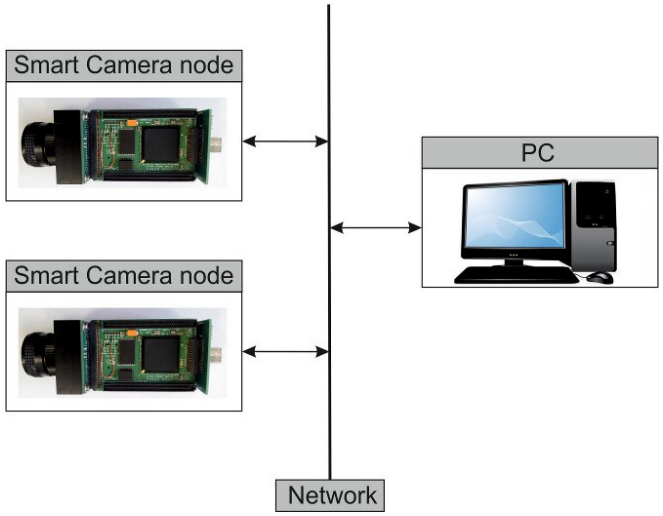

Fig. 3: Demonstration system architecture

Figure 4 shows the FPGA logical architecture within each camera. First component is an image sensor IP block which controls the E2V image sensor. Then, the flow of pixel is processed by an histogram hardware module which computes the image intensity distribution. Next component implemented is a softcore which controls image sensor configuration (resolution, frame rate, ROI). It is also in charge of network management. In the proposed application, each softcore has to manage a very simple kind of communication: send and receive image histogram data at the image sensor frame rate. Last component is an Ethernet controller IP which manage transport to physical layer, from UDP packet encapsulation to physical chip configuration (Marvell 88E1111). The Ethernet IP can be addressed by the softcore register to configure port, IP and MAC address.

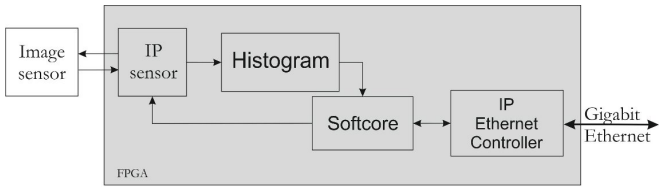

Fig. 4: Smart Camera implementation

Total resource allocation of this application only use 5% of logic elements but 45% of FPGA memory for a 1240×1080 resolution frame. The most memory consumer is the softcore component, requiring instruction and data memory space. In the case of a software application exceeds FPGA internal memory, we will shift softcore memory space to external memory blocks available in the camera. Table I shows detailed implementation results.

TABLE I: Hardware resource usage level

Operation	Logic Elements (%)	Memory bits (%)
Image sensor IP	271 (0,2%)	0
Softcore	2040 (1,7%)	1611264 (40,4%)
Processing	1250 (1,5%)	131072 (3,2%)
Ethernet IP	2643 (2,2%)	34944 (1%)
Total (usage level)	6204 (5,2%)	1777280 (44,6%)

IV. Conclusion

Objectives of this demonstration are twice. First, it exposes our theoretical architecture implemented in a real hardware platform and supporting a simple application. Then, we guarantee the good integration of our smart camera platform in a collaborative context through an Ethernet communication. Future development will focus on a wireless transceiver integration and a real distributed smart camera application such as multi-camera tracking.

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