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Development of an On-Chip Sensor for Substrate Coupling Study in Smart Power Mixed ICs

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***Abstract*— In order to merge low power and high voltage devices on the same chip at competitive cost, Smart Power integrated circuits (ICs) are extensively used. Electrical noise induced by power stage switching or external disturbances generates parasitic substrate currents, leading to a local shift of the substrate potential which can severely disturb low voltage circuits. Nowadays this is the major cause of failure of Smart Power ICs, inducing costly circuit redesign. Modern CAD tools cannot accurately simulate this injection of minority carriers in the substrate and their propagation in the substrate. In order to create a link between circuit design, modelling and implementation in innovative CAD tools there is a need to validate these models by measuring the high voltage perturbations that activate parasitic structures in the substrate directly on the chip. This paper presents an on-chip noise sensor dedicated to measurements of transient voltage fluctuations induced by high voltage activity and coupled by the substrate.**

Index Terms*— *on-chip sensor; Smart Power IC; substrate noise coupling; electromagnetic compatibility; substrate parasitic bipolar structures;

I. Introduction

Nowadays, many segments of microelectronics move towards monolithic system integration merging on the same IC (Smart power ICs) low voltage analog and/or digital parts with high voltage parts using power transistors.

Substrate coupling in Smart power ICs occurs when parasitic bipolar structures (with unpredictable size and location) are activated after an injection of current into the substrate due to internal switching activity or external noise coupling. When low power analog and digital applications are integrated with high voltage (HV) devices on the same IC, these side effects become very important and hurtful to the circuit operation. In turn, designers have to rely on empirical basis for the design strategy, which is expensive and time consuming. Today, when simulating circuits with HV-MOSFETS devices, their specific SPICE models are used in every CAD tool but these models do not address generation of these parasitic substrate currents of minority and majority carriers.

AUTOMICS project [1] aims at providing SPICE models, once implemented in CAD tools, will allow optimizing high voltage and high current capability, EMI-EMC performance with respect to substrate parasitic robustness. Moreover, AUTOMICS should considerably improve the design methodology by developing efficient CAD models of parasitic structures activated by HV functions integrated in automotive Smart Power ICs [1]. In order to detect parasitic bipolar structures activation and the induced substrate coupling effect, some measurements have to be done directly on internal sensitive nodes using an on-chip sensor and thereby validate the proposed Spice models of the parasitic bipolar junction.

This paper aims at presenting an on-chip sensor dedicated to the characterization of transient voltage fluctuations due to parasitic structures activation in real application conditions. Section II briefly presents substrate-coupling issues in Smart Power ICs. Section III introduces the principles and structure of the proposed on-chip sensor. Section IV presents experimental measurements of substrate coupling effects on sensitive nodes in a Smart Power IC.

II. Substrate Coupling Issues In Smart Power ICs

In Smart Power ICs, sources of substrate coupling are parasitic NPN and PNP bipolar transistors (Fig. 1) activated by ‘below-ground’ or ‘above-supply’ working conditions of High Voltage-MOSFETS at the circuit output [2], [3]. These parasitic bipolar transistors can be activated during normal circuit operation by the switching on/off of inductive loads. They can be also activated during usual automotive chip testing (EMI-EMC tests), by external electromagnetic perturbations or electrostatic discharges.

Two physical mechanisms are behind this type of coupling as seen in Fig.1. The first one is the injection of holes (majority carriers) into the p substrate. This happens when the power output of the circuit, the drain of the power PMOS, exceeds the power supply voltage VDD, activating a parasitic PNP transistor. This in turn leads to a local voltage shift of the substrate potential in the neighbour sensitive electronic blocks. The second physical mechanism is the injection of electrons (minority carriers) into the p substrate when the drain of the power NMOS, at the power output of the circuit, is below the ground potential and thus activates a parasitic NPN transistor. These minority carriers injected into the substrate can be collected by every surrounding NTUB and causing a voltage fluctuation of the N-WELL of a surrounding sensitive blocks and cause its dysfunction.

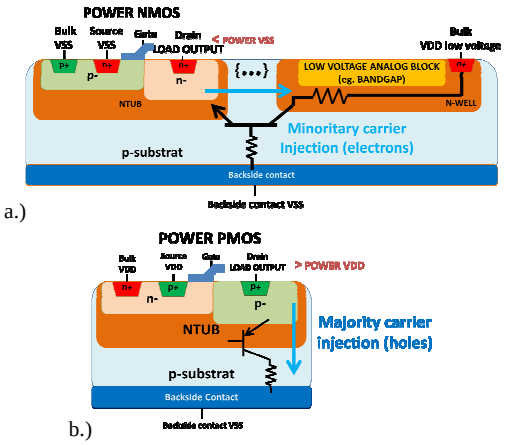


Fig. 1 Wafer cross section of power a.)NMOS b.)PMOS

III. On-Chip Sensor : Principle & Structure

The on-chip sensor was developed to address signal and power integrity issues at circuit level, like an on-chip oscilloscope. Based on a sequential equivalent-time sampling method, the sensor exploits the benefits of subsampling techniques, which ensure a very high virtual sample rate without severe constraints on hardware bandwidth like in high speed sampling circuits. The signal to measure has to be repeatable and synchronized with the sampling command of the sensor [4], [5]. The on-chip sensor has its dedicated 5V power supply as a critical and crucial requirement to avoid any external disturbances and noise produced of other blocks of the circuit architecture description.

The on-chip sensor architecture, presented on Fig. 2., is composed of an analog/digital core cell used to control 8 sensor probes placed close to nodes monitored during the test [4], [5]. Each probe is composed of one Sample&Hold (S&H) cell, followed by a folded cascode operational amplifier in buffer configuration. The sensor core integrates an 8x1 analog multiplexer (to externally select one of the 8 probes), a folded cascode operational amplifier in the buffer configuration and a delay cell used to control the acquisition time. The delay cell, used for subsampling method, provides a programmable sampling command with a variable delay added to the falling edge of the synchronization signal by a delay ΔTi [4], [5]. The principle of subsampling method and the signal reconstruction are described in Fig. 3, . The control of the delay is done by two external analog signals: the V_{range} signal shapes the time range for the delay, while the V_{analog} signal ensures the delay fine control. The delay law varies between 50ns and 1200ns.

The input voltage range of a nominal (without attenuator) is between 0.6 V and 4 V. For high voltage measurements an attenuator is placed at the input of the probe. To ensure low intrusion during voltage measurements the S&H cell (with the optional attenuator) form a high impedance probe with input capacitance of 25fF with a bandwidth of 1.7GHz.

Due to imperfections and mismatch in the implementation of the on-chip sensor, calibration procedures have to be performed. The sensor imperfections can be easily compensated by post-processing from the transfer function characterization.

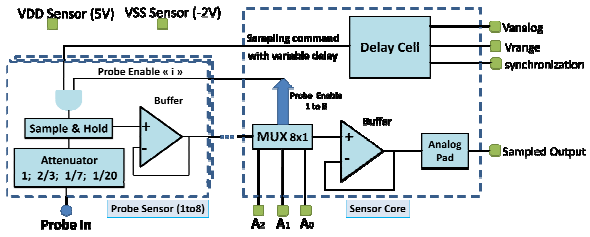


Fig. 2 Sensor-on chip architecture

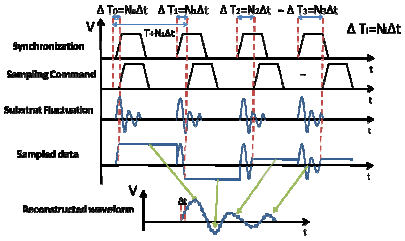


Fig. 3 The subsampling principle and the reconstruction of the temporal

IV. Study Of Substrate Coupling Issues In Smart Power Circuits

The on-chip sensor is now used to study substrate coupling effect in Smart Power IC. The proposed study focuses on typical sensible devices and structures used in 0.35µm AMS High Voltage CMOS technology using the H35 20V design kit with 3 metal layers. This technology permits to isolate low voltage transistors, with a buried N-WELL, from high voltage part of the circuit. The sensor was entirely designed with 5V isolated MOS transistors. sensor was entirely designed with 5V isolated MOS transistors. The entire test circuit (the on chip sensor, one DC-DC converter and two bandgaps are on the same die) is mounted in a 32 QFN package, and is soldered on a four-layer EMC test board with all surrounding electronics and I/O connections.

Sensor measurements aim at determining the amount of coupling between a power part (the output stage of a DC-DC converter) and a low voltage analog part (bandgap reference voltage). Two sensor probes have been placed on the DC-DC converter output in order to measure its transient voltage profile. Three other sensor probes are placed on the bandgap sensitive nodes, in order to measure the impact of substrate coupling on this structure. TABLE I. gives the characteristics of these sensors. In order to ensure that the sensor does not affect the bandgap function, two bandgap devices are present in the test chip: one with the sensor probes at their critical nodes and another without. No major differences are observed between both bandgap.

Table I

Probes S4, S5, S6, S7 And S8 Characteristics

Probe No.	**Probe Location**	**Input signal range**	**Attenuation ratio**
Probe S4	DC-DC output	4V to 60V	1/7
Probe S5	DC-DC output	4V to 60V	1/7
Probe S6	Bandgap N-WELL	0.6V to 4V	1/1
Probe S7	Bandgap output	0.6V to 4V	1/1
Probe S8	Bandgap VDD	0.6V to 4V	1/1

Two case studies are intended in this work. The first one is done during nominal circuit operation and consists in observing the coupling between a power device (DC-DC converter) and a low voltage analog block (1.23V bandgap reference voltage circuit, later bandgap). The second experiment, done by inducing an external electromagnetic perturbation, has the purpose to measure the coupling and the impact of the current injection on the output of the power device (DC-DC converter) to the low voltage block (bandgap).

A. *Coupling between power and low voltage analog block*

The objective of the experiment presented on Fig. 4 is to observe disturbances induced by the switching of one DC-DC converter on a bandgap circuit. Measurements will be done directly on the DC-DC converter outputs (sensor probes S4, S5) and also directly on the bandgap circuit sensitive nodes as its N-WELL, its output, and on its low voltage power supply (sensor probes S6, S7 and S8 respectively).

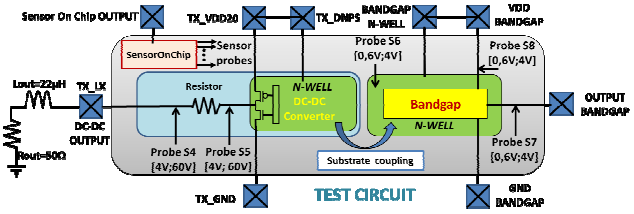


Fig. 4 Coupling between power and low voltage analog blocks

During DC-DC switching operation, on-chip sensor measurements, presented on Fig. 5, shows that some noise appears on the bandgap sensitive nodes. The noise amplitude is linked to the DC-DC converter power supply voltage (TX_VDD20) and the switching current (related to the load resistance and inductance). Due to the high temporal resolution of the on-chip sensor measurements (in comparison to oscilloscope measurements), the observed voltage fluctuations on the bandgap sensitive nodes leads us to a better understanding of the coupling mechanism present in Smart Power ICs.

The voltage overshot above the high voltage power supply, observed on the rising edge of the DC-DC converter output signal, more precisely on the drain of the conducting output power PMOS. This effect is the source of the activation of the parasitic PNP transistor leading to a local positive voltage shift of the substrate. Thus surrounding bandgap N-WELL has also a positive voltage shift relative to this voltage shift. As a consequence, bandgap power supply and its output have the same initial signal shape of this perturbation. The residual following fluctuations are caused by the resonance of the substrate RLC network. The bandgap output signal is not perturbed by these residual fluctuations, as expected.

On the other side, when a falling edge occurs at the DC-DC converter output (probes S4 & S5 saturates below 0,4V), the drain of the conducting output power NMOS have a similar below ground voltage overshot. This effect leads to the activation of the parasitic NPN transistor and is the source of a local negative voltage shift of the substrate potential. Surrounding bandgap N-WELL collects the substrate current and has also a negative voltage shift. Thus, bandgap power supply and its output have the same initial signal shape of this perturbation and the residual following fluctuations are also caused by the resonance of the substrate RLC network. The bandgap output signal has been perturbed also by these residual fluctuations, but in a much less amount.

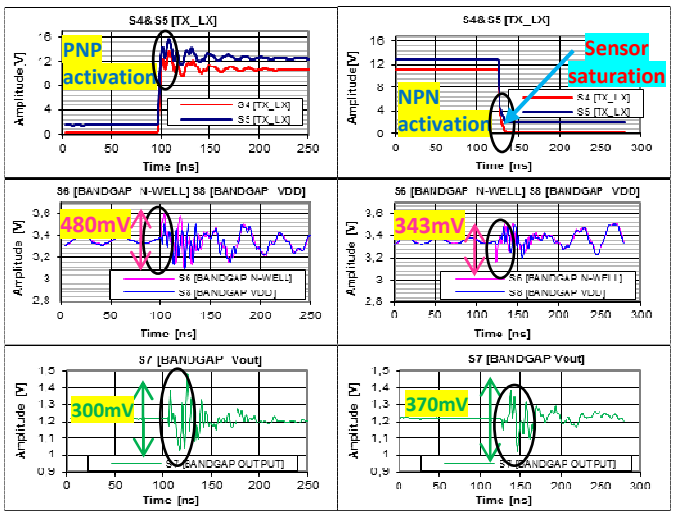


Fig. 5 DC-DC output effects on Bandgap power supply and output (left colon: rising edge; right colon: falling edge)

B. *Influence of an EMI injected on DC-DC output stage on bandgap*

In the experience presented on Fig. 6, the output of the DC-DC converter (TX_LX pin) harmonic disturbances are coupled in order to simulate the coupling of an electromagnetic interference test (EMI injection test). In real conditions the potentially mechanically large load or long cables connected to the output of the DC-DC converter may couple a significant amount of electromagnetic disturbance.

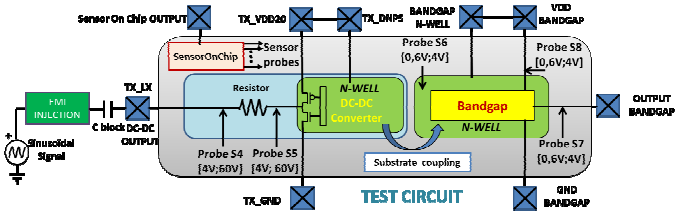


Fig. 6 Description of the conducted EMI test

For the EMI injection test, the DC-DC converter power supply voltage (TX_VDD20) is set to 12 V without any resistive load on its output. The on-chip measurements are performed on the same nodes as in the previous test.

The test has been performed with various disturbance amplitudes and at different frequencies. Only measurements with frequency of 10MHz will be presented in this paper, see Fig. 7, as they show very well the nature of the coupling between the DC-DC converter output and the bandgap sensitive node. This test highlights the role of the substrate coupling mechanism and especially the role of the PN junction between the drain of the PMOS device of the DC-DC converter output and the surrounding N-WELL. Depending on

the amplitude of the disturbance, the nature of the coupling may change as we can see on Fig. 7.

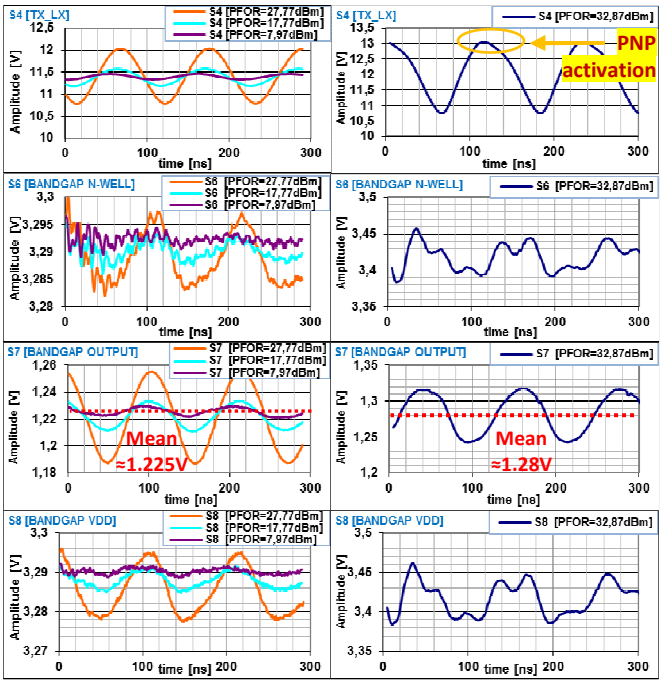


Fig. 7 EMI test on chip measurements of in presence of a 10 MHz disturbance with different Power Forward values (PFOR=7,97dBm;17,77dBm;27,77dBm;22,87dBm;32,77dBm;36,57dBm)

From the previous measurement results the effects on the signals on the DC-DC converter output (TX_LX) and on bandgap internal signals are quite complicated to be fully described as they are dependent on the EMI amplitude and frequency. Nevertheless some interesting general conclusions can be drawn and two issues can be determined.

For small voltage fluctuations amplitude coupled on TX_LX node, below a threshold voltage $V_{treshold}$ above the power supply voltage TX_VDD20, the measured signals are not distorted. It can be noticed that a part of this disturbance is coupled on the internal signals of the bandgap and has the same shape as the input disturbance and the amplitude and phase of these internal bandgap signals are related to the input frequency. By doubling the disturbance amplitude the induced voltage amplitude, induced within the bandgap is also doubled, showing the linearity of the coupling effects. These effects can be associated to parasitic RLC network of the substrate and/or a coupling by the power distribution network and can't be caused by a substrate coupling mechanism with parasitic bipolar transistor activation as described before. Nevertheless, the impact on the integrity of the output voltage of the bandgap remains weak or moderate.

On the other side, when voltage fluctuations amplitude coupled on TX_LX node are "large enough" and exceeds a threshold voltage $V_{treshold}$ above the power supply voltage TX_VDD20 (nearly equal to the threshold voltage of a PN junction) the measured signals are distorted. This distortion of coupled signals on the bandgap sensitive nodes is due to the activation of the parasitic PNP transistor caused by an above power supply condition on the drain of the PMOS transistor of the DC-DC converter power output. The surrounding N-WELL of the bandgap device fluctuates too, but the shape of the signal is distorted clearly showing that the current within the substrate triggers the activation of the parasitic PN junctions. The bandgap power supply and its output fluctuates too and their signal shape showing a non-linear regime of this type of coupling. As a result, the integrity of the output voltage of the bandgap gives voltage fluctuations of several tens up to hundreds of millivolts and generation of voltage offsets (as seen on Fig. 7 the observed voltage offset at the bandgap output is about +55mV).

V. Conclusions

This paper presents an on-chip sensor dedicated to the analysis of substrate coupling issues in Smart Power ICs. On-chip sensor offers a more accurate evaluation of these substrate coupling issues than a simple oscilloscope measurements without the possibility to scan IC internal nodes. This on-chip sensor has the advantage to perform low intrusion voltage measurements with high temporal resolution, have a large bandwidth obtained by subsampling technique and due to its separated power supply and its closeness to the measured point any additional noise coupling from other circuit blocks is avoided.

The first experiment clearly shows the effect of substrate coupling mechanism in Smart Power Ics when the DC-DC converter output is switching causing a coupling on bandgap critical nodes. Both coupling mechanism are observed and the activation of the parasitic PNP and NPN transistor are demonstrated. The amount of substrate coupling is linked to the DC-DC converter power supply voltage and its switching current. With the second experiment, the EMI injection tests on the output of the DC-DC converter, the analysis of the results confirms the major importance of the parasitic PN junction activation in the coupling between the DC-DC converter output and a neighbour bandgap reference voltage.

In the future, these on-chip measurements can be used to validate the new SPICE models of Smart power ICs developed within the AUTOMICS project.

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References

[1] (2014) The AUTOMICS web site [Online]. Available: https://www.automics.eu/

[2] F. Lo Conte, J.-M. Sallese, M. Pastre, F. Krummenacher and M. Kayal. "A circuit-level substrate current model for smart-power ICs, IEEE Transactions on Power Electronics", vol. 25, num. 9, p.2433-2439, 2010.

[3] M. Schenkel, "Substrate Curent Effects in Smart Power ICs", Ph.D thesis, 2003, Technische Wissenschaften ETH Zürich, Nr. 14925, Available from: e-collection.library.ethz.ch, pp 1-24.

[4] S. Ben Dhia, "Une nouvelle methodologie de caracterisation de l'integrite du signal en cmos submicronique profond." Ph.D thesis, 2003, Institut national des sciences appliquées de Toulouse.

[5] S. Ben Dhia, A; Boyer, "On-Chip Noise Sensor for Integrated Circuit Susceptibility Investigations" IEEE transactions on instrumentation and measurement, vol. 61, no. 3, march 2012.