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SiGe:C BiCMOS COMPONENTS AND INTEGRATION SOLUTIONS FOR F-BAND RADAR FRONTENDS

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INTRODUCTION

Remote radar sensing and imaging systems are continually evolving and move at a rapid pace toward high millimeter-wave and terahertz frequencies in order to achieve superior image resolution together with enhanced detection capabilities [1]. High-precision imaging sensors for smart robots, security sensors for detection of concealed objects or Earth remote sensing are among many applications that can benefit from the nature of this valuable part of the frequency spectrum. Considering the growing requirements for low cost and compactness of such systems, availability of reliable high performance and inexpensive millimeter-wave building blocks becomes more and more important. Favourably to the latter evolution, recent progress in SiGe BiCMOS technologies has shown that very fast Heterojunction Bipolar Transistor (HBTs) with f_{max} of 500 GHz and above are possible even at more relaxed lithographic resolution compared to similarly performing RF-CMOS counterparts [2]-[4]. This progress together with the availability of high-performance CMOS modules, advanced micromachining and wafer-level packaging techniques make SiGe BiCMOS very attractive for future radar and imaging systems that will benefit not only from the inherent physical properties of millimeter-waves but also from the high degree of integration and cost effectiveness that can be achieved today.

This contribution presents major intermediate results achieved towards the realizations of a 140 GHz Frequency-Modulated Continuous-Wave (FMCW) Multiple-Input Multiple-Output (MIMO) imaging system for screening applications, obtained within the FP7 IP NANOTEC. Design and measured performance of key millimeter-wave building blocks such as F-band frequency multipliers, LNAs, PAs, a differential MEMS SPDT switch and an on-chip high-voltage generator will be introduced. All ICs were implemented in an 0.13µm SiGe:C BiCMOS process provided by IHP GmbH. Different approaches to frequency multiplication, specifically a cascade of Gilbert cells or push-push multipliers will be discussed. The design of a state-of-the-art SiGe:C BiCMOS LNA featuring 4 dB noise figure and 20 dB gain at 110 GHz will be presented in detail. Use of on-chip and off-chip antennas will be discussed together with engineering of compensated bondwire chip-to-antenna interconnects for millimeter-wave applications. Two different bondwire compensating structures implemented on RO3003 substrate will be shown. Afterwards, complete TX/RX radar modules with on-chip and off-chip antennas will be presented and demonstrated in an experimental radar scenario. It will be shown that the radar front-end with the on-chip antennas can provide EIRP of up to 15 dBm and a system bandwidth of 56.8 GHz from 104.4 GHz to 161.2 GHz, which provides milimmeter-range resolution. On the other hand, the radar front-end with the off-chip antennas and compensated differential bondwire interconnects achieves 9 GHz bandwidth and maximum EIRP power of 13 dBm. Experimental measurement results suggest that a compensated bondwire interconnect with total length of 0.8 mm can achieve the above bandwidth and minimum insertion loss of 0.2 dB. The latter demonstrates that the well-established wire-bonding techniques are still an attractive solution for millimeter-wave interconnects even beyond 100 GHz.

KEY RADAR FRONTEND COMPONENTS

Frequency Multipliers for TX and RX ICs

Certainly the most challenging task in millimeter-wave and terahertz systems is the design of a signal source that fulfils specified requirements and enables the integration with the rest of the system into a single chip. For such purpose, frequency conversion strategies that rely on a low-frequency signal source in combination with frequency multipliers are often used. This technique has also been adopted to the F-band MIMO radar that is under development. Two different approaches to multiplication by eight have been investigated and are described hereafter.

The first approach is based on a cascade of three Gilbert cells, each one connected as a squarer [5]. Since the double-balanced Gilbert cell requires differential signal excitation, the single-ended input signal that is to be multiplied is first fed to an active balun followed by a differential limiting amplifier. The latter is achieved using a common-emitter/common collector active balun followed by a differential cascode amplifier. The multiplied balanced output signal at 140 GHz is assured by a differential cascode PA with a floating base designed to provide high common mode suppression. A schematic of the overall multiplying chain together with the active balun and amplifying stages is depicted in Fig. 1a. For simplicity, current mirror based biasing networks of individual stages are omitted. A photograph of the realized F-band frequency multiplier, integrated into a receiver (RX) IC is shown in Fig. 1b. Single-ended on-wafer measurements of a stand-alone multiplier were carried out with the help of a spectrum analyzer equipped with a harmonic mixer to extend the range to the F-band. Single-ended measurement results of three different samples are plotted in Fig. 1c. It can be seen that a 3-dB bandwidth of up to 20 GHz and maximum output power of 3 dBm (6 dBm differential) can be achieved. Suppression of the undesired harmonics is better than 25 dBc. The frequency multiplier consumes 186 mW.

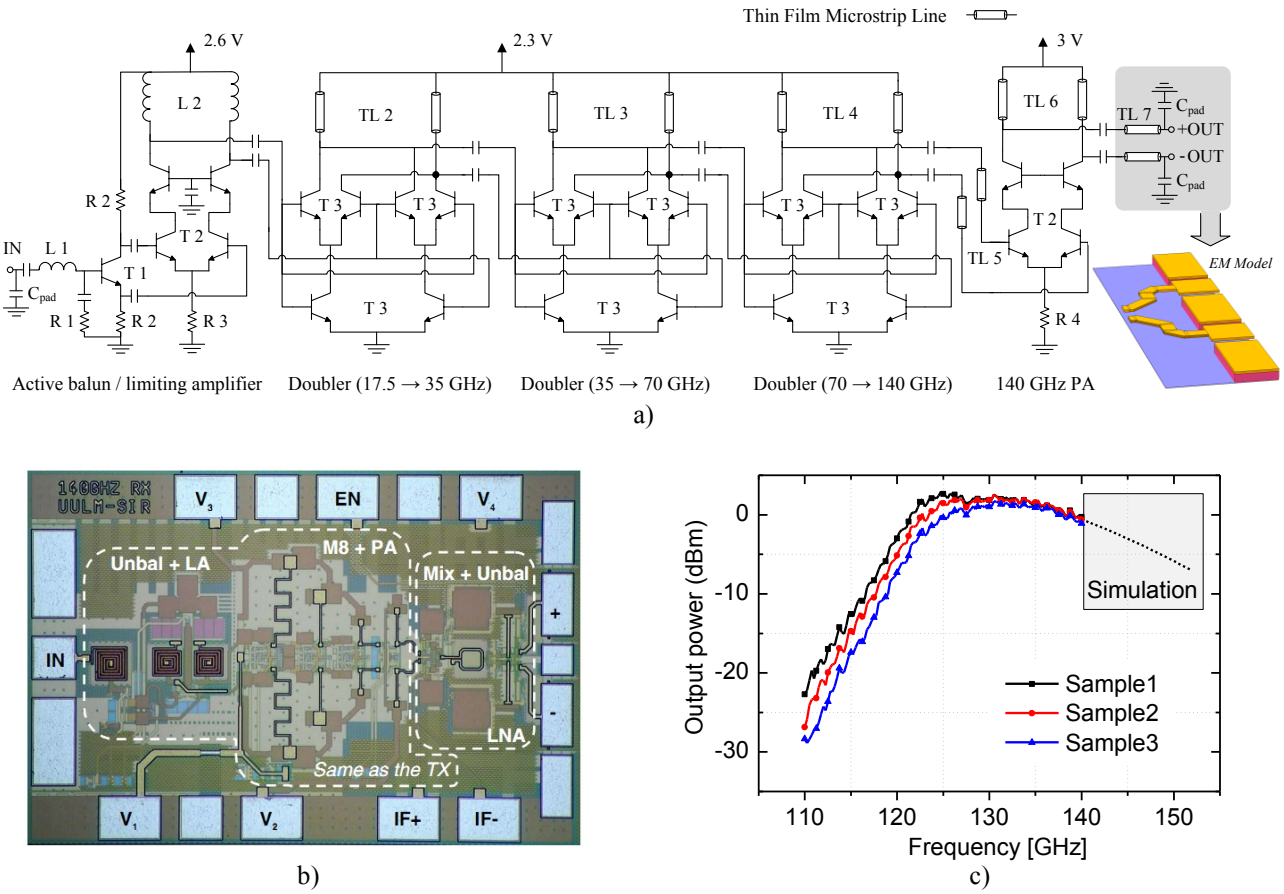


Fig. 1. Simplified schematic of the Gilbert cell based multiplier by eight (a) and a photograph of the realized RX IC that deploys the same multiplier (b). On-wafer measurement results of three standalone ICs are shown as well (c) [5].

The second approach to the multiplication by eight is based on a cascade of three push-push multipliers by two [6]. Push-push multipliers also require a differential input. However, they can only provide a single-ended output. As a result, baluns need to be used to feed the balanced input of the subsequent push-push stage. Compared to the Gilbert cell approach, push-push multipliers offer better balanced output signal. A simplified schematic of a single push-push multiplying cell is depicted in Fig. 2a. The input active balun and the output buffer stage are similar to those used in the Gilbert cell based multiplier (common-emitter/common-collector balun and a differential cascode as an output buffer stage as in Fig. 1a). Q1 and Q2 form the push-push pair, which is biased in class B mode for a maximum conversion

gain. A common-base amplifier made of Q3 is inserted to increase the conversion gain. C1 and C2 are used for inter-stage matching. For each doubler stage, a well-balanced differential input is critical for high conversion gain and low output harmonics. Unlike conventional push-push, a transformer is used to generate the differential output signal for the following stage. The transformer acts also as a resonant load enhancing the gain at the desired frequency while suppressing the undesired harmonics. Compared with transmission line-based balun designs, the transformer solution has a smaller size, a better output balance and comparable coupling loss. Another advantage of using a transformer is that DC feeding to the amplifier is possible through the primary coil, which is difficult for baluns such as the Marchand balun. A photograph of a realized transmit (TX) IC based on the push-push multiplier with an on-chip antenna is shown in Fig. 2c. Since the measurement setup was limited only to the F-band, the output power above 140 GHz was impossible to determine. However, considering the measured centre frequency of 137 GHz (maximum power of 5.4 dBm) and the lower 3-dB cut-off at 110 GHz, the bandwidth is expected to be above 30 GHz [6]. Suppression of the undesired harmonics is better than 38 dBc. The module has a power consumption of 170 mW.

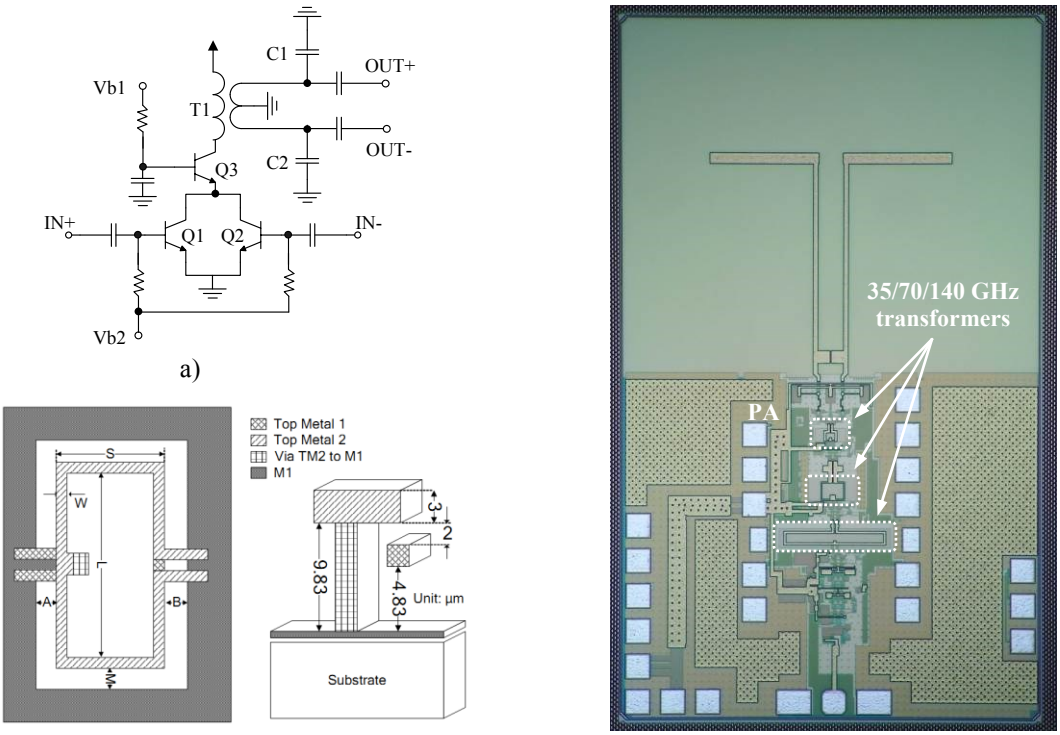


Fig. 2. A schematic of a single push-push multiplying cell (a) and a layout with a cross-section of the transformer (b). A chip photograph of the TX IC that uses the push-push multiplier by eight is depicted as well (c) [6].

Low Noise Amplifier

To demonstrate the increasing competitiveness of the SiGe BiCMOS technology against III-IV technologies, a 110 GHz LNA has been designed [7]. The LNA consist of two cascode stages. Fig. 3a shows a simplified schematic of the first stage. The second stage is identical to the first stage, except for larger transistor dimensions, and consequently modified transmission line lengths. Large resistors are used to connect the bias nodes to a current mirror that biases both stages. The reactances for the matching networks are implemented using Thin Film Microstrip Lines (TFMLs), with the topmost layer used as the signal line and the bottom layer as the ground plane. In this configuration, the dielectric (SiO_2) height between the top-metal and the bottom-metal equals 9.83 µm.

The size of the first stage transistors is scaled to achieve optimum noise and power matching. Devices with five fingers were chosen as an optimum, providing 3 dB minimum noise figure and 10 dB maximum available gain. The second stage uses eight fingers for higher gain. Furthermore, inductive emitter degeneration is utilized by including a 33 µm line between the emitter and the ground for simultaneous power and noise matching, by increasing the real part of the input impedance of the amplifier. The influence of the parasitic via inductance at critical nodes of the LNA was carefully analyzed using the EM simulator Sonnet. Two of these critical circuit nodes are depicted in Fig. 3a, namely the common-base termination and top- to bottom-metal via interconnects. A substantial influence on the circuit performance was observed as the base inductance increases from 0 to 30 pH, which increases the gain from 18 dB to 28 dB. Clearly, accurate modeling of the common-base termination is crucial, as the large parasitic inductance will lead to peaking and potential instabilities. Via interconnects also reduce the operating frequency of the amplifier by approximately 10% [7].

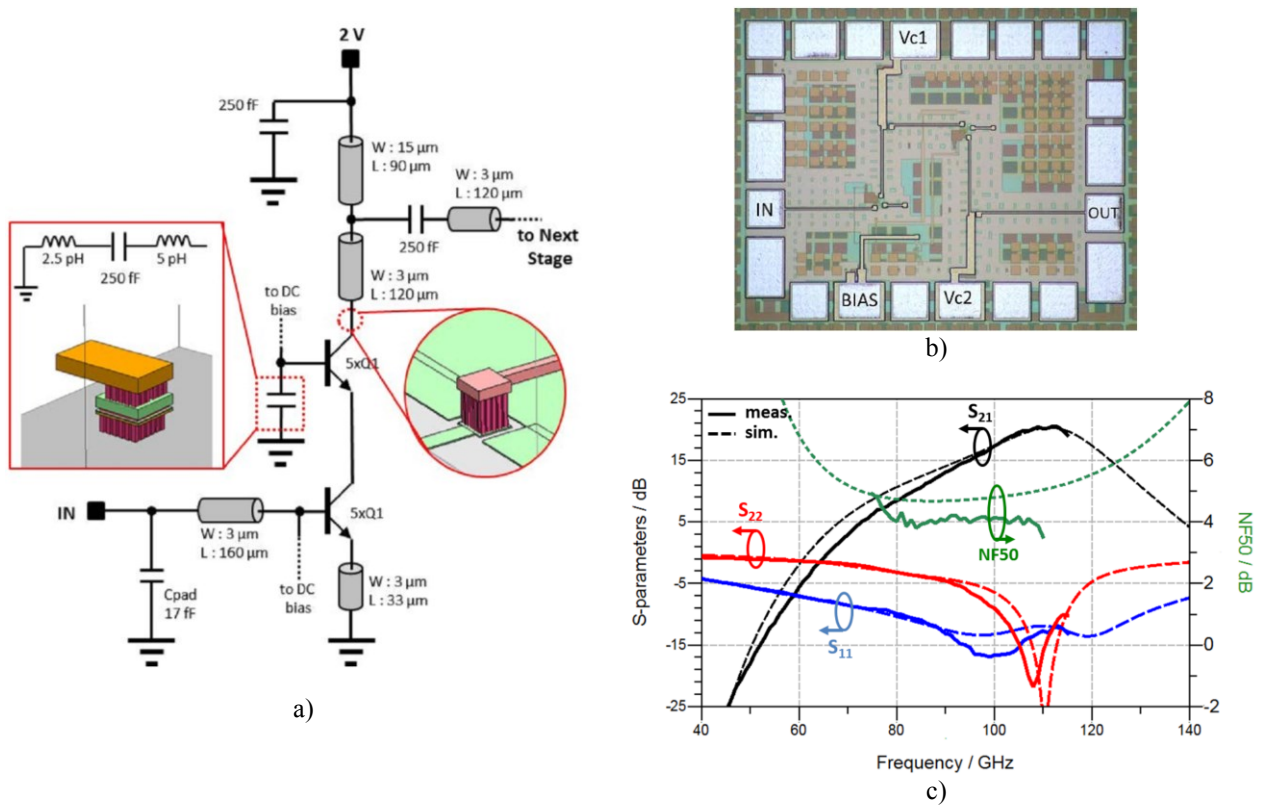


Fig. 3. A simplified schematic of the first LNA's stage (a), chip photograph of the fabricated LNA (b) and S-parameter with noise figure measurement results (c). Noise characterization was carried out in two different labs [7].

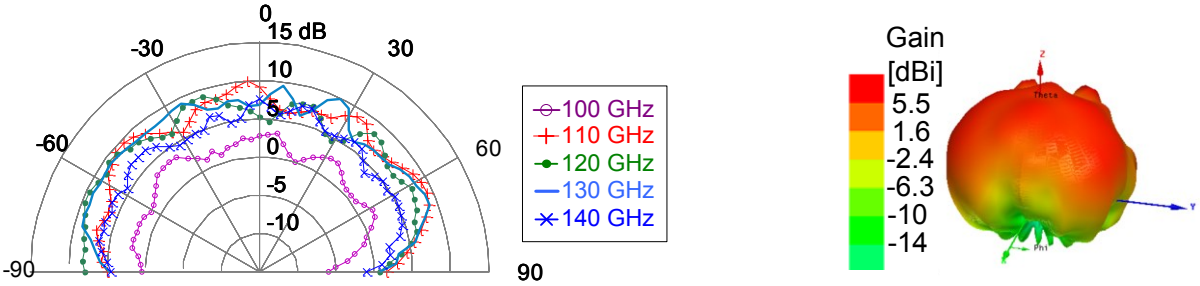
The chip photograph of the fabricated LNA is shown in Fig. 3b. The IC occupies an area of 760 µm x 540 µm. The circuit consumes 17 mW DC power from a 1.9 V source. The measurement and simulation results are presented in Fig. 3c. An excellent agreement can be seen, with a peak gain of 20.5 dB at 110 GHz and a 3-dB bandwidth of 100 to 120 GHz. The measured input and output return losses are better than 10 dB from 100 to 115 GHz. The simulated input 1-dB compression point of the LNA equals -24 dBm. The noise figure measurements are performed in two different institutes using independent measurement setups, both measurements are presented in Fig. 3c. The measured NF varies from 4 to 5 dB from 80 to 95 GHz, and remains on average around 4 dB from 95 GHz up to 110 GHz (the spike at 109 GHz is neglected). As it can be seen, the measured NF is in general lower than the simulated value. However, this discrepancy between measurement and simulation is not completely unexpected, as the HBT noise models are conservative. On the other hand, it should be kept in mind that a certain amount of measurement uncertainty (e.g. ±0.25 dB) is involved in case of NF measurements at such high frequencies.

Antennas and Integration Solutions

On-chip antennas fully integrated in standard BiCMOS processes become a reality in emerging millimeter-wave and THz imaging and radar systems [8]-[12]. This success is possible thanks to fast and accurate EM computational methods and advanced wafer processing techniques that allow localized backside wafer etching or precise wafer thinning to reduce losses in low-resistivity silicon substrates [11], [13]. Although fully integrated on-chip antennas significantly facilitate packaging and offer good radiation properties already today, the relatively large area they occupy (half wavelength in the air at 100 GHz is approximately one and half millimeter) may still be prohibitive for certain low-cost millimeter-wave imaging and radar systems deploying a large number of TX/RX channels. Moreover, to achieve good radiation properties, the space surrounding the on-chip radiating elements shouldn't contain any metal fillers, which is often incompatible with standard high-volume integration processes that require specified metal densities across all layers to achieve high yield. Off-chip antennas, on the other hand, offer ease of manufacturing at lower costs and superior performance namely in terms of radiation efficiency and bandwidth compared to their on-chip counterparts [14]. At the same time, bondwire interconnection techniques are widespread and very popular due to the rather simple technology involved. Performance degradation of chip-to-antenna interconnects at higher frequencies has been, however, identified as one of the key challenges due to reactance introduced by the bondwire, which in turn narrows down the usable bandwidth and introduces losses. Nonetheless, several studies have shown that bondwire interconnects with excellent properties in the millimeter-wave range are possible and reproducible [15]-[17]. Flip-chip interconnects would be another alternative, however, the overall complexity of the mounting process and other inherent drawbacks of this technique such as dielectric detuning by the opposite substrate [18], [19], lack of direct visual control or worse heat sinking make this solution less attractive for millimeter-wave interconnects. As a result, bondwire

interconnects are in certain systems inevitable and therefore need to be carefully assessed. In this work, both solutions based on on-chip and off-chip antennas were investigated and are described hereafter.

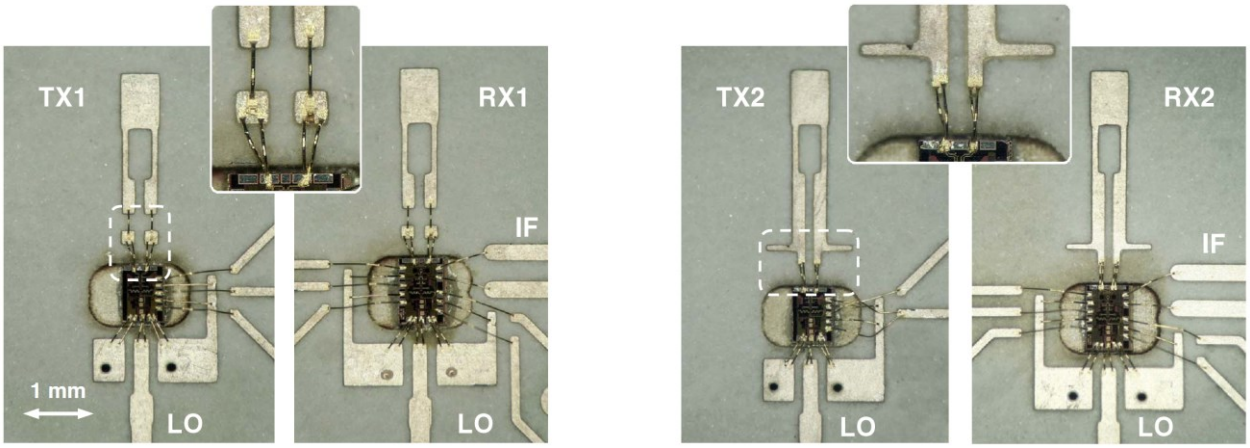
Wideband dipole on-chip antennas for TX and RX ICs with the push-push frequency multipliers have been implemented on a low-resistivity substrate [11]. Given the substrate resistivity of 50 Ωcm and the relative dielectric constant of 11.9, the substrate thickness of 150 µm was chosen for best reflection at 140 GHz, which is one of the wafer thickness options provided by the foundry. A photograph of the realized antenna integrated together with the push-push TX is shown in Fig. 2c. As a backside reflector, an aluminium backplane that serves as a chip carrier is used. The undesired radiation modes were controlled by front-side metal patterns. The simulated antenna gain is about 3 to 4 dBi from 120 to 140 GHz. The antenna gain was characterized by mounting the TX chip on a rotational platform in a microwave absorber chamber, and using a horn antenna with known gain to detect the directional radiated power from the on-chip antenna. The antenna gain was extracted by taking the received power, horn antenna gain, the multiplier output power and the path loss into account. Due to instrument limitations, the radiation pattern was only characterized up to 140 GHz. The radiation patterns at different frequencies are plotted in Fig. 4a, showing that the on-chip antenna has a measured gain of 4 to 9 dBi from 105 to 140 GHz [11].



a) b)

Fig. 4. Measured antenna gain at different frequencies at φ=90° (a) and the simulated radiation pattern at 140 GHz (b).

The possibility to use off-chip antennas and to compensate bondwire interconnects has been investigated as well. For this purpose, two dedicated TX and RX modules operating from 100 to 160 GHz were realized [5]. These modules deploy ICs with Gilbert cell multipliers described in the previous section and use a differential end-fire patch antenna that has been designed in CST Microwave Studio and realized on a 127 µm thick RO3003 substrate. The size of the patch is 745 x 545 µm and its feed-point is matched to a 100 Ω differential line using an impedance transformer, which consists of two 100 µm wide microstrip lines spaced by 300 µm. The simulated return loss and gain of the antenna across the required band are better than -10 dB and 6.9 dBi, respectively. The simulated radiation efficiency is 96%. Photographs of realized Gilbert-cell based TX/RX modules with off-chip antennas and two types of differential chip-to-antenna compensation structures are shown in Fig. 5. Design and performance of both types of the compensation structures are described hereafter.



a) b)

Fig. 5. A photograph of realized Gilbert-cell based TX/RX modules with off-chip antennas and two different chip-to-antenna compensation structures: LCL (a) and differential microstrip stub (b) interconnects [20].

The first compensation structure consists of two bondwire bridges (gold wires with a diameter of 17 µm) with a common contact point at an intermediate off-chip pad that acts as a capacitance of 15 fF to ground (Fig. 5a). This configuration forms an LCL T-network, which turns this interconnect into a matching structure between the output pads of the IC and the differential feed-point of the antenna. The distance between the output pads of the chip and the antenna structure is 800 µm. The estimated bondwire length at both sides of the T-network is approximately 320 µm.

Very low-profile interconnects were possible thanks to the ultrasonic wedge-bonding and horizontal alignment of the chip pads and the off-chip metal structures. To further lower the inductance, two bondwires are used in parallel.

Bondwires in the second topology connect the output chip pads directly to a differential matching structure (Fig. 5b). The matching structure uses differential microstrip stubs to match the chip output together with the bondwire inductance to a 100 Ω differential line. A 500 µm long 100 Ω differential line with 100 µm slot is used to connect the antenna to the matching structure. The whole planar structure was EM simulated and optimized in CST Microwave Studio. The distance between the output pads of the chip and the compensation structure is 350 µm and the estimated length of the bondwire is 365 µm.

The influence of the bondwire interfaces has been evaluated using a wireless link that uses the realized TX/RX modules [20]. Knowing the measured TX output power, LNA gain, simulated antenna gain, pathloss and conversion gain of RX mixer and IF buffer, loss per interconnect was possible to estimate. The result is shown in Fig. 6 for the microstrip stub and LCL interconnects with double bonding (two bondiwres wires in parallel for lower inductance). It can be seen that a 7.5% bandwidth and an insertion loss as low as 0.2 dB are possible. To evaluate the reproducibility, one pair of the TX/RX modules was re-packaged, re-bonded and re-measured. The result is depicted also in Fig. 6 and suggests that high reproducibility of the proposed solution can be achieved.

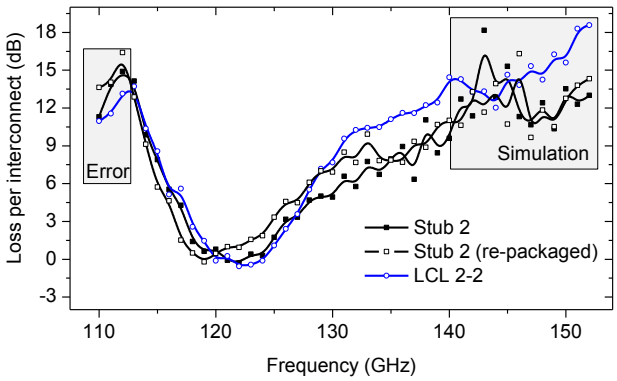
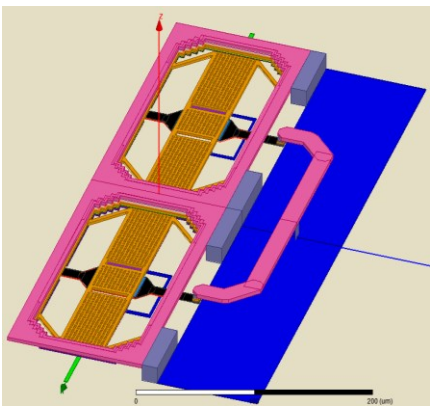


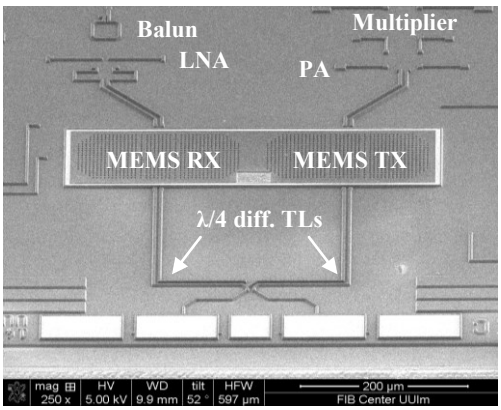
Fig. 6. Loss per interconnect for both compensation topologies derived from the IF measurements. Measurements of completely re-packaged TX/RX modules with Stub 2 interconnects are depicted as well [20].

SPDT Antenna Switch with MEMS

In the next step, the stand-alone TX/RX ICs were integrated in a single IC that can be operated either as a transmitter or a receiver. To allow switching between the antenna and the TX/RX paths, an SPDT switch is needed. The SPDT switch designed for this purpose uses quarter-wave transformers made of TFMLs and MEMS switches in a shunt configuration. An EM model of a single-ended SPDT switch with two MEMS elements is shown in Fig. 7a. Preliminary simulation results of an SPDT with un-encapsulated MEMS suggest excellent performance: insertion loss as low as 1.3 dB, matching better than -10 dB across 90-180 GHz and isolation better that 30 dBc at the mid-band (140 GHz). Since the TX/RX ICs and antennas are designed differentially, the SPDT should ideally be differential as well to avoid losses caused by balanced-unbalanced conversion. For this purpose, a differential SPDT switch with differential MEMS switch was designed. An SEM image of the first differential SPDT switch with MEMS embedded into a TR module with Gilbert cell based multipliers is shown in Fig. 7b. This circuit is currently undergoing on-wafer characterization.



a)



b)

Fig. 7. An EM model of a single-ended SPDT switch with two MEMS elements (a) and an SEM image of the first differential SPDT switch with MEMS embedded into a TR module with Gilbert cell based multipliers (b).

To operate the MEMS switches, voltages up to 60 V have to be generated on chip. Fast charging and discharging of control node is required to ensure high switching speed of MEMS switch. In case of charging the control node by charge pump and discharging the node by a special discharge resistor two problems arise. The first is that high voltages can hardly be reached and the second is high power consumption [21]. The solution is to use a charge pump principle not only for charging the output node but also for discharging the output node. Best suited for this action is the Pelliconi circuit [22]. A triple-well process with n-well, p-well and isolated p-well (p-well that is placed in an n-well that can have high voltage to substrate) is required for this circuit technique to be able to have different nMOS bulk voltages according to rising voltage in the different high voltage stages. Based on the Pelliconi approach, a high voltage generator was realized in an 0.13µm SiGe:C BiCMOS. Measurements have proved full operational functionality with output voltages up to 55 V measured with high-resistance voltage meter.

TRANSMIT AND RECEIVE RADAR MODULES

Before the first deployment of the realized modules in the MIMO configuration, a single-channel radar measurements were carried out. For this purpose, a chirp generator based on a Phase-Locked Loop (PLL) modulated by a Direct-Digital Synthesis (DDS) has been realized with discrete off-the-shelf components. The chirp generator can generate ramps across 13-21 GHz with speed of 20 µs. In this experiment, a chirp bandwidth of 56.8 GHz (104.4-161.2 GHz) was used. To allow IF sampling with a PC soundcard, the speed of the ramp was intentionally slowed down to 37 ms. A block diagram of the single-channel radar measurement setup is shown in Fig. 8a. Raw data of the first range resolution measurements are depicted in Fig. 8b and show the capability to distinguish two reflectors spaced by 3.8 mm.

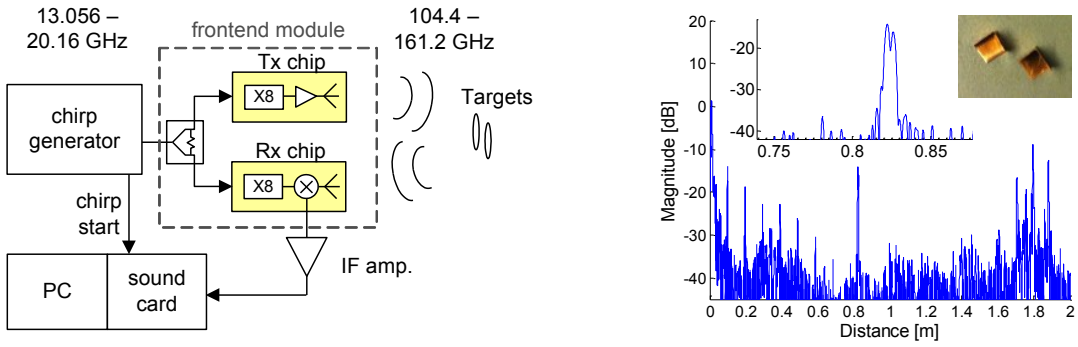


Fig. 8. A block diagram of the experimental single-channel radar measurement setup (a) and measurement results showing the capability to distinguish two reflectors spaced by 3.8 mm even without averaging (b).

A photograph of the first 1D MIMO module equipped with the Gilbert cell based TX/RX ICs and off-chip antennas is depicted in Fig. 9. The module deploys two TX ICs and six RX ICs in a linear arrangement. For coherent chirp signal distribution, a symmetric distribution network with Wilkinson dividers has been realized. The module is currently being tested in a configuration where the two TX ICs are alternately switched on and off and the IF signals from six RX ICs are sampled in parallel.

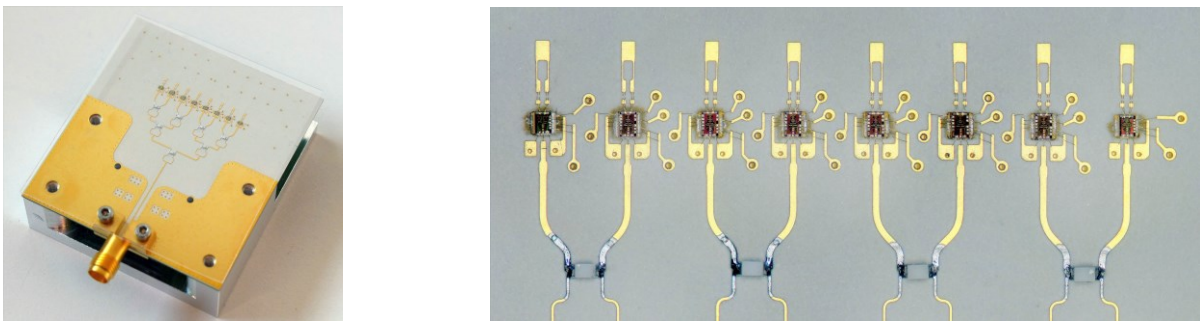


Fig. 9. A photograph of the realized 1D MIMO module with wire-bonded Gilbert-cell based TX/RX ICs that is currently undergoing validation test procedures.

CONCLUSION

Key building blocks for an F-band FMCW MIMO radar system were presented and it has been shown again that the SiGe BiCMOS technology has a very high potential for millimeter-wave radar applications. Different approaches to frequency multiplication were discussed together with the use of on-chip and off-chip antennas. The latter includes

Gilbert cell and push-push based multipliers which are particularly interesting for millimeter-wave applications. Design and measurement results of a state-of-the-art SiGe:C BiCMOS LNA with 20 dB gain and 4 dB noise figure at 110 GHz were also presented.

Packaging aspects were also addressed: two different compensation techniques for millimeter-wave differential chip-to-antenna interconnects were designed and their performance was determined as well, showing that the well-established wire-bonding techniques are still an attractive solution for millimeter-wave interconnects even beyond 100 GHz. All presented IC were implemented in a 0.13 µm SiGe:C BiCMOS technology and are currently being tested in the first 1D MIMO array. Second generation of new TX/RX ICs with integrated MEMS SPDT switch and an on-chip high-voltage generator are being currently tested on-wafer. In the next step, the latter ICs will be integrated into the final 2D MIMO module.

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