A path toward high voltage devices : 3.3 kV 4H-SiC JBS and JFET

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Introduction

In the context of higher voltage reaching, this study presents the methodological design of a 3.3kV 4H-SiC JFET. Different criteria have been studied to determine optimized values for the critical parameters. By taking account of the technological process limitations, we were then able to fabricate the device and reach our aim. The device is classically formed of a drain electrode on the rear face of the wafer, which funnels the current to a source electrode *via* a channel, controlled by a gate electrode.

High voltage sustainability

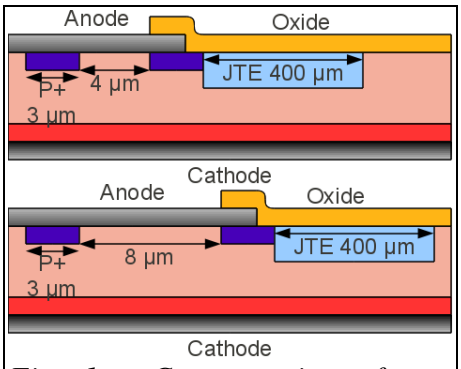

Fig. 1 : Cross section of two different kind of JBS diodes

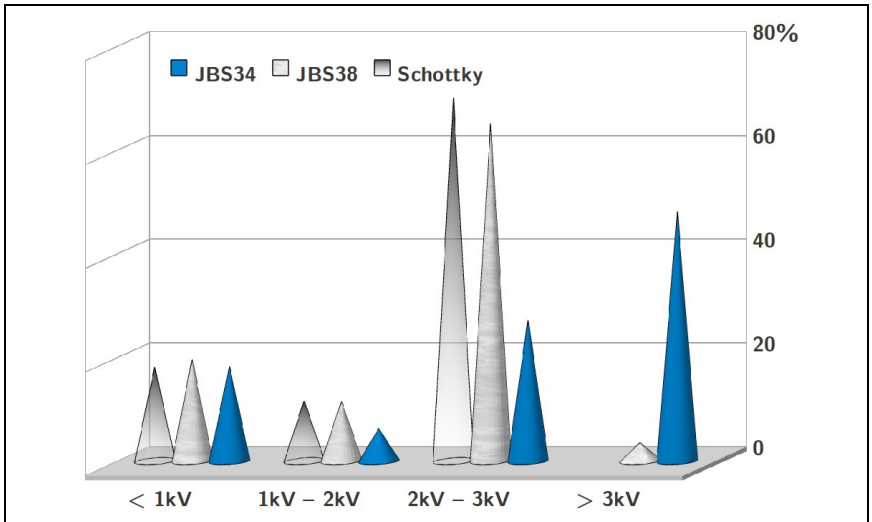

Fig. 2 : Statistical presentation as a function of avalanche voltage

In order to sustain high voltages, we first optimized the first epilayer with a 10^{15} cm^{-3} doping level and 40 µm thick. For this optimization, we have taken into account the edge termination and the passivation efficiency. Schottky and JBS diodes [1] (Fig. 1) were performed on CREE material used as our device support. As a first result, we observed the influence of the P+ strips : their presence or not for Schottky diodes, and their spacing for the JBS (a 3 to 4 ratio or a 3 to 8). Fig. 2 shows that the more bipolar it is, the higher voltage it sustains and the lower they leaks. The reliability of those statistics came from high number of tested samples : 214 Schottky diodes, 224 JBS 3/8 and 459 JBS 3/4. Electrical characteristics on Fig. 3 [2] are *I-V* curves showing the highest voltage sustained by different kinds of diodes. About 50% of JBS3-4 sustains voltage higher than 3kV ; highest reached voltage is 3.5kV, with a mean value of 2.4kV and a 3kV median. On the other hand, all Schottky diodes and 96% of JBS3-8 do not sustain more than 3kV. Peripheral protection are all the same.

Such diodes can also be implemented in an inverter leg as freewheeling diodes.

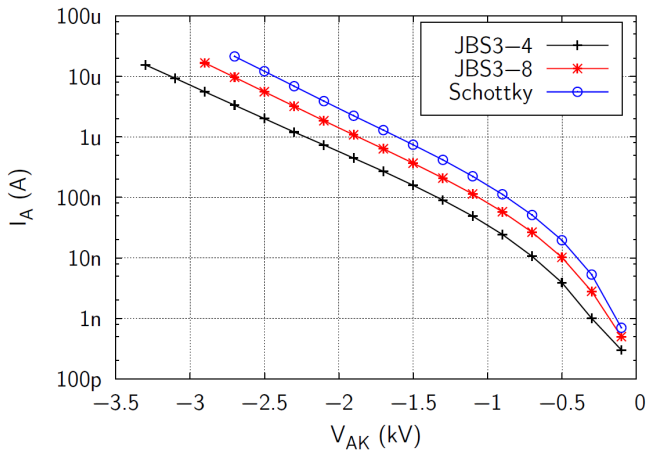

Fig. 3 : Reverse characteristics of JBS 3/4

Design and characterization of JFET

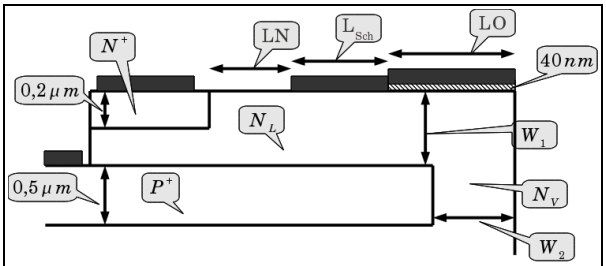

Fig. 4 : Cross section of vertical and lateral channel JFET with a Schottky contact for the upper gate electrode

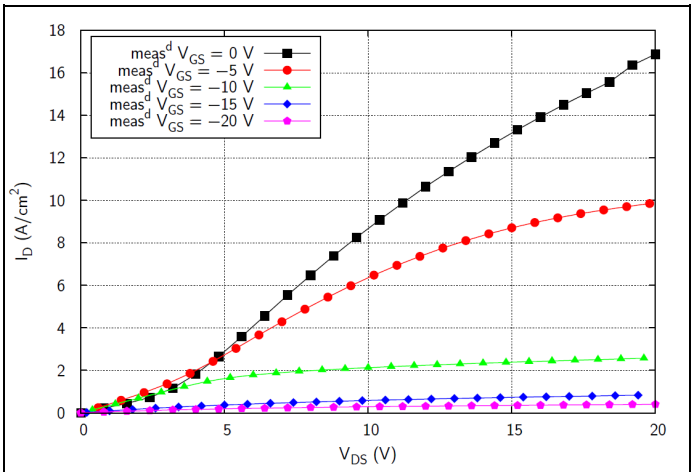

Fig. 5 : Electrical characteristics of the fabricated JFET showing the modulation effect (– 5V step)

Then, to ensure the gate blocking capability of the JFET we decided to add a lateral channel [3,4] in addition to the existing vertical channel. What makes the difference between our structure and the others is the upper Schottky gate oxide-protected (Fig. 4), that ensures both low blocking-command voltage (in absolute value) and low leakage current through the gate [5]. W_1 and W_2 are the widths of lateral and vertical channel respectively, while N_L and N_V are their respective doping levels. *LN* is the margin between the source and the surface gate contacts, L_{Sch} is the length of the Schottky surface gate contact and *LO* is the length of the protecting oxide.

Those last three parameters define the length of the lateral channel and can vary from 3 up to 5 µm. These values are respectively set by technological constraints and the maximum allowed lateral channel resistivity. To make a more efficient and reliable device, we have to find the optimal values for those seven parameters. To this end, we performed finite elements simulations with Sentaurus™. While the breakdown voltage V_{BR} must be maxed out, the pinch-off voltage $V_{GS\text{-}off}$ and the on-state resistance R_{on} must be the lowest as possible. So we used a criterion inspired from Baliga's one [6] : $max\left|\frac{V_{BR}^2}{V_{GS-off}\cdot R_{on}}\right|$

Fig. 5 shows the electrical characteristics $J_{DS}(V_{DS})$ with different V_{GS} at 25°C. Increasing the control voltage V_{GS} from 0 V to – 20 V clearly affects the channel modulation, and -20 V as V_{GS} are sufficient to block the JFET. Measurements have been performed under probes without thick metal layer. So the on-state resistance is lower than expected value.

Summary

The aim we followed was finding new technique to reach 3.3kV. After performing some diodes and study the influence of geometry, we design and fabricate a JFET based on a new structure with low leakage levels. Both components (diode and JFET) ensure a 3.3kV blocking voltage and open new paths for many applications.

References

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