An integrated class D audio amplifier based on sliding mode control

Gaël Pillonnet, Rémy Cellier, Nacer Abouchi, Monique Chiollaz

► To cite this version:

Gaël Pillonnet, Rémy Cellier, Nacer Abouchi, Monique Chiollaz. An integrated class D audio amplifier based on sliding mode control. IEEE International Conference on Integrated Circuit Design and Technology, Jun 2008, Grenoble, France. pp.4, 10.1109/ICICDT.2008.4567259 . hal-01103736

HAL Id: hal-01103736

<https://hal.science/hal-01103736>

Submitted on 15 Jan 2015

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

An Integrated Class D Audio Amplifier based on Sliding Mode Control

Gael Pillonnet, Rémy Cellier, Nacer Abouchi, Monique Chiollaz
Advanced Audio Research Laboratory at CPE Lyon/INL
Grenoble/Lyon, France
gael.pillonnet@cpe.fr, remy.cellier@st.com

Abstract — Class D amplifiers are becoming the most feasible solution for embedded audio application. However, distortions due to the non-linear nature of switching stage are the main drawback for this amplifier topology. This paper discusses the design and implementation of high fidelity audio class D using sliding mode control scheme. This design method proves to be a cost effective solution for industrial circuit. Experimental IC results, using commercial 0.13 μm CMOS technology, verified the theoretical results: the efficiency is above 90%, THD is lower than 0.01% and PSRR is superior to 70 dB.

Index Term — Switching audio amplifier, Sliding mode control, linearity, feedback.

I. INTRODUCTION

The audio class D amplifiers are widely used in various industrial portable and consumer electronics such as mobile phone, due to their high efficiency behavior compared with linear amplifier (class AB) [1].

The open-loop class D amplifier is composed by a Pulse Width Modulator (PWM), a power stage and an output filter as depicted on figure 1. The PWM comparator compares the input signal V_{in} with internally generated carrier waveform at high frequency. Resultant waveforms (V_{pwmm} , V_{pwmp}) are a series of pulses where the pulse width is proportional to amplitude of input signal V_{in} . The power stage is used to provide sufficient current to drive a low impedance load. The H-bridge scheme is used to increase the output power by four times compared to the single-ended solution. The unwanted signal components of PWM are removed by the LC output filter.

The motivating factor research in class D amplifier is efficiency. It results in a remarkable high power efficiency of 100% while an ideal switching characteristic is presumed. This is because the output power MOS operate in the triode and cut-off regions, hereby dissipating very low quiescent power.

One major drawback of the open-loop class D architecture is its non-linear behavior [1-5]. Audio quality is limited: Total

Harmonic Distortion (THD) is typically 0.1% and Power Supply Rejection Ratio (PSRR) is low.

Figure 1. Open-loop class D amplifier

Several approaches have been described to alleviate this problem. Power stage perturbations and power supply noise can both be limited with feedback from the output power stage. Some solutions are used: control based on Sigma Delta Modulator [6], Controlled Oscillated Modulator (COM) architecture [7], PWM feedback [8-9], digital feedback [10,11], bang-bang control [12,17], and sliding mode [13,14]. However, these techniques provide a low PSRR at high frequencies of audio band or they have a high power consumption ($>1\text{mA}$). Moreover it becomes difficult to design a robust controller. The target of this research is to design a class D audio amplifier for mobile application (1W output power), offering both high efficiency and high audio performances.

The proposed design relies on the Sliding Mode (SM) Control, whereby high efficiency and improved sound quality is obtained at very low circuit complexity. The characterization results of the IC using 0.13 μm CMOS technology prove the validity of the theoretical results.

II. PROPOSED ARCHITECTURE

The field of switching electronics poses challenging control problems that cannot be treated in a complete manner using traditional modeling and controller design approaches.

The main difficulty arises from the hybrid nature of these systems due to the presence of switches that induce different modes of operation and operate with a high frequency.

Class D amplifiers invite the application of advanced hybrid systems methodologies. In fact, the amplification is achieved by the use of MOS devices that operate as power switches, turning on and off with a high switching frequency. The two different substructures are: in state 1, the transistor P is ON and the transistor N is OFF, so V_{out} is equal to V_{bat} . The state 2 is the opposite behavior (P OFF, N ON) and V_{out} is connected to the ground. Sliding Mode is alternative solution for control problems in hybrid systems [13-16].

The SM controller is based on the state variables of the system to be controlled. In this approach, the controller allows the output voltage to follow the audio reference voltage by minimizing the average of $V_{in} - V_{out}$. The sliding surface S is given by:

$$S = -K \int_0^t (V_{in} - V_{out}) dt$$

The sign of sliding surface defines the state of class D. If $S > 0$ (the output signal is superior to audio reference), the control switch the power stage in the state 1 to stop the charge transfer into the load. Since it is impossible to switch the system at infinite rate, chattering occurs in the sliding mode using hysteresis cycle [13].

$$-\Delta \leq S \leq +\Delta$$

Figure 2 shows the diagram of the proposed class D amplifier using sliding mode control. The architecture consists of an integrator, a hysteresis controller and a power stage.

Figure 2. The block diagram of proposed solution

The system is asynchronous¹. The switching frequency is here determined by the slope of the sliding surface S . The frequency of one complete cycle is given by:

$$f_s = \frac{V_{bat}(1 - M^2)}{4\Delta\tau}$$

Where V_{bat} is power supply, Δ width of hysteresis windows, τ integration time constant and $M = V_{in}/V_{bat}$ modulation index.

Figure 3 shows the results of simulated switching frequency versus power supply variation V_{bat} [2.3,4.8]V and input level V_{in} . The control parameter (Δ , τ) is chosen to have $f_s = 1\text{MHz}$ at $V_{in} = 0$ and $V_{bat} = 3.5\text{V}$. Since the switching power loss in class D amplifier depends on the switching frequency,

¹ PWM ramp is not present to synchronize and keep constant the switching frequency

the efficiency can be optimized by selecting appropriate values for the control parameters. At transistor level, the circuit has variations due to temperature and tolerance effects. This lead to some variation in the idle switching frequency, but this design maintains f_s out of audio band (higher than 200 kHz).

Figure 3. Simulation results of switching frequency vs V_{in} and V_{bat}

The main advantage of SM control is an excellent frequency response. Actually, the loop bandwidth is equal to the switching frequency because the system has one cycle control response. It offers an inherently infinite PSRR in theory. A high PSRR is offered, making this solution very robust towards perturbations on the supply voltage, like i.e. 217Hz noise in the GSM mobile phone. Moreover, it does not have any carrier generators in the design compared to PWM control [8-11]. It is an effective advantage for the system design and consumption. The proposed control is stable by nature because the sliding surface is bounded by the hysteresis window. The system is robust since the filter is not included within the loop. The external and circuitry variation have not impact in the stability.

This proposed approach has the advantage of spread spectrum EMI, due to the varying switching frequency. The instantaneous switching frequency depends on external parameters: the power supply and the input level. This leads to improved power efficiency at high output levels. In stereo application, the switching frequency difference between the both channels can generate high frequency intermodulation product in audio band.

III. DESIGN OF BUILDING BLOCKS

Analog design of class D amplifier with sliding mode control was done using CMOS 0.13 μm technology. Electrical schematic and layout were shown on figure 4 and 5.

Figure 4. Electrical schematic of proposed solution

When the real OA characteristic (second order behavior) is assumed, the transfer function becomes:

$$C(p) = \frac{1}{RCp} \Rightarrow \frac{G_{dc}}{1 + (\tau_a + (1 + G_{dc})RC)p + RC\tau_a p^2}$$

The degradation off the integrator linearity is significant for an amplifier static gain and bandwidth respectively inferior to 60dB and 3MHz. Moreover, better performance didn't increase linearity of integration but increase consumption.

In hysteresis block, comparators must be design in order to obtain the fastest possible response (10ns of switching delay at 20 μ A of static consumption). RS latch is used to lock state after switching. Bouders of hysteresis window were centered on reference voltage V_{ref} :

$$U+ = V_{ref} + \frac{\Delta}{2} \quad \& \quad U- = V_{ref} - \frac{\Delta}{2}$$

The integrator time constant τ , defined by RC product, and width of hysteresis window Δ can be changed in order to test sliding mode control performance with different switching frequencies. The power stage was designed to optimize efficiency in 8 Ω load under 1W. The ON resistances of MOS transistors were approximately equal to 0.1 Ω and the parasitic capacitors are estimated to hundred of picofarad. The reconstruction output low pass filter ($L=20 \mu$ H, $C=20$ nF) is not integrated in the chip. The square die measures 3.5 mm².

Figure 5. Layout of class D amplifier

IV. EXPERIMENTAL RESULTS

The performances of class D prototype amplifier were measured using audio analyzer (UPV). Unless otherwise noted, assume the following measurement conditions:

- 8 Ω load and $\{L, C\} = \{20\mu\text{H}, 20\text{nF}\}$ in LC filter
- THD and noise measurement at load
- 20Hz to 20kHz measurement bandwidth
- Ambient temperature of approximately 25°C

Figure 6 shows input and output signal in typical work. Duty cycle of output waveform is equal to 50% without input signal. Measured output offset in this case is 2.4 mV.

Figure 6. Waveform of input and output signal

A. Total Harmonic Distorsion (THD+N)

Figure 7 shows the Fast Fourier Transforms (FFT) measured when the signals were 1kHz sine wave of 1W output power. In this case, THD is equal to 85dB (0.005%). With A-weighted filters, which stand for ears sensibility, THD became superior to 90dB.

Figure 7. FFT for 1W 1kHz sine

Figure 8. THD+N versus V_{in}

Figure 8 shows how THD+N (THD including noise) varies with input level at 1kHz. Just before saturation (i.e. $V_{in} > V_{bat} = 3.6\text{V}$), at Full Scale, THD is equal to 95dB. SNR can be measured at -60dB FS ($V_{in}=3.6\text{mV}$) and value is 97 dB (60+37).

B. Power Supply Rejection

PSRR is measured with square wave of 300mV_{pp} (-20dB FS) at 217 Hz, which stand for GSM emission perturbation. In this case, as shown on figure 9, PSRR is above 70dB.

Figure 9. FFT for 1W 1kHz sine with 217Hz square wave on supply

C. Class D audio amplifier comparison

A comparison of the performance of this audio amplifier with the commercial class D audio amplifier [6-14] show on table 1, reveals that our design can seriously compete with one of the switching audio amplifiers ICs leading the market.

TABLE I. CLASS D AUDIO AMPLIFIER COMPARISON

	Current Art	Specification	This work Simulation	This work Measurement
THD+N (%)	0.1 to 0.01	0.01	0.003	0.005
SNR (dB)	80 to 105	95	100	97
PSRR (dB)	0 to 60	60	75	70
Consumption (mA)	2 to 10	1	0.40	0.45

V. CONCLUSION

The amplifier based on sliding mode control offers a state of the art combination of low idle power consumption, high power efficiency and excellent audio performance. This novel control presents, on a low voltage low power IC, a PSRR (70 dB), a linearity (<0,005%) and SNR (97 dB) superior to actual solutions. In addition, low static consumption (<500μA) increases battery life time. Another advantage of this amplifier compared with conventional architectures is the lack of a high frequency carrier modulator which always increases complexity and produces non linearity. This control is protected by a pending patent.

ACKNOWLEDGEMENT

The authors gratefully acknowledge STMicroelectronics that sponsored this work. We would also like to acknowledge the design team of Advanced Audio IP's: F. Amiard, E. Allier, C. Faure, D. Chesneau and P. Marguery.

REFERENCES

- [1] K. Nielsen, "Linearity and Efficiency Performance of Switching Audio Power Amplifier Output Stages - A fundamental Analysis", 105 AES Convention, San Francisco, 1998
- [2] A. Pietro; N. Flemming; R. Lars, "Time Domain Analysis of Open Loop Distortion in Class D Amplifier Output Stages", 27th International AES Conference, September 2005
- [3] Wu and al., "Analytical technique for calculating the output harmonics of an H-Bridge inverter with dead time", IEEE Transactions on Fundamental Theory and Applications, Volume 46, Issue 5, p 617-627, may 1999
- [4] G. Pillonnet, N. Abouchi, "Reduction of power stage THD by adding output capacitance ", 27th Audio Engineering Society (AES) international conference, 1-3 sept. 2005, Copenhagen, Denmark
- [5] G. Pillonnet, « Intégration d'une chaîne de conversion numérique analogique intégrant la modulation par largeur d'impulsion pour la téléphonie mobile », INL/CPE Lyon/STMicroelectronics, Ph.D Thesis, Dept of INL, CPE Lyon, dec 07
- [6] E. Gaalaas, BY Liu, N. Nishimura, R Adams, "Integrated stereo $\Delta\Sigma$ class D amplifier", IEEE journal of Solid-State Circuits, Volume 40, Issue 12, p 2388 - 2397, dec. 2005
- [7] L. Soo-Hyoung, S. Jae-Young Shin, L. Ho-Young Lee, "A 2W, 92% efficiency and 0.01% THD+N class-D audio power amplifier for mobile applications, based on the novel SCOM architecture", IEEE Custom Integrated Circuits Conference 2004, p291-294, 3-6 Oct. 2004
- [8] A. R. Oliva, S.S. Ang, T. V. Vo, "A multi-loop voltage feedback filterless class-D switching audio amplifier using unipolar pulse-width-modulation", IEEE trans. on Consumer Electronics, vol. 50, issue 1, p 312-319, feb. 2004
- [9] K. Nielsen, "High Fidelity PWM based Amplifier Concept for Active Speaker Systems with a very Lower Energy Consumption", 100th AES convention, Copenague, 11-14 may 1996
- [10] P. Midya, B. Roekner, T. Paulo, "High Performance Digital Feedback for PWM Digital Audio Amplifiers", 121th AES convention, San Francisco, 5-8 oct. 2006
- [11] J. Tol and al., "A Digital class D Amplifier with Power Supply Correction", 121th AES convention, San Francisco, 5-8 oct. 2006
- [12] T. Ge, M.T. Tan, JS. Chang, "Design and analysis of a micropower low-voltage bang-bang control class D amplifier", IEEE Int Symp. on Circuits and Systems (ISCAS 2005), p 224-227, 23-26 May 2005
- [13] M. A. Rojas-Gonzalez, E. Sanchez-Sinencio, "Design of Class D Audio Amplifier IC Using Sliding Mode Control and Negative Feedback", IEEE trans. on Consumer electronics, vol. 53, issue 2, p 209-217, may 2007
- [14] G. Pillonnet, N. Abouchi, «A Hybrid System Approach for Class D audio Amplifier», 29th Audio Engineering Society (AES) international conference, 2-4 sept. 2006, Seoul, South Korea
- [15] J.Y. Hung, W. Gao, J.C. Hung, "Variable Struture Control: A Survey", IEEE tran. on Industrial Electronics, vol. 40, n. 1, feb. 1993
- [16] K. D. Young, U. Ozguner, "Sliding Mode : Control Engineering in Practice", American Control Conference San Diego, june 1999
- [17] S. Poulsen, M.A.E Andersen, "Hysteresis controller with constant switching frequency", IEEE Transactions on Consumer Electronics, Volume 51, Issue 2, p 688-693, May 2005