A High Performance Switching Audio Amplifier Using Sliding Mode Control

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Abstract — The switching audio amplifiers are widely used in various portable and consumer electronics due to their high efficiency, but suffers from low audio performances due to inherent nonlinearity. This paper presents an integrated class D audio amplifier with low consumption and high audio performances. It includes a power stage and an efficient control based on sliding mode technique. This monolithic class D amplifier is capable of delivering up to 1W into 8Ω load at less 0.01% THD from a 2.3V power supply voltage in the high fidelity range (20Hz-20kHz). The power supply rejection is superior to 70dB.

Index Term — Switching audio amplifier, sliding mode control, linearity, feedback.

I. INTRODUCTION

The operation of class D amplifier was invented in 1959 by Baxandall, who suggested using LC oscillator [1]. The motivating factor research in class D amplifier is efficiency. It results in a remarkable high power efficiency of 100% while an ideal switching characteristic is presumed. This is because the output power MOS operate in the triode and cut-off regions, hereby dissipating very low quiescent power. Therefore, the audio class D amplifiers are becoming the most feasible solution for embedded audio application such as mobile phone.

One major drawback of the class D amplifier is its non-linear behavior [2-6]. This problem can both be limited with efficient feedback from the output power stage. Even if feedback is used, audio quality is limited: Total Harmonic Distortion (THD) is typically 0.1% and Power Supply Rejection Ratio (PSRR) is inferior to 60dB. The research community focuses now to the efficient error correction by feedback control systems [7-15].

The general close-loop class D amplifier topology is illustrated in figure 1. The circuit is composed by a Pulse Width Modulator (PWM), a power stage, an output filter and the control block. The control block serves to correct the errors introduced by the power stage and the power supply.

The audio input signal V_{in} is compared to the output signal to provide the error signal V_e . The main objectives of control block are to achieve a perfect reproduction of the input signal and command the power stage with a pulse width modulation train. The resultant waveforms (V_{pwmm} , V_{pwmp}) are a series of pulses where the pulse width is proportional to amplitude of input signal V_{in} . These signals drive the power stage composed of MOS devices. The H-bridge scheme is used to increase the output power by four times compared to the single-ended solution. The unwanted signal components of PWM are removed by the LC output filter.

Figure 1. General class D amplifier topology

Several approaches have been described to design the control block. Some solutions are used: control based on Sigma Delta Modulator [7], Controlled Oscillated Modulator (COM) architecture [8], PWM feedback [9-10], digital feedback [11,12], bang-bang control [13,14], and sliding mode [15]. However, these techniques provide a low PSRR at high frequencies of audio band or they have a high power consumption, superior to 1mA. Moreover it becomes difficult to design a robust controller. The target of this research is to design a class D audio amplifier for mobile application (1W output power), offering both low power consumption and high audio performances.

The proposed design relies on the Sliding Mode (SM) control, whereby high efficiency and improved sound quality

is obtained at very low circuit complexity. The characterization results of the IC using 0.13 μm CMOS technology prove the validity of the theoretical results.

II. PRINCIPLES OF SM TECHNIQUE

The main objective of efficient control is minimization of error introduced by power stage with stable frequency response in audio band.

The type of most similar to the proposed solution in this paper is the topology described in [13,14]. The architecture is presented in figure 2.

Figure 2. The block diagram of proposed solution

The operating principle of sliding mode technique is the hysteresis control of the sliding surface S , given by:

$$S = -\frac{1}{\tau} \int_0^t (V_{in} - V_{out}) dt$$

The feedback signal is the output signal taken from the power stage, before the passive low pass filter. The control function integrates the difference between the output voltage and the reference audio signal V_{in} . The hysteresis block generates the PWM binary signal V_c .

The figure 3 shows the input, the sliding surface and the output signals with a modulation index of 0.3. The modulation index is the ratio between input voltage and power supply voltage.

Figure 3. Input, sliding surface and output waveforms at $M=0.3$

The switching frequency varies with the modulation index due to the integration of a variable error, resulting in a flatter slope of sliding surface. The switching frequency of class D based on this sliding mode control is given by:

$$f_s = \frac{V_{bat}(1 - M^2)}{4\Delta\tau}$$

Where V_{bat} is power supply, Δ width of hysteresis windows, τ integration time constant and $M=V_{in}/V_{bat}$ modulation index.

The main advantage of SM control is an excellent frequency response. Actually, the loop bandwidth is equal to the switching frequency because the system has one cycle control response. It offers an inherently infinite PSRR in theory. A high PSRR is offered, making this solution very robust towards perturbations on the supply voltage, like i.e. 217Hz noise in the GSM mobile phone. Moreover, it does not have any carrier generators in the design compared to PWM control [8-11]. It is an effective advantage for the system design and consumption. The proposed control is stable by nature because the sliding surface is bounded by the hysteresis window. The system is robust since the filter is not included within the loop. The external and circuitry variation have not impact in the stability.

This proposed approach has the advantage of spread spectrum EMI, due to the varying switching frequency. The instantaneous switching frequency depends on external parameters: the power supply and the input level. This leads to improved power efficiency at high output levels. In stereo application, the switching frequency difference between the both channels can generate high frequency intermodulation product in audio band.

III. POWER SUPPLY REJECTION IMPROVEMENT

The power supply rejection ratio is one of the primary relevant performance characteristics for the class D amplifier. In fact, the power supply is connected directly to the battery of the personal mobile devices contained system dependent noise. Performance specifications demand that this noise be rejected. The prior works using the SM topology [13,14] integrate a constant hysteresis windows. But this structure is not efficient to limit the switching frequency variation and to obtain a high PSRR.

Specifically, in [13,14], the bang-bang controller is realized based on usual Schmitt trigger (an op-amp with positive and negative feedbacks). In this case, the PSRR can be expressed as:

$$PSRR = \pi M(1 - M) \frac{f_{bat}}{f_s}$$

Where f_{bat} is the frequency variation of the supply voltage.

For example, if the switching frequency is equal to 600kHz and a perturbation on the supply voltage at 1 kHz, the PSRR is inferior to 60dB at $M=0.5$. The smith trigger structure limits the power rejection and cause audible sound during the GSM emission.

To circumvent this problem, we propose to employ a novel architecture based on variable hysteresis windows. The bounds of hysteresis window were centered on reference voltage V_{ref} :

$$U+ = V_{ref} + \alpha V_{bat} \quad \& \quad U- = V_{ref} - \alpha V_{bat}$$

Figure 4 shows the schematic of the windows generation block.

Figure 4. the proposed hysteresis windows genration block

The electrical equations of hysteresis window are given by:

$$\begin{cases} V_{wm} = -\frac{R_1}{R_0}V_{bat} + V_{ref}\frac{R_3}{R_2 + R_3}\left(1 + \frac{R_1}{R_0}\right) \\ V_{wp} = \frac{R_5 R_1}{R_4 R_0}V_{bat} + V_{ref}\left(1 + \frac{R_5}{R_4} - \frac{R_5 R_3}{R_4(R_2 + R_3)}\left(1 + \frac{R_1}{R_0}\right)\right) \end{cases}$$

This variable hysteresis window limits the switching frequency variation du to supply voltage. In the proposed architecture, the switching frequency can be expressed as:

$$f_s = \frac{1 - M^2}{8\alpha\tau}$$

The switching frequency can be made more constant, regardless of M, with the proposed basic design. Because of the reduced switching frequency variation, the supply rejection is maintained and performance of the controller is not reduced.

IV. INTEGRATED CIRCUIT

A Bridge Tied Load (BTL) class D amplifier using sliding mode control is presented in figure 5. The amplifier has been designed on STMicroelectronics CMOS 0.13μm technology.

Figure 5. Functional schematic of proposed solution

In hysteresis block, comparators must be design in order to obtain the fastest possible response (10ns of switching delay at 20 μA of static consumption). RS latch is used to lock state after switching.

The integrator time constant τ , defined by RC product and width of hysteresis window Δ can be changed in order to test the sliding mode control performance with different switching frequencies. The power stage was designed to optimize efficiency in 8 Ω load under 1W. The ON resistances of MOS transistors were approximately equal to 0.1Ω and the parasitic capacitors are estimated to hundred of picofarad. The reconstruction output low pass filter is not integrated in the chip. The square die, shown on figure 6, measures 3.5 mm².

Figure 6. Die of class D amplifier

V. EXPERIMENTAL RESULTS

The performances of class D prototype amplifier were measured when the load is 8 Ω and the input is a 1kHz sine wave source. The power supply used here is 3.6V. In order to minimize the external component size, a small size inductor and capacitor is used. The inductance is 20μH and the capacitance is 20nF. The measurement bandwidth is 20 Hz to 20 kHz. The ambient temperature of approximately is 25°C.

A. Total Harmonic Distorsion (THD+N)

Figure 7 presents the Fast Fourier Transforms (FFT) measured at 1W output power. In this case, THD is equal to 90dB (0.003%). With A-weighted filters, which stand for ears sensibility, THD became superior to 95dB. When the output power is 1mW, the SNR is equal to 97dB.

Figure 7. FFT for 1W 1kHz sine

B. Power Supply Rejection

PSRR is measured with square wave of 300mV_{pp} (-20dB FS) at 217 Hz, which stand for GSM emission perturbation. In this case, as shown on figure 8, PSRR is above 70dB.

Figure 8. FFT of output waveform

C. Class D audio amplifier comparison

A comparison of the performance of this audio amplifier with the commercial class D audio amplifier [6-14] show on table 1, reveals that our design can seriously compete with one of the switching audio amplifiers ICs leading the market.

TABLE I. CLASS D AUDIO AMPLIFIER COMPARISON

	Current Art	Specification	This work Simulation	This work Measurement
THD+N (%)	0.1 to 0.01	0.01	0.002	0.003
SNR (dB)	80 to 105	95	100	97
PSRR (dB)	0 to 60	60	75	70
Consumption (mA)	2 to 10	1	0.40	0.45

VI. CONCLUSION

A single chip low voltage high performances class D audio amplifier has been proposed. By the high power supply rejection ratio coupled with the low consumption, the proposed circuit is suitable for portable devices with battery operations. The control based on sliding mode control offers a state of the art combination of low idle power consumption, high power efficiency and excellent audio performance: a PSRR (70 dB), a linearity ($<0.005\%$) and SNR (97 dB) superior to actual solutions. This control is protected by a pending patent.

ACKNOWLEDGEMENT

The authors gratefully acknowledge STMicroelectronics that sponsored this work. We would also like to acknowledge the design team of Advanced Audio IP's: F. Amiard, E. Allier, C. Faure, A. Nagari and P. Marguery.

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