A topological comparison of PWM and hysteresis controls in switching audio amplifiers

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***Abstract* — The switching audio amplifiers are widely used in various portable and consumer electronics because of their high efficiency, but suffer from low audio performances due to inherent nonlinearity. This problem can be limited with efficient feedback from the output power stage. The research community focuses now to the efficient error correction by feedback control systems. This paper proposes a theoretical and practical comparison between the PWM control and our proposed hysteresis solution. These topologies are widely used in a very wide range of applications. This work shows that the hysteresis solution offers both lower power consumption and higher audio performances for embedded audio application.**

***Index Term* — Switching audio amplifiers, hysteresis control, linearity, PWM feedback.**

I. INTRODUCTION

The audio class D amplifiers offer a high efficiency that can not be matched by any other power amplifier technology, as class AB or class G. It results in a remarkable high power efficiency of 100% while an ideal switching characteristic is presumed. This is because the output power MOS transistors operate in the triode and cut-off regions, hereby dissipating very low quiescent power. Therefore, this way is the most feasible solution for embedded audio application such as mobile phone.

The major drawback of the class D amplifier is its non-linear behaviour [1-5]. Performances in terms of low distortion and noise are improved when a close-loop is used. The main objectives of control are to achieve a perfect reproduction of the input signal and command the power stage with a pulse width modulation train. The research community focuses now to the efficient error correction by feedback control systems.

The loop is shaped by considering the following important parameters: a consistent loop gain at all audio frequencies, high PSRR especially at lower frequencies to lower the demands of supply rejection, a wide open-loop bandwidth to obtain a good transient response, and avoidance of missed pulses at the modulator which can produce undesirable sub harmonic components.

Several approaches have been described to design the control block. Some solutions are used: control based on Sigma Delta Modulator [6], Controlled Oscillated Modulator (COM) architecture [7], PWM feedback [8-9], digital feedback [10,11], hysteresis control [12,13], and sliding mode [14]. Performances differs significantly with the modulator topology are used.

The paper [15,16] compares clearly the linear and non linear methods for audio class D, but concludes that hysteresis control is not the best solution.

The target of this paper is to compare in theory and practice the performances of the PWM feedback and our hysteresis control (patent pending) for mobile application at 1W output power.

II. PWM FEEDBACK TOPOLOGY

A. Principle

The PWM close-loop class D amplifier topology is illustrated in figure 1. The circuit is composed by a Pulse Width Modulator (PWM), a power stage and the control block. The control block serves to correct the errors introduced by the power stage and the power supply variation.

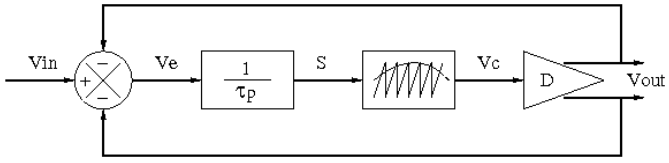

Figure 1. Block diagram of PWM feedback class D

The audio input signal V_{in} is compared to the output signal to provide the error signal V_e. Then, the error signal is integrated by the control block and modulated by PWM

modulator. The resultant waveforms are a series of pulses where the pulse width is proportional to amplitude of input signal V_e. These signals drive the power stage composed of integrated MOS devices. The H-bridge scheme is used to increase the output power by four times compared to the single-ended solution and to improve the power supply rejection.

The passive analog low-pass filter between the power stage and the speaker is required to reduce RF radiation and switching noise entering the speaker. Most commercial class D amplifiers have an uncompensated filter because the filter transfer is unpredictable for load which is not purely resistive, which is the case for practical speakers.

Since the power stage is present in the forward path, the errors generated by the power stage are reduced as specified by the sensitive function H(s):

$$H(s) = \frac{1 + 2RCs}{R_{in} R_{fb} C^2 s^2} G_{pwm} \qquad (1)$$

Where $G_{pwm}=V_{bat}/V_{saw}$ is the linear gain of the PWM modulator and the power stage. Vbat is the power supply voltage connected directly to the mobile battery; Vsaw is the ramp voltage of PWM modulator.

The power supply rejection is increased with a high gain in audio band. The PWM frequency is chosen at ten times higher than the control bandwidth to limit the inherent THD due to the PWM modulation.

B. Integrated circuit

To evaluate and compare in more detail in terms of integration and practical performances, a Bridge Tied Load (BTL) class D amplifier using PWM feedback topology has been designed on CMOS 0.13µm technology (fig. 2). The control system can be implemented without external components for three level modulated outputs.

A switching frequency of 600kHz is used. The power stage was designed to optimize efficiency in 8Ω load under 1W. The ON resistances of MOS transistors were approximately equal to 0.1Ω. The reconstruction output low pass filter is not integrated in the chip. The square die is shown on figure 6.

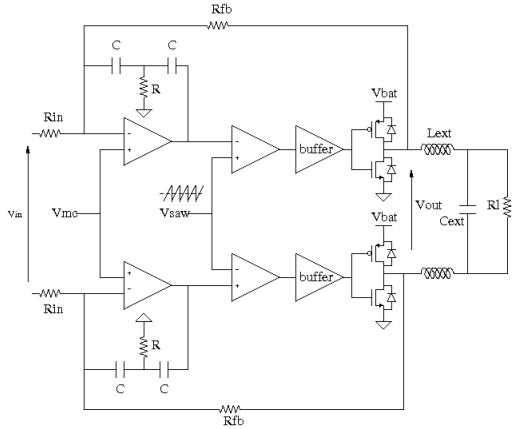

Figure 2. Functional schematic of PWM feedback topology

III. HYSTERESIS CONTROL TOPOLOGY

A. Principle

The main objective of efficient control is minimization of error introduced by power stage with stable frequency response in audio band.

The type of most similar to the proposed solution in this paper is the topology described in [13,14], presented in figure 3, but we introduce a hysteresis windows variation (see equation 1).

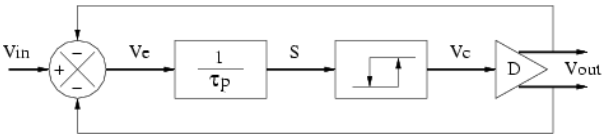

Figure 3. The block diagram of hysteresis solution

The feedback signal is the output signal taken from the power stage, before the passive low pass filter as PWM solution. The control function integrates the difference between the output voltage and the reference audio signal V_{in}. The hysteresis block generates the differential PWM signal V_c in binary modulation.

The operating principle of this technique is the hysteresis control of the error signal, given by:

$$S = -\frac{1}{\tau}\int_0^t (V_{in} - V_{out})dt \qquad (2)$$

If the error signal is ultrasonic (the error frequency is higher than audio bandwidth), the hysteresis controller can be put to practical use even in high end audio.

The figure 4 shows the input, the integrated error S and the output signal with a modulation index of 0.3. The modulation index M is the ratio between input voltage and power supply voltage.

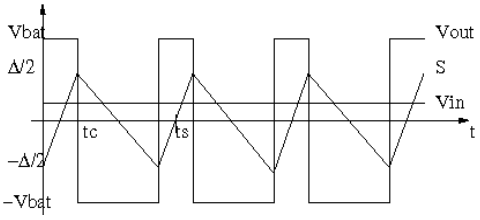

Figure 4. Internal waveforms of hysteresis control at M=0.3

The switching frequency varies with the modulation index due to the integration of a variable error, resulting in a flatter slope. The switching frequency of class D based on our hysteresis control with variable windows width is given by:

$$f_s = \frac{1 - M^2}{8\alpha\tau} \qquad (3)$$

Where V_{bat} is power supply, 2α width of hysteresis windows, τ integration time constant and $M=V_{in}/V_{bat}$ modulation index.

The effect of modulation index in switching frequency necessities the audio signal level limitation to bound the switching frequency variation.

The main advantage of hysteresis control is inherently very good power supply rejection thanks to hysteresis modulator. Actually, the loop bandwidth is equal to the switching frequency because the system has one cycle control response. It offers theoretical an inherently infinite PSRR if the supply rejection can be considered very slow compared to the switching frequency. This solution is very robust towards perturbations on the supply voltage, like i.e. 217Hz noise in the GSM mobile phone. Moreover, it does not have any carrier generators in the design compared to the PWM control. It is an effective advantage for the system design and consumption. The proposed control is stable by nature because the sliding surface is bounded by the hysteresis window. The external and circuitry variation have not impact in the stability.

This proposed approach has the advantage of spread spectrum EMI, due to the varying switching frequency. The instantaneous switching frequency depends on external parameters: the power supply and the input level. This leads to improved power efficiency at high output levels. In stereo application, the switching frequency difference between the both channels can generate high frequency intermodulation product in audio band.

B. *Integrated circuit*

A prototype of hysteresis control illustrated in figure 5 has been build using CMOS 0.13µm technology. The proposed design relies on our hysteresis control solution, whereby high efficiency and improved sound quality is obtained at very low circuit complexity.

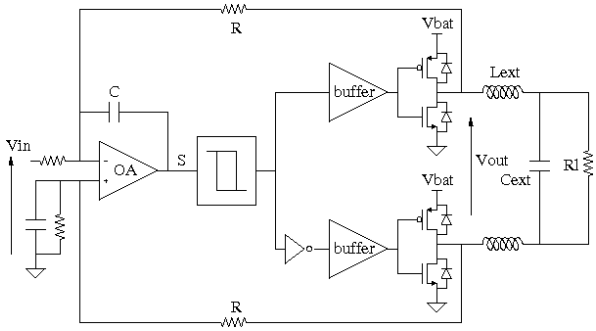

Figure 5. Functional schematic of hysteresis control

In hysteresis block, comparators must be designed in order to obtain the fastest possible response. To maintain the control bandwidth at all modulation index, we propose to employ a novel architecture based on variable hysteresis windows. The bounders of hysteresis window were centered on reference voltage V_{ref}:

$$U+ = V_{ref} + \alpha V_{bat} \quad \& \quad U- = V_{ref} - \alpha V_{bat} \quad (4)$$

The integrator time constant τ, defined by RC product and width of hysteresis window Δ can be changed in order to test the hysteresis control performance with different switching frequencies.

Figure 6 shows the die photographs of implemented solution.

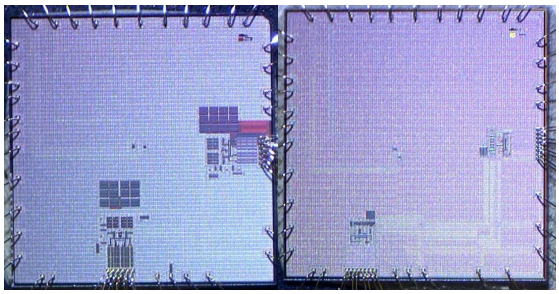

Figure 6. Die of both class D amplifier : PWM (left), Hysteresis (right)

IV. EXPERIMENTAL RESULTS

The performances of PWM and hysteresis topologies are measured and compared in practice on a similar power stage. The load is 8Ω and the power supply is 3.6V. In order to minimize the external component size, a small size inductor and capacitor is used for passive low-pass filter. The inductance is 2µH and the capacitance is 2nF. The measurements were performed with audio analyser (UPV). The idle switching frequency of 600kHz is used for hysteresis circuit, as the PWM solution.

A. *Power Efficiency*

To make a fair comparison, both circuits should be operating at the same conditions: power supply voltage, load. This works achieves a lower consumption of the hysteresis control block. The ternary modulation of the PWM solution improves the efficiency at low power. The both efficiency is up to 90% at 1W output power.

B. *Total Harmonics Distortion*

The first measurement, in figure 7, shows the output spectrum in audio band, using a 1kHz reference signal with the modulation index of 0.7.

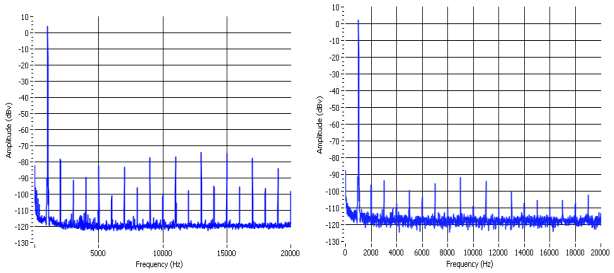

Figure 7. FFT of output signal : PWM (left), Hysteresis(right)

Figure 8 shows the THD versus input level of both circuits (gain 0dB, R=8Ω). The total audio band noise level is not increased with the hysteresis control compared to a PWM system. The dynamic range is 96dB in a 20kHz signal bandwidth.

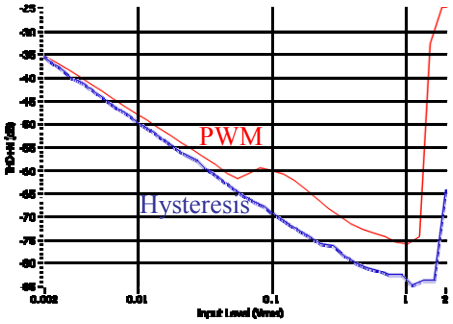

Figure 8. THD+N versus input level

Figure 9 shows THD versus frequency of input tone. The distortion is lower with hysteresis control because of a large control bandwidth. In the PWM control, the inherent THD and the lower sensitive function cause more distortion.

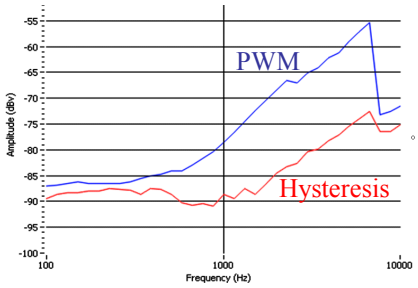

Figure 9. THD versus input frequency

C. *Power Supply Rejection*

Figure 10 shows the output spectrums during power supply variation due to GSM RF emission. The PSRR test conditions are a full scale input signal at 1kHz frequency, V_{bat} equal to 3.6V and a ripple of 300mV_{pp} at 217Hz frequency.

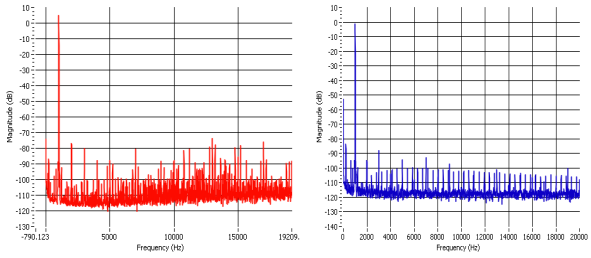

Figure 10. Output spectrum during a GSM burst
PWM (left), Hysteresis (right)

The main benefit of the hysteresis controller is the PSRR improvement of around 20dB due to loop bandwidth equal to switching frequency even if the binary modulation is used.

V. CONCLUSION

This paper has described and compared in theoretical and practice the both main topologies to correct non-linear behaviour of switching power amplifier: the PWM feedback and hysteresis controls. To make a fair comparison, both circuits operating at the same conditions and has been design for mobile phone applications. The advantage of hysteresis feedback is simple modelling and optimization, low consumption (no PWM modulator) and an effective correction of all power stage generated error sources (THD<0.001%). Our hysteresis control presents, on a low voltage low power IC, a PSRR (70dB), a linearity (<0,005%) and SNR (97dB) superior to the PWM solution.

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