A synchronized self oscillating Class-D amplifier for mobile application

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Abstract — **An integrated Class-D amplifier using a synchronized self-oscillating modulator based on a hysteresis control is presented. This new feedback topology can achieve a higher gain bandwidth product to increase linearity and power supply rejection than the fixed switching frequency solutions. The switching frequency spread can also reduce the external EMI filtering constraints. To reduce the idle consumption and radiated emissions at zero output level, a synchronization technique is presented to provide truly differential outputs. The proposed amplifier, realized in CMOS 130nm process, drives up to 1W load with 0.02% THD+N, 90% efficiency with power supply range from 2.3 to 5V. The synchronization technique reduces shows up to 75% of idle consumption**.

I. INTRODUCTION

Due to their high efficiency, Class-D amplifiers are a very attractive solution to implement audio drivers in application with tight power consumption and low voltage requirements such as large electronics consumers systems (mobile phone, GPS…). The basic analog input Class D topology and the signal spectrum of each stage are shown on figure 1. It is composed by a modulation stage which transform low frequency analog audio input signal in high frequency modulated stream V_{mod}. Then, a power stage translates the bit stream to power supply rails V_{OUT} in order to feed the load. A low pass filter decrease high frequency components to rebuild the original signal V_{ls}. This basic topology, called *open loop analog Class-D* suffers from low intrinsic Power Supply Rejection Ratio (PSRR) which make it unsuitable for noisy power supply such as in mobile phone applications. Moreover, the nonlinearity introduced by the signal path (modulator, power stage, filter) affect the audio signal, which not allow the use of this topology for high end application. The key quality parameters, PSRR and linearity, could be increased by an efficient control, but it introduces extra consumption and more complex circuitry. The control of Class-D amplifiers is a key research topic until 90's to find the best trade off structure in order to achieve good quality performances without extra consumption.

In addition, a common problem of switched systems is the Electro-Magnetic Interference (EMI) which is not yet widely investigated for high density PCB like in mobile phone. Class D amplifiers are the sources of both radiated and conducted interferences for neighborhood systems (like DC/DC converter, RF transceiver, digital base band, etc…).

The main focus of this work is to improve the control performances by exploring self-oscillating solution in order to reduce the EMI issue as well by spreading the high frequency tone due to the modulation introduced in the output signal.

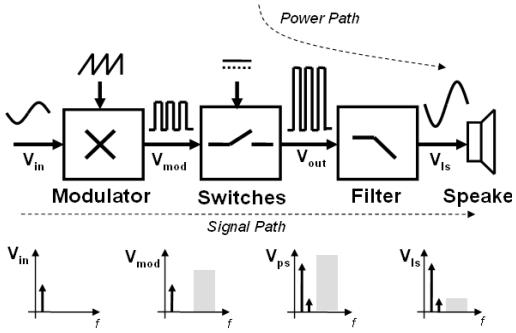

Figure 1. Basic Class-D topology and spectrum of each stage

II. FEEDBACK COMPARISON

Many academic and industrial researches propose control solutions based on large range of modulations and on different type of controller. Theses modulations schemes can be classified in two different categories: the fixed frequency modulation schemes and the self oscillating modulations. The fixed frequency solutions, as the well know PWM (Pulse Width Modulation) [1] and PDM (Pulse Density Modulation) [2] are widely used in industrial circuits. On the other hand, few industrial solutions and publications based on a Self Oscillating (SO) modulation are proposed [3-4-7-10]. SO Class D amplifiers are attractive because they no longer required an external critical clock signal. In addition, they provide a variable switching frequency resulting in a spreading of the output signal spectrum, and the peak of energy as well [11]. However, variable switching frequencies in stereo application

can produce unwanted and annoying folding tones in audio band.

SO behavior can be realized in two main ways, based on phase shift (PSSO) or hysteresis (HSO). For the same switching frequency value, HSO has the best loop gain in comparison to PSSO [5]. Indeed, HSO have a natural second order Noise Transfer Function. These allow the use of a simple first order active integrator corrector saving silicon area in comparison to other controls which required many extra capacitors. A first version of HSO Class D amplifier with single ended output was proposed [10]. But this previous work cannot be used for filter less operation due to binary modulation.

Then, in order to allow "filter less" operation, to save power consumption, to limit high frequency spurious in output signal and to increase output power, Bridge Tied Load (BTL) configuration with three levels modulation is used in almost industrial products [5]. If SO modulation is used, the switching frequencies of both BTL channels are unsynchronized due to channel's mismatches and then it creates extra power consumption due to ripple current into the load. Compare to [10], a new circuitry has been designed to improve the control efficiency (by reducing the loop delay) and the quiescent power consumption (by including a synchronized ternary modulation and using low power techniques). Both the previous work and the proposed work use the same power stage, which allow a relevant comparison of performances.

III. IMPLEMENTATION

A. *Proposed synchronization : three levels HSO*

Unlike BTL PWM Class-D amplifiers, where a ternary modulation is easily achieved by using in-phase carrier, it is quite difficult to realize ternary modulation with SO loop. As the voltage across the load is on three levels, which can not be realized with one hysteresis cycle, a ternary modulation HSO loop must have at least two separates channels. As they have self-oscillating behavior, and due to the process mismatches, the two channels need to be synchronized to achieve correct three levels modulation. As [3, 8] had already proposed for PSSO based amplifiers, a coupling factor K between each channel is introduced in our proposed HSO topology as shown in Fig. 2.

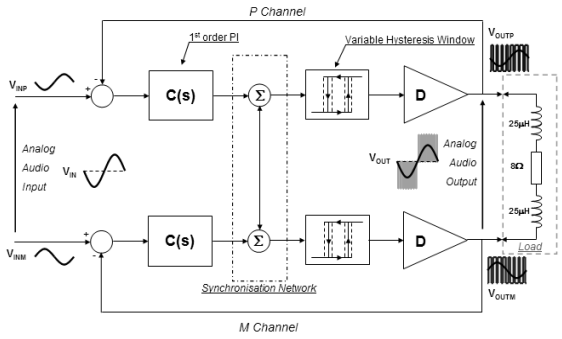

Figure 2. BTL HSO Class-D amplifier with ternary output modulation

The value must be defined in function of the process standard deviation of resistances and capacitors. With bigger value of K, a better synchronized ternary modulation on the output can be achieved, but in spite of less linearity of the fully differential control loop. Indeed, the coupling avoids each channel to oscillate on its own frequency, which dynamically changes the gain of the loop and then decreases the linearity. The choice of K value is then a tradeoff between distortion and efficiency requirements. In the proposed design, a value of 0.1 is used which leading to 80% efficiency at nominal power (0.1W) and 0.02% of THD.

B. *PSRR improvement with variable hysteresis window*

The proposed design used a variable hysteresis window in order to increase power supply rejection [9, 10] by adding a feed forward correction of supply variation and making the switching frequency not sensitive to the supply. For these reasons, the hysteresis limits are built as:

$$\begin{cases} V_{H+} = V_{REF} + \alpha V_{BAT} \\ V_{H-} = V_{REF} - \alpha V_{BAT} \end{cases}$$

C. *Electrical parameters*

The Figure 3 shows the electrical schematic of one BTL channel of the proposed Class-D including the synchronization network and the variable hysteresis window.

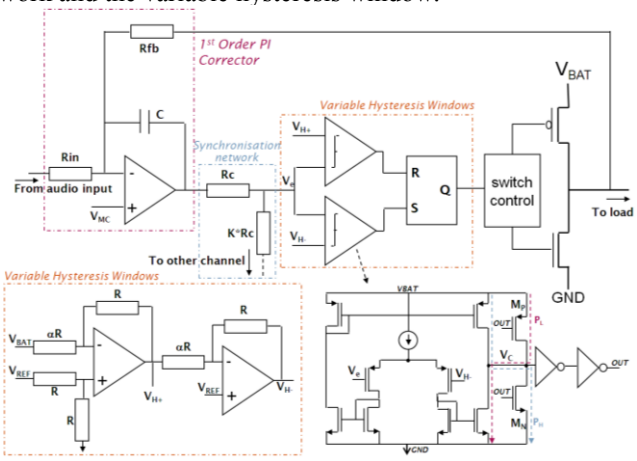

Figure 3. BTL HSO Class D amplifier schematic

With 3.6 V power supply, the design values for α (half of the hysteresis window width) and τ (active integrator pole) are 0.1 and 3.5µs respectively, which leads to 360kHz idle switching frequency (without input signal). This frequency keeps relative high efficiency at low power and enough loop bandwidth to correct all unwanted errors introduced by power supply variation and by power stage. The ratio R_{fb}/R_{in} fixes the audio gain of the amplifier and is equals to 6dB. In addition, a low loop delay is important to avoid the HSO loop to collapse to a PSSO loop [5]. For this reason, the hysteresis window is then built with two low delay comparators. Each comparator is designed using two stages structure and consumes 20µA of quiescent current with a delay of 9ns. In fig. 3, the paths P_H & P_L are used to set up the voltage V_C near to the threshold of the next comparison in order to minimize the commutation time (M_P & M_N transistors have to be sized carefully to avoid comparator glitch). The corrector is implemented as an active RC integrator (R=200kΩ & C=17.5pF) with a 10MHz GBW two stages folded cascode op-amp (170µA of biasing due to synchronization resistive load - fig 3). The choice of α and τ values is a design trade off. A low value of the RC product increases the sensitivity from parasites and current consumption whereas a high value increases both the thermal noise and the die area.

Figure 4 shows the layout of this solution, using double oxide CMOS 130nm technology.

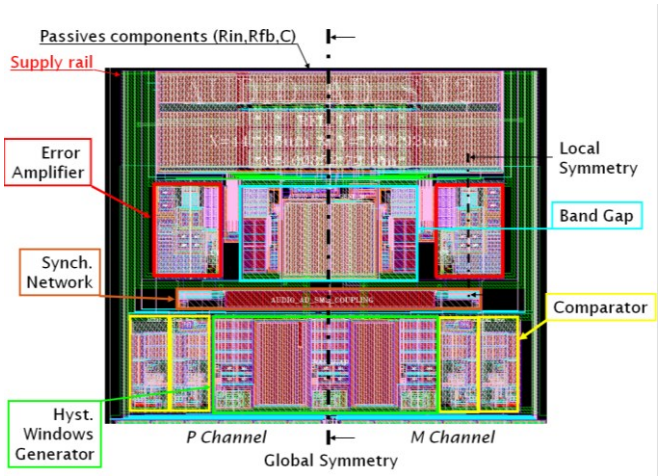

Figure 4. Layout of BTL HSO Modulator for Class-D Amplifier with ternary output modulation

The control area (including error integrator, coupling and hysteresis) is 0.14mm². The power stage size is 0.31mm², which means than stereo version of this Class D amplifier, measures 0.9mm², and each channel is able to provide 1W @0.1%THD in 8Ω load with 4.8V power supply (0.7W with 3.6V).

IV. SILICON MEASUREMENT

The performances of this Class-D prototype amplifier were measured with an 8Ω load with 50µH in series and 1kHz sine wave as input signal. The power supply used in most of the measures is 3.6V. The ambient temperature is 25°C. The idle switching frequency is fully configurable between 364kHz and 512kHz. Otherwise specified, 364kHz is used.

A. Proposed HSO Synchronization

Figure 5 shows THD+N in audio band and efficiency measurements versus output power for synchronized (Sync) or unsynchronized (UnSync) solutions. The noise floor is not impacted by the synchronization (SNR_A=97.5dBA, full scale defined at $1V_{RMS}$). The synchronized mode increases efficiency at low-medium output power but introduces extra distortion on the output signal as shown in section III.A. For example, the linearity is reduced by 5dB when the coupling is active for 0.1W output power, but the efficiency is increased by 15%. The measured amplifier linearity (0.02% at high power) is enough compared to the micro-speaker distortion performance (>1%) integrated in mobile phone application.

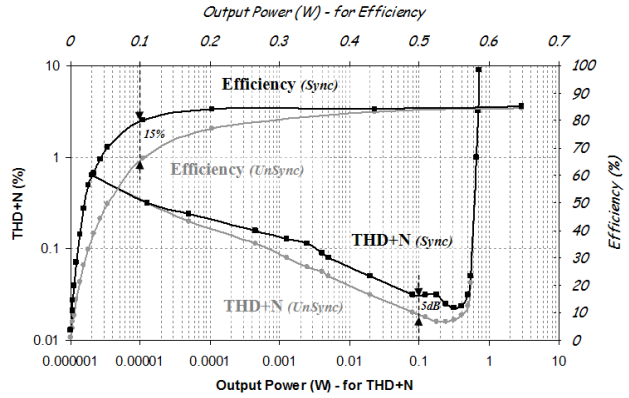

Figure 5. THD+N and Efficiency vs. P_{OUT} @1kHz

In case of stereo application, a frequency offset of at least 20 kHz between the two mono amplifiers idle switching frequency is added. This is necessary to avoid parasitic coupling inter-modulation spurious folding back into audio band when two mono amplifiers are used.

The synchronization increases the efficiency in low and medium power range which is the most use case in listening music test. Music has a crest factor (defined by the ratio between the peak and the RMS voltages) about 10dB or more. A dynamic activation of synchronization depending on signal level could be a solution for high-end application to keep the benefit of efficiency improvement (with synchronization) at low modulation index and higher linearity (without synchronization) at medium to high modulation index.

Figure 6 shows the output waveforms of each BTL channel without input signal. Any mismatches between each channel (passives components, comparators…) leads to unsynchronized square wave between P and M channel (fig. 6, left side). When the coupling is activated, the two channels are synchronized (fig. 6, right side). The output signals are perfectly in phase and then the voltage across load is always null removing the inductor current which causes extra power consumption. The quiescent current is equals to 12mA in unsynchronized mode and fall to 3.7mA with synchronization, saving then 75%. As the coupling reduces the gain of the loop, the output idle switching frequency is a little bit reduced.

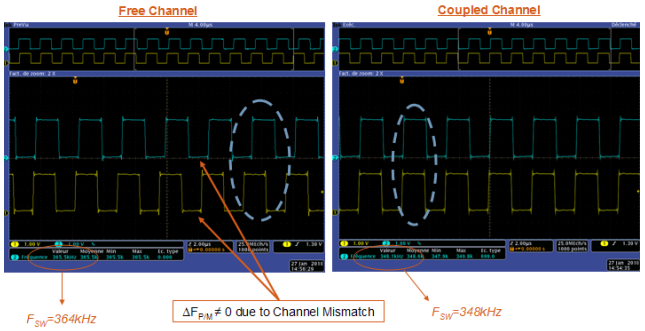

Figure 6. Output voltages of each BTL channel with(out) synchronization

B. Conducted and emitted EMI measurement

As explained in section 2, HSO technique has the benefit to spread output modulation spectrum. Figure 7 shows one BTL channel output voltage spectrum with 512 kHz idle switching frequency. As the switching frequency is dependent on the signal amplitude, then the more the amplitude is high, the more the output spectrum is spread. When the output signal is $1V_{RMS}$, the spread of the switching frequency is large and the maximum amplitude is reduced of 14dBV in comparison of the case without signal.

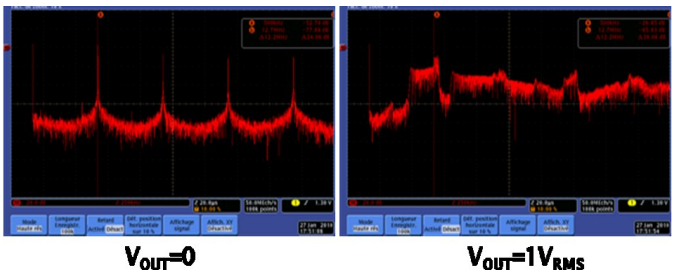

Figure 7. Output spectrum of one BTL channel

Moreover, the spreading method decreases the energy peak of radiated EM fields around the circuit. The figures 8 and 9 show the measurement of magnetic radial fields' magnitude around the chip when the output signal amplitude is $1V_{RMS}$. These measurements were realized into Faraday cage, and done on two Class D topologies (PWM and HSO feedbacks), integrated in an identical package (TQFT 44 pins), using the same power stage, and plugged on the same test board to have relevant comparison measurements. As both circuits use ternary modulation, the maximum radiated energy is located around $2F_{SW}$. The scans have been performed at this frequency (left side) and 10% higher (right side) in order to show the spread of the radiated energy.

Figure 8. Radiated EM measurement bench

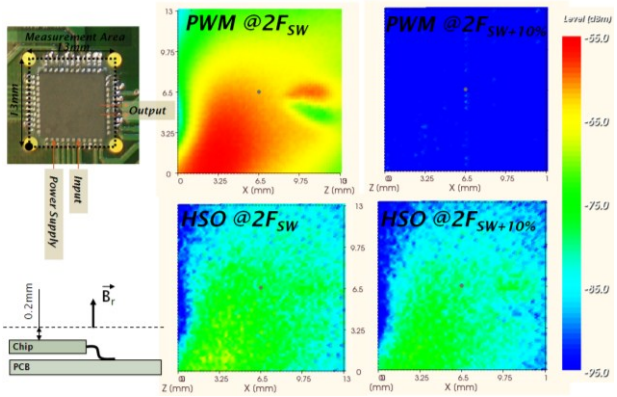

Figure 9. Map of radial magnetic field around the HSO and PWM Class D

As predicted, in PWM modulation, all the radiated energy is located at the switching frequency and its odd harmonics and energy radiation is very low elsewhere (lowest than minimum level measurable). In HSO, the spread appears clearly and the radiated energy is quite constant on the entire frequency band of interest. In addition, the figure 9 shows that the critical localization in term of radiated energy are firstly the supply pins and secondly the output pins, which is logical because it is the place where electric power is located. Only radial component of magnetic field is shown in this paper, but measurement with axial magnetic field and electric field drive to equivalent radiated energy map.

C. State of art comparison

Table 1 resumes the performances of recently published amplifiers. [6] is a recent PWM based Class-D amplifier, using 45nm CMOS process (which explain the low power efficiency). [3,7] are two 1W PSSO Class-D dedicated to mobile phone. [4] is the only one (except the one presented in this work) HSO based silicon Class D amplifier published using ternary modulation ("filter less" capability).

Design	CMOS Process (nm)	Loop Topology	Area (mm^2)	THD (%) @1kHz – 500mW	I_Q – 8Ω (mA)	Efficiency (%) $0.1P_{MAX}$ – P_{MAX}*	SNR (dB_A)
Presented	130	HSO	0.45	0.02	3.9	70 - 87	97
[6]	45	PWM	0.42	0.1	3	30 - 82	100
[7]	350	PSSO	1.2	0.025	1.3*	65 - 90	95
[3]	250	PSSO	1.28	0.02	2.04	Na - 88	97
[4]	500	HSO	1.31	0.05 ***	Na	62 - 88	92

* No load - ** P_{MAX} is defined @1%THD - *** @P=60mW

HSO : Hysteresis based Self Oscillating
PSSO : Phase Shift based Self Oscillating

Table 1. Class D performances comparison

V. CONCLUSION

Synchronized hysteresis control can achieve less electromagnetic emission while keeping the same audio performances and power efficiency as other fixed or variable switching frequency modulator. The introduction of synchronization can increase dramatically the efficiency at low power with an inaudible THD degradation. Silicon results confirm the interest of hysteresis control to achieve quiet and high end Class-D amplifier. It has been shown that self-oscillating Class-D Amplifiers are good alternative to wide spread PWM ones by reducing circuitry area, increasing loop order and spreading EMI.

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