3D Packaging Structure for High Temperature Power electronics

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Outline

Introduction

The 3-D structure

Module Manufacturing

Conclusion
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Conclusion
High Temperature Power Electronics

- Actuators and electronics close to the jet engine
- Deep thermal cycling (-55/+225°C)
- Long operating life (up to 30 years)
High Temperature Power Electronics

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- Long operating life (up to 30 years)
- Share the cooling system between electrical and internal combustion engines.
- Cooling fluid temperature: 120 °C
High Temperature Power Electronics

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- Cooling fluid temperature: 120 °C
- continuous operation, low thermal cycles count
- e.g 5 years operation at 225°C
High Temperature Power Electronics

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- Share the cooling system between electrical and internal combustion engines.
- Cooling fluid temperature: 120 °C
- Continuous operation, low thermal cycles count
- E.g. 5 years operation at 225°C
- Nasa mission to Venus: up to 480°C
- Mission to Jupiter: 100 bars, 400°C
Previous results: SiC JFETs are attractive for $> 200 \, ^\circ C$ operation:

- rated at 1200 V (or more), several Amps
- Voltage-controlled devices
- No reliability issue related to gate oxide degradation
High Temperature Thermal Management


SiC JFET:
- 490 mΩ, 1200 V
- $R_{ThJA} = 4.5 \, K/W$
- 135 °C ambient
- On-state losses

Run-away current changed from 3.65 to 3.7 A

High temperature capability ≠ reduced cooling needs!
SiC JFETs must be attached to a low-$R_{Th}$ cooling system.
Standard packaging offers cooling through one side of the die only

“3-D” or “Sandwich” package: thermal management on both sides

Requires suitable topside metal on the die

Requires special features for topside contact
Double Side Cooling

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- “3-D” or “Sandwich” package: thermal management on both sides
- Requires suitable topside metal on the die
- Requires special features for topside contact
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The proposed 3-D Structure

- Two ceramic substrates, in “sandwich” configuration
- Two SiC JFET dies (SiCED)
- assembled using silver sintering
- 25.4 mm×12.7 mm (1 in×0.5 in)
Ceramic Substrates

- Si$_3$N$_4$ identified previously for high temperature
- For development: use of alumina
- Etching accuracy exceeds standard design rules
- Double-step copper etching for die contact
- Custom etching technique

Scale drawing for 2.4 × 2.4 mm$^2$ die
Bonding Material: Silver Sintering

Silver Paste
- Based on micro-scale silver particles (Heraeus LTS-117O2P2)
- Low temperature (240 °C) sintering
- Low pressure (2 MPa) process

No liquid phase involved:
- No movement of the die
- No bridging across terminals
- No height compensation thanks to wetting
3-D Structure: Challenges

- Behaviour of silver paste during assembly (bridging, compensation of height differences)
- High-resolution alignment of parts
- Etching resolution of the DBC substrates
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Preparation of the Substrates

plain DBC board
Preparation of the Substrates

plain DBC board → 1a - Photosensitive resin coating
Preparation of the Substrates

1a - Photosensitive resin coating
1b - Exposure and Development
Preparation of the Substrates

1a - Photosensitive resin coating
1b - Exposure and Development
2 - Etching
Preparation of the Substrates

1. Photosensitive resin coating
2. Exposure and Development
3. Etching
Preparation of the Substrates

1. Photosensitive resin coating
2. Exposure and Development
3. Etching
4. Resin coating
Preparation of the Substrates

- **plain DBC board**
- 1a - Photosensitive resin coating
- 1b - Exposure and Development
- 2 - Etching
- 3a - resin coating
- 3b - Exposure and Development
Preparation of the Substrates

plain DBC board → 1a - Photosensitive resin coating → 1b - Exposure and Development → 2 - Etching → 3a - resin coating → 3b - Exposure and Development → 4a - Photosensitive film laminating
Preparation of the Substrates

1. Photosensitive resin coating
2. Exposure and Development
3. Etching
4. Photosensitive film laminating
5. Exposure and Development

plain DBC board
1a - Photosensitive resin coating
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3a - resin coating
3b - Exposure and Development
4a - Photosensitive film laminating
4b - Exposure and Development
Preparation of the Substrates

1. **Photosensitive resin coating**
   - **1a** - Photosensitive resin coating
   - **1b** - Exposure and Development

2. **Etching**
   - **2** - Etching

3. **Resin coating**
   - **3a** - Resin coating
   - **3b** - Exposure and Development

4. **Photosensitive film laminating**
   - **4a** - Photosensitive film laminating
   - **4b** - Exposure and Development

5. **Etching**
   - **5** - Etching

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**Notes:**
- **plain DBC board**
- **Ampere**
Preparation of the Substrates

1. Photosensitive resin coating
2. Exposure and Development
3. Etching
4. Photosensitive film laminating
5. Exposure and Development
Preparation of the Substrates

plain DBC board → 1a - Photosensitive resin coating → 1b - Exposure and Development → 2 - Etching → 3a - resin coating → 4a - Photosensitive film laminating → 4b - Exposure and Development → 5 - Etching → 6 - Singulating
Preparation of the Substrates

- Final patterns within 50 \( \mu m \) of desired size
- Two designs, for 2.4\( \times \)2.4 mm\(^2\) and 4\( \times \)4 mm\(^2\) dies
- Total copper thickness 300 \( \mu m \), \( \approx 150 \mu m \) per step
Preparation of the Dies

- Standard aluminium topside finish not compatible with silver sintering
- Ti/Ag PVD on contact areas
- Need for a masking solution
- jig with locating pockets.
Preparation of the Dies

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Before PVD
Preparation of the Dies

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- Ti/Ag PVD on contact areas
- Need for a masking solution
- Jig with locating pockets.

Before PVD

After Ti/Ag PVD
assembly without drying

- 30 min Drying step at 85 °C, 30 min sintering at 240 °C.
- 5 minutes pre-drying before assembly, to increase paste viscosity
  - use of a glass die to observe paste spreading
- Sintering under low pressure (2 MPa)
Sintering process

- 30 min Drying step at 85 °C, 30 min sintering at 240 °C.
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assembly without drying

5 min pre-drying
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5 min pre-drying
Assembly

- Ceramic laser-cut jigs for precise alignment of dies and substrate
- Two sintering steps using the same temperature profile
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- Screen printing
- 2- Mounting in alignment jig
- 3- Die-alignment jig, dies and spacer placing

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- Screen printing
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- 3- Die-alignment jig, dies and spacer placing
- 4 - First sintering step

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Assembly

- Screen printing
- 2- Mounting in alignment jig
- 3- Die-alignment jig, dies and spacer placing
- 4 - First sintering step
- 5 - Removal of die-alignment jig

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Assembly

- Screen printing
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- 4 - First sintering step
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- 6 - Screen printing on "drain" substrate

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Assembly

- Screen printing
- Mounting in alignment jig
- Die-alignment jig, dies and spacer placing
- First sintering step
- Removal of die-alignment jig
- Screen printing on "drain" substrate
- Mounting in alignment jig
- Second sintering step

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Assembly

1. Screen printing
2. Mounting in alignment jig
3. Die-alignment jig, dies and spacer placing
4. First sintering step
5. Removal of die-alignment jig
6. Screen printing on "drain" substrate
7. Mounting in alignment jig
8. Second sintering step

- Ceramic laser-cut jigs for precise alignment of dies and substrate
- Two sintering steps using the same temperature profile
Encapsulation

- Tests performed on a “sandwich” without dies
- Parylene thickness very uniform, including in intricate areas
- Fluorinated parylenes (HT, VT4, etc.) for high temperature capability
Complete assembly
After first sintering step
Die before assembly

0.08
0.06
0.04
0.02
0
-30
-25
-20
-15
-10
-5
0
VG (V)
ID (A)

5

Measured for $V_{DS} = 10 \, mV$

- Only preliminary tests performed, on a probe station
- Contact on Gate, Source and Drain of all JFETs
- No short-circuit between contacts
- Drop in current probably associated with test probes and oxidation of substrate
Prototype

Size: 25×25 mm²
Switching waveforms

- Tests performed on the smallest dies (2.4×2.4 mm², $R_{DS_{on}} = 500 \text{ mΩ}$)
- 300 Ω Resistive load, 0.5 A current (no cooling system used)
- Oscillations due to external layout (and capacitances of the JFETs)
Limitations of the structure

- little contact surface compared to size of substrates
- mechanical stress supported by the dies
- need for stress relief features
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- 3D structure using only high-temperature-rated materials;
  - Should be able to operate continuously at 300 °C, including passivation;
- Silver sintering is suited to rigid sandwich structures;
- Proposed etching technique offers satisfying resolution;
- Package for demonstration of technology, no cooling attempted yet;
- Next step: design a mechanically robust structure.
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Thank you for your attention,

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