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PiSDF: Parameterized & Interfaced Synchronous Dataflow for MPSoCs Runtime Reconfiguration

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Abstract—Dataflow models of computation are widely used for the specification, analysis, and optimization of Digital Signal Processing (DSP) applications. In this talk, we present the Parameterized and Interfaced Synchronous Dataflow (πSDF) model that addresses the important challenge of managing dynamics in DSP-oriented representations. In addition to capturing application parallelism, which is an intrinsic feature of dataflow models, πSDF enables the specification of hierarchical and reconfigurable applications. The Synchronous Parameterized and Interfaced Dataflow Embedded Runtime (SPIDER) is also presented to support the execution of πSDF specifications on heterogeneous Multi-processor Systems-on-Chips (MPSoCs).

I. PARAMETERIZED AND INTERFACED SYNCHRONOUS DATAFLOW (πSDF)

A dataflow Model of Computation (MoC) models an application as a directed graph of computational entities, called actors, that exchange data packets, called data tokens, through a network of First-In First-Out queues (FIFOs) [1]. Synchronous Dataflow (SDF) [1] is the most commonly used dataflow MoC. Production and consumption token rates are fixed scalars in an SDF graph. A static analysis of an SDF graph ensures consistency and schedulability properties that imply deadlock-free execution and bounded FIFO memory needs.

A πSDF specification of an image processing is presented in Figure 1. The top-level graph of this application contains three actors. The Filter actor is a hierarchical actor whose internal behavior is specified with a sub-graph. Parameters size and N influence the behavior of the application at compile time and at runtime respectively.

II. SYNCHRONOUS PARAMETERIZED AND INTERFACED DATAFLOW EMBEDDED RUNTIME (SPIDER)

The SPIDER runtime [3] is a Real-Time Operating System (RTOS) whose purpose is to map and schedule πSDF graphs on heterogeneous Multi-processor Systems-on-Chips (MPSoCs). The SPIDER runtime exploits the parallelism and the predictability of πSDF specifications to minimize the latency of applications.

Figure 2 illustrates the operating principle of the SPIDER runtime. The purpose of the Master core is to make mapping and scheduling choices and send jobs to all processing elements, including itself, through FIFOs. On job completion, a core can send new parameter values and monitoring information back to the master core through the Params and Timings FIFOs respectively. A pool of data FIFOs can be accessed by Master and Slave cores to exchange data between jobs.

REFERENCES