In depth static and low-frequency noise characterization of n-channel FinFETs on SOI substrates at cryogenic temperature

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H. Achour [a,d], B. Cretu [b,c,*], J.-M. Routoure [a,c], R. Carin [a,c], R. Talmat [a,d], A. Benfdila [d], E. Simoen [e], C. Claeys [e,f]

[a] University of Caen Basse-Normandie, UMR 6072 GREYC, F-14050 Caen, France
[b] ENSICAEN, UMR 6072 GREYC, F-14050 Caen, France
[c] CNRS, UMR 6072 GREYC, F-14032 Caen, France
[d] GRMNT, Mouloud Mammeri University of Tizi-Ouzou, Algeria
[e] Imec, Kapeldreef 75, B-3001 Leuven, Belgium
[f] E.E. Dept. KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

A B S T R A C T

The impact of cryogenic temperature operation (10 K) on the short channel effects and low frequency noise was analysed on strained and unstrained n-channel FinFET transistors fabricated on silicon on insulator (SOI) substrates in order to evaluate the devices static performances and to study the low frequency noise mechanisms. The main electrical parameters are investigated and it is evidenced that even at very low temperatures, the strain-engineering techniques boost the devices performances in terms of mobility, threshold voltage, access resistances and drain saturation currents. The DIBL effect, Early voltage and the intrinsic gain are ameliorated only for the short channel devices. A drawback, however, is that slightly improved turn-on capabilities may be noted for standard channel devices compared to strained ones. Low frequency noise measurements show that the carrier number fluctuations dominate the flicker noise in weak inversion even at 10 K operation. Access resistance noise contributions were evidenced in strong inversion.

Keywords:
SOI FinFET
Strain
Very low temperature
Short channel effects
Analog parameters
Low frequency noise

1. Introduction

The development of low and very low temperature microelectronics is of considerable interest for the space industry, which is an important customer of cryogenic electronics since many satellites and space probes consist of a cryogenic enclosure which ensures to maintain the embedded devices at a constant very low temperature (e.g. 77 K and 4.2 K). An advantage of the use of low temperature operation for specific applications is that the devices/circuit performances increase compared to room temperature operation. The temperature reduction leads to a higher speed due to improved transport properties and amelioration of turn-on capabilities. Other favourable aspects of the cryogenic operation are the disappearance of the thermally activated parasitic effects, the decrease of the leakage currents, and the reduction of the interconnection resistances, of the power consumption and of the thermal noise, respectively. Thus, one may note that the parasitic effects which are accompanying the continuous miniaturization of the devices can be controlled by reducing the operating temperature. However, some disadvantages, such as impurity freeze-out, access resistance effects, anomalies in the transient response etc., may appear at low temperature operation and may limit the functionality of the circuits. Other difficulties are associated with the changes in the fundamental mechanisms related with electronic transport and fluctuations in the devices [1–7].

The multi-gate FinFET has been considered as a promising structure for the future technology nodes, in particular since the 3D geometry may offer an improved control of the short-channel effects through a better electrostatic control of the gate over the conduction channel, giving the possibility to achieve a higher I_{ON}/I_{OFF} ratio, and providing an enhanced mobility due to the undoped channel [8–11]. However, according to the International Technology Roadmap for Semiconductors (ITRS), the FinFETs still need to reach a higher I_{ON} to meet the technology requirements. For the enhancement of the device mobility without adding major process complexity, strain-engineering techniques may be used [12–15].

This work is focused on a detailed characterization of unstrained and strained n-channel FinFETs on SOI substrates at very low temperature (10 K) operation in terms of short channel

* Corresponding author at. ENSICAEN, UMR 6072 GREYC, F-14050 Caen, France. Tel.: +33 (0) 2 31 45 27 17; fax: +33 (0) 2 31 45 26 98.
E-mail address: bogdan.cretu@ensicaen.fr (B. Cretu).

effects, analog operation parameters and low frequency noise performances. It is important to observe whether or not strain-engineering is still useful at this cryogenic temperature.

2. Devices and experimental procedures

The studied devices were processed at imec in a 32 nm SOI technology with standard and strain-engineered channels. The tested n-channel FinFETs have a fin width (W_{Fin}) of 25 nm, fin height (H_{Fin}) of 65 nm, 5 fins (N_{Fin}) in parallel and a mask gate length (L_G) varying from 0.13 μm to 1 μm. The gate oxide consists of a high-k dielectric (HfSiON) on top of a 1 nm interfacial SiO_2 resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The tested devices are on standard SOI substrates and on biaxial globally strained sSOI substrates combined with uniaxial local strain by CESL (Contact Etch Stop Layers) and using SEG (Selective Epitaxial Growth) in the drain and source regions (sSOI + CESL + SEG).

The static and the low frequency noise measurements were performed directly at wafer-level using a Lakeshore TTP4 prober. DC measurements were made using an HP4156B semiconductor parameter analyser.

In linear regime operation, the devices were biased with an applied drain voltage V_{DS} = 20 mV for an applied gate voltage V_{GS} which varies from −0.5 V up to 1.5 V. In the saturation regime, $I_D(V_{DS})$ measurements were performed for different fixed applied gate voltage V_{GS} from 0.6 V up to 1 V, for an applied drain voltage V_{DS} which varies from 0 up to 1.2 V.

In the linear regime measurements were performed for all available gate lengths at 10 K, 80 K and at room temperature. The saturation regime operation was investigated for all available gate lengths at room temperature, while at 10 K the measurements were focused only on three mask gate lengths of 0.13 μm, 0.25 μm and 0.7 μm.

The noise measurement set-up allows to bias the devices by choosing the V_{GS} and V_{DS} voltages, and also to measure the total dynamic resistance between drain and source r_T and the transconductance g_m by applying a small signal at the source and gate nodes, respectively. Drain current fluctuations are amplified and the noise spectral density is calculated using a FFT spectral analyser. Noise is reported at the input of the device by dividing by the square of the measured voltage gain between the gate and the output and this for different applied gate voltages. The low frequency noise measurements were focused only on two mask gate lengths (0.2 μm and 0.1 μm).

3. Results and discussion

3.1. Static measurement

Typical output transfer characteristics $I_D(V_{GS})$, $g_m(V_{GS})$ and $I_D(V_{DS})$ for standard and strained n-channel FinFETs at 10 K are shown in Fig. 1(a) and (b). Correct behaviours can be observed even for the shortest mask gate length and one can note that the benefit of the use of a strain-engineered channel seems to be preserved at this low temperature operation.

At temperatures lower than 40 K, the effective mobility has a bell-shaped behaviour with the inversion charge [6,7]. In order to eliminate the effects of the mobility gate voltage dependence at 10 K operation, according to [16], an adapted function (noted Y_{10K}) defined as $(I_D)^{2/3}/(g_m)^{1/3}$ should be constructed. In the inset of Fig. 1(a) is plotted the Y_{10K} function for the shortest mask gate length (L_G = 0.16 μm) for both standard and strained channel. A linear dependence of this function with the applied gate voltage can be observed in strong inversion, as expected. Thereafter, by using the parameter extraction technique described in [16], the main electrical parameters of the studied devices can be estimated at 10 K operation. At room temperature and 80 K operation, the electrical parameters are extracted following the Y-function methodology proposed in [17]. It should be noted that, according to [16,17], the maximum of the effective mobility can be estimated at 10 K, while at 80 K and 300 K it is the low field mobility. The obtained values are summarised in Table 1. The impact of phonon scattering mechanisms decreases with the temperature reduction; this may explain the increase of the extracted mobility from 300 K down to 80 K for both studied structures. The impact of Coulomb and surface roughness scattering mechanisms increases at low temperature operation [18]; this could be associated to the reduction of the mobility at 10 K. The benefit of a strain-engineered channel is evidenced by an enhancement of about 240% of the extracted low field mobility compared to standard ones at room temperature. This enhancement is reduced at 80 K operation (*i.e.* about 200%). One should note that this enhancement of the mobility is drastically reduced at 10 K operation (*i.e.* about 133%); this trend could be associated with a more pronounced impact of the scattering mechanisms (Coulomb and surface roughness) in strained structures at low temperature operation.

The extracted threshold voltage (V_{TH}) values for the 0.14 μm and 1 μm mask gate length for standard and strained n-FinFETs are shown in Fig. 2. The solid line gives the expected behaviour of the threshold voltage increase with temperature reduction, which is modelled with a rate of about – 0.57 mV/K [19]. This trend is not respected at cryogenic temperature operation; at 10 K operation the values of the threshold voltage are lower than those at 80 K. This could be related to the temperature behaviour of the Fermi level and of the surface potential at very low temperatures which are caused primarily by the temperature dependence of the intrinsic carrier concentration [20]. Moreover, the shift of the threshold voltage $|V_{TH}(300\,K) - V_{TH}(10\,K)|$ for the SOI devices is about 110 mV for L_G = 1 μm and 87 mV for L_G = 0.14 μm, while in strained device it is about 41 mV for L_G = 1 μm and 32 mV for L_G = 0.14 μm, resulting in a lower threshold voltage for the strained structures at 10 K.

An important electrical parameter, in particular for dynamic switching circuits, is the subthreshold swing *S*, defined as the inverse of the slope of the log (I_D) versus V_{GS} characteristics in the subthreshold region. Compared to the room temperature value, a theoretical reduction of the substhrehold swing with a factor 3.75 and 30 should be obtained at 80 K and 10 K operation, respectively. Substantial enhancement of the turn-on capabilities could then be obtained only by lowering the temperature. The extracted values of the subthreshold swing for a mask gate length of 0.2 μm are summarised in Table 1. The obtained subthreshold swing values present a slight degradation to the ideal values at room temperature and 80 K (*i.e.* 60 mV/dec and 16 mV/dec, respectively). The difference observed between the expected and experimental values of the *S* parameter at 10 K (ideal value of 2 mV/dec, while experimental value are about 17 mV/dec and 14 mV/dec for strained and unstrained devices, respectively) may be related to an increase of the interface states at the band edges at very low temperatures [4]. Slightly improved turn-on capabilities may be noted for standard channel devices compared to strained ones at all investigated temperatures.

The access resistance R_{access} leads to a decrease of the drain current of the devices compared to the drain current which can be obtained with an ideal device under the same bias conditions and becomes a major concern for scaled down devices. The increase of the parasitic access resistance impact on the output transfer performances is one of the drawbacks related with the use of narrow n-channel FinFETs. The access resistance and the

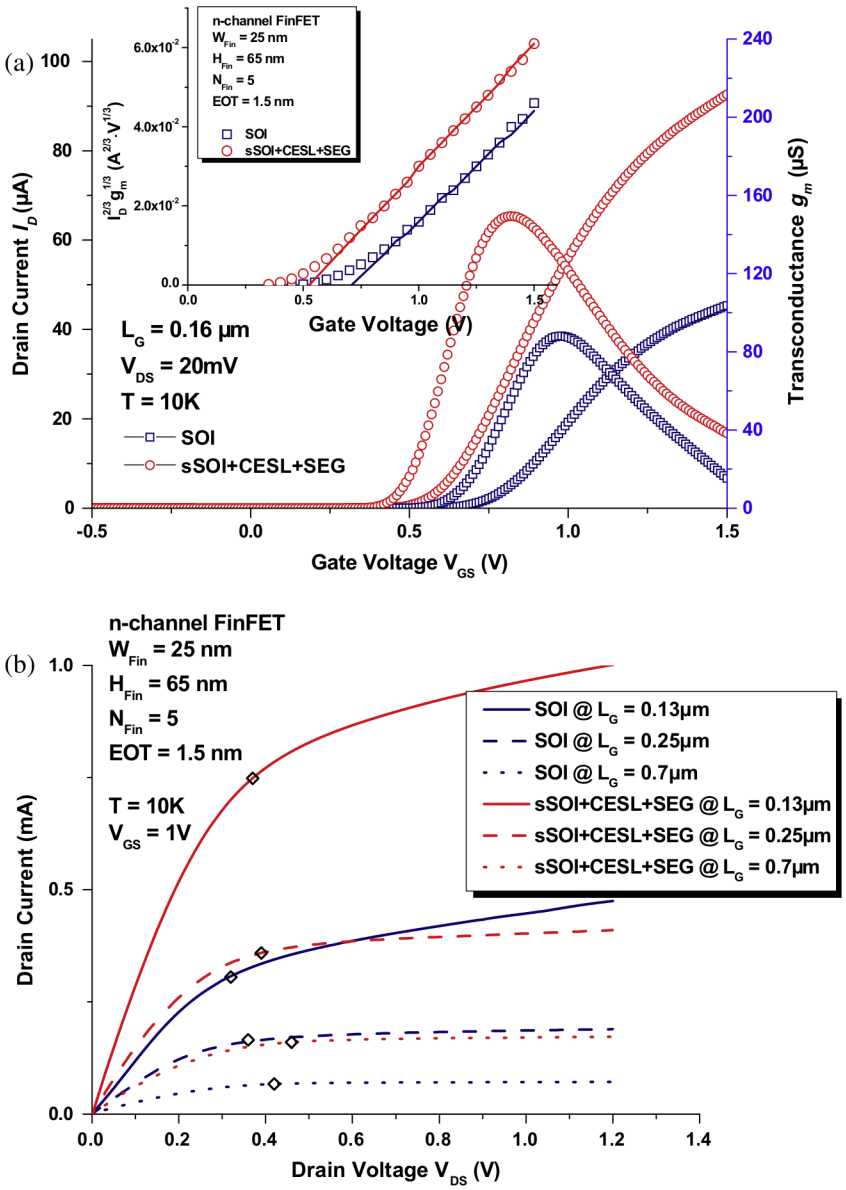

Fig. 1. Typical output transfer characteristics at 10 K operation for standard and strained n-channel FinFET: (a) The drain current $I_D(V_{GS})$ and the transconductance $g_m(V_{GS})$ for a fixed channel length of L_G = 0.16 µm; from the inset can be observed linear behaviour with the applied gate voltage of the $Y_{10K}(V_{GS})$ function in strong inversion. (b) The drain current $I_D(V_{DS})$ for L_G = 0.13 µm, L_G = 0.25 µm and L_G = 0.7 µm. The rhombus points represent the extracted I_{Dsat} and V_{Dsat} levels.

Table 1
Summary of the extracted values for the mobility, access resistance, ΔL and the subthreshold swing at 10 K, 80 K and 300 K. The extracted values of I_{ON} are presented for two channel gate length at 10 K and 300 K.

		SOI			sSOI + CESL + SEG		
		10 K	80 K	300 K	10 K	80 K	300 K
μ (cm^2/Vs)		490	593	220	653	1187	530
R_{access} (Ω)		178	181	210	84	82	123
ΔL (nm)		18	37	54	22	26	49
S (mV/dec) @ L_G = 0.2 µm		14.3	17.2	62.3	16.7	18.1	64.2
I_{ON} (µA)	0.7 µm	71		61	170		142
	0.13 µm	447		433	965		894

difference between the mask and the effective gate length ($\Delta L = L_G - L_{eff}$) of the studied devices are extracted following the total resistance technique described in [21]. The benefit of the integration of SiGe in the source and drain regions, realized by selective epitaxial growth is highlighted by the significant reduction of the access resistance in the devices that received SEG compared to standard ones with about 50–60% for all investigated temperatures (see Table 1). The decrease of the access resistance which can be observed from 300 K down to 80 K is more pronounced for strained devices (about 33%) compared to standard

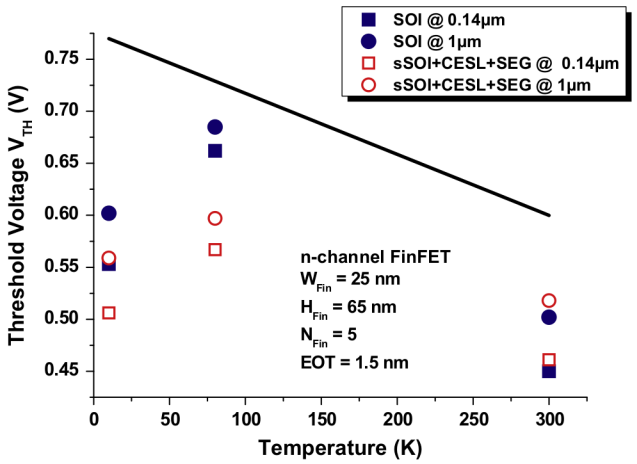

Fig. 2. Threshold voltage V_{TH} versus the temperature for standard and strained devices for two different gate lengths $L_G = 0.14$ µm and $L_G = 1$ µm. The solid line represents the expected increase of the threshold voltage with temperature reduction (rate of −0.57 mV/K).

ones (about 14%). This trend seems not to be followed at very low temperatures: the extracted access resistance values at 10 K are near to those extracted at 80 K. Increase of the access resistance at deep cryogenic operation was already reported and this behaviour is related to the impurity freeze-out of the lightly doped source and drain regions [5].

The effective channel length is a key MOSFET parameter since it is directly related to the current level supplied by the transistor. It is the only one (among the mask, physical (or poly), metallurgic and effective gate length) that can be directly extracted from electrical measurements. The estimated values of ΔL are summarised in Table 1. For a given temperature, the obtained values are quite similar for standard and strained devices. This suggests that the charge charring effect is not significantly affected by the use of strain. As expected, amelioration is observed by lowering the temperature operation: for the shortest channels available (*i.e.* 0.13 µm), the gate voltage controls effectively about 60% of the channel mask length at 300 K against about 85% at 10 K.

The estimated values of the I_{ON} current, defined as $I_{ON} = I_{DS}@V_{DS} = V_{GS} = 1$ V, are presented in Table 1 for a long and a short channel device at room temperature and 10 K operation. The enhancement of the I_{ON} current with temperature reduction from 300 K down to 10 K is more pronounced for long-channel transistors (about 11–19%) compared to short-channel transistors (about 4–8%) for both structures. An I_{ON} increase in strained devices compared to standard ones with a factor of about 2.4 and 2.1 can be observed even at 10 K operation for a long-channel and a short-channel, respectively.

The drift velocity v_D increases with the drain voltage and reaches a maximum at high electric field. For an applied drain voltage higher than the saturation voltage, this maximum is weakly dependent on the applied gate bias. In order to eliminate the influence of the access resistance the following expression can be used for the drift velocity estimation: $v_D = g_m/[WC_{ox}(1 - g_m R_{access}/2)]$ [21]. As expected from theory, v_D is found to vary as the inverse of the channel length even for the short devices due to prevailing mobility limited transport (see Fig. 3a). The use of strain leads to enhanced values of the saturation velocity. Therefore, reducing the temperature increases the drift velocity for both devices due to the reduced phonon scattering contribution. It may be noted that at 10 K, the estimated drift velocity for the shortest strained channel devices (about $10.9 \cdot 10^6$ cm/s for $L_G = 0.13$ µm) is very close to the value of the non-stationary regime at this temperature (*i.e.* $13.2 \cdot 10^6$ cm/s [22]).

In the subthreshold operation, the drain induced barrier lowering effect (DIBL) leads to enhanced source injection resulting in an increased leakage current. The DIBL effect is generally studied by the threshold voltage reduction by increasing the drain voltage ($V_{TH}(V_{DS}) = V_{TH} - \lambda \cdot V_{DS}$, where λ is the DIBL parameter). As this short-channel effect results in a lowering of the source/substrate barrier by applying a high drain voltage, we can estimate the DIBL effect by using the following parameter: $\mathrm{DIBL} = [\partial(\log I_{DS})/V_{DS}]_{V_{GS}=const.}$. The DIBL and λ parameters are linked by the subthreshold slope. In Fig. 3(b) the extracted DIBL parameter at room temperature and at 10 K is plotted. For the shortest channel gate length, an enhancement of the DIBL effect is highlighted by the deviation to the expected variation with the inverse of the channel length (solid lines in Fig. 3b). This trend was already reported for advanced 50 nm nMOSFETs with 1.2 nm SiO_2 dielectric [23]. However, this increase is more pronounced for the standard devices than for the strain-engineered ones. On the contrary, for long gate lengths the strained devices suffer more from the DIBL effect. The DIBL parameter λ, which can be calculated taking into account the extracted values for the subthreshold swing and the DIBL, is represented in the inset of Fig. 3(b). The amelioration of the DIBL effect, which can be observed at very low temperature operation (*i.e.* 10 K), seems to be more significant for short channels (reduction of λ with a factor of about 6 for $L_G = 0.13$ µm against a factor of about 2 for $L_G = 0.7$ µm for both structures). Because this parasitic effect is essentially electrostatic, one expects that the DIBL parameter should be nearly temperature insensitive [24]. However, reduction of the DIBL at lower temperatures was already reported for small geometry devices [25,26].

The obtained values of the absolute Early voltage V_{EA} parameter, defined as $V_{EA} \cong I_{DS}/g_{DS}$, ($g_{DS}$ being the drain conductance measured in saturation at $V_{DS} = 1.2$ V and $V_{GS} = 1$ V) for our devices are shown in the Fig. 3(c). At cryogenic temperature operation, an increase with a factor of about 2 of V_{EA} is observed in strain-engineered devices compared to standard ones for $L_G = 0.13$ µm. This benefit is lost for $L_G = 0.25$ µm and $L_G = 0.7$ µm, for which is evidenced a degradation with a factor about 1.3 and 1.6, respectively. At room temperature operation, the same behaviour is observed; the benefit of using a strained channel is kept for gate length lower than $L_G = 0.5$ µm. Except for the $L_G = 0.13$ µm strained device, the operation at 10 K seems to lead to a degradation of the Early voltage for both structures. Linear dependence of the V_{EA} with the mask gate length can be observed from Fig. 3(c) for standard devices, resulting in a ratio of about 60 V/µm at room temperature, which exceeds the normally reported values for conventional FD SOI [27]. The same ratio (at 300 K) could be observed also for strained devices by taking into account only the shortest channel length ($\leqslant$0.35 µm).

Another common analog figure of merit is the transistor intrinsic gain A_V, defined as $A_V = V_{EA} \cdot g_m/I_{DS}$. Using the obtained values of V_{EA} the intrinsic gain determined at 10 K and at room temperature are presented in the inset of Fig. 3(c) as a function of the gate length L_G. The obtained values are of the same order of magnitude than already reported for a similar FinFET technology [28]. For long channel devices ($L_G = 0.7$ µm) the intrinsic gain is about 5.7 dB higher for unstrained devices compared to strained ones at 10 K, which is about 1 dB higher that at room temperature operation. With the mask gate length L_G downscaling, this difference reduces and for $L_G = 0.13$ µm an improvement of about 2.1 dB (which is 0.4 dB higher than at 300 K) can be observed for strained devices against the standard ones.

3.2. Low frequency noise at 10 K

Typical frequency normalized gate voltage noise spectral density is plotted in Fig. 4(a). One can notice that the noise spectral

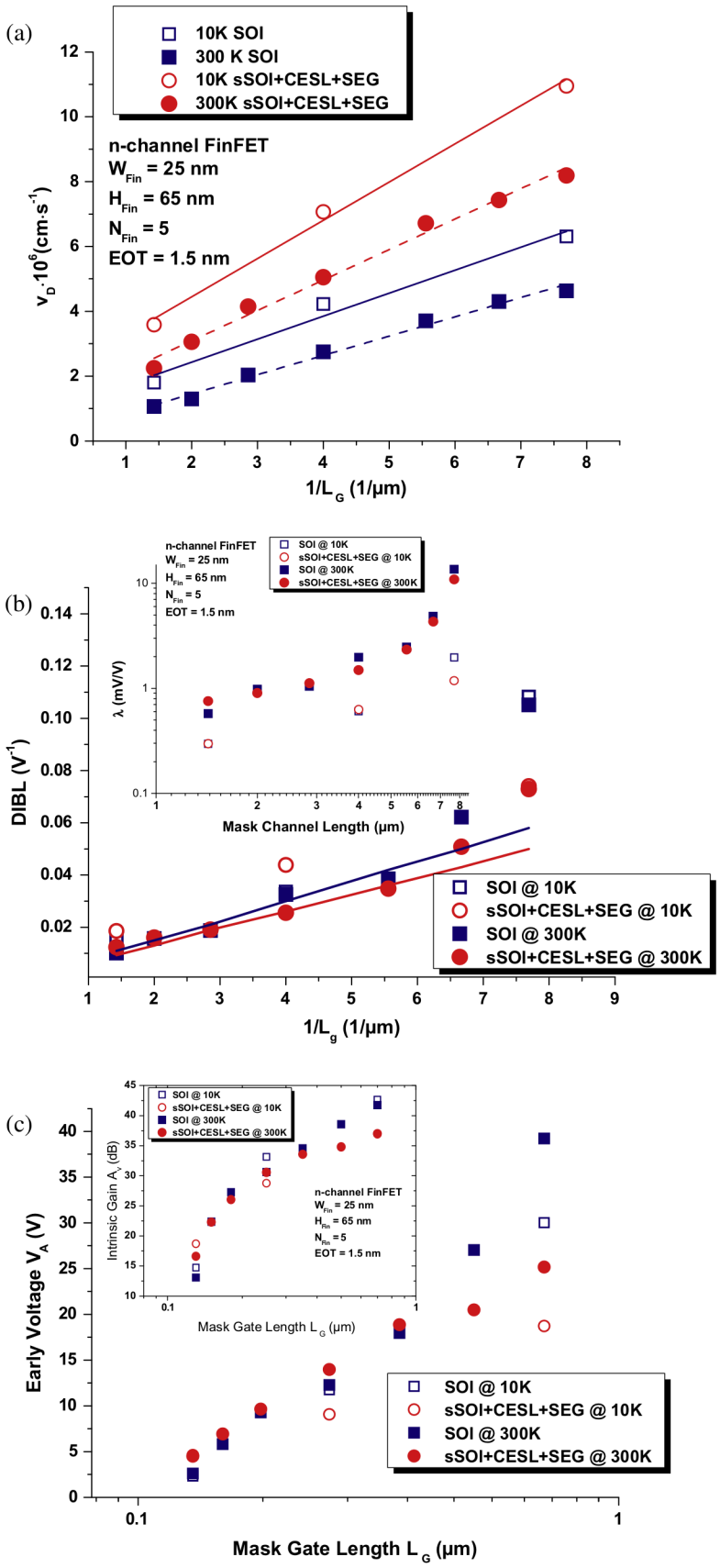

Fig. 3. Extracted parameters at 10 K and room temperature from output characteristics in saturation mode of operation: (a) Intrinsic drift velocity v_D versus the inverse of the channel gate length L_G; (b) The DIBL parameter versus the inverse of the channel gate length; The solid line represent the expected variation as $1/L_G$; In the inset are represented the calculated values of λ DIBL parameter; (c) The Early voltage V_{EA} versus the channel gate length L_G; in the inset is represented the intrinsic gain A_V versus the channel gate length.

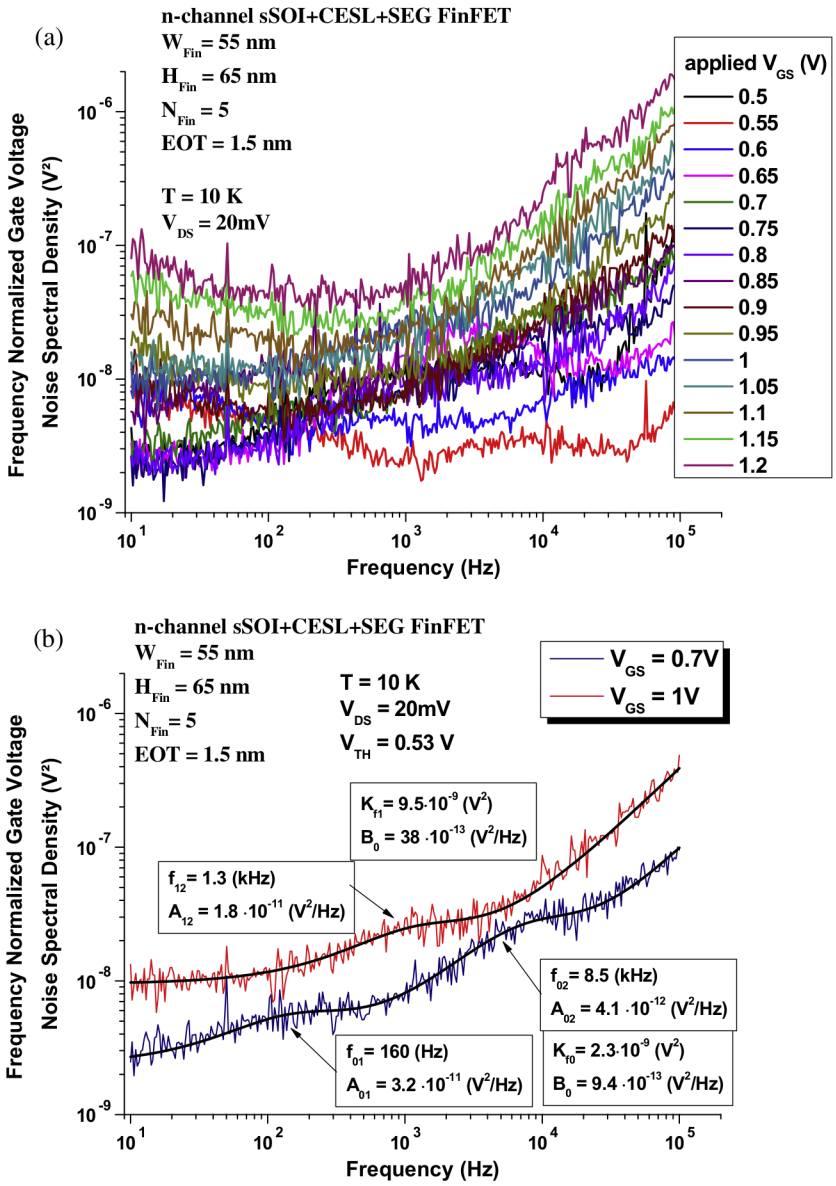

Fig. 4. Typical frequency normalized gate voltage noise spectral density for a strained device at 10 K for L_G = 0.2 µm. (a) For all applied gate voltages; (b) Comparison between experimental noise spectra and model of equation 1 (black lines). White noise, flicker noise and Lorentzian contributions are considered to obtain the best agreement between the experimental noise spectra and model.

density contains both 1/*f* and Lorentzian contributions. Generally, the frequency dependence of the different contributions on the total noise spectral density at the input of a MOS transistor can be expressed as:

$$S_{V_G}(f) = B + \frac{K_f}{f} + \sum_{i=1}^{N} \frac{A_i}{1 + \left(\frac{f}{f_{0i}}\right)^2}. \quad (1)$$

where B is the white noise level, K_f/f is the flicker noise and the third term of the equation presents a sum of Lorentzian components, with A_i the plateau value and f_{0i} the characteristic frequency. As shown in Fig. 4(b), Eq. (1) permits to perfectly model the experimental noise spectra, allowing to identify the different noise parameters.

The extracted 1/*f* noise level (K_f) variations with the applied gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$) are illustrated in Fig. 5 for the two investigated mask gate lengths of the standard and strained devices at 10 K operation. At this cryogenic temperature, the extracted 1/*f* noise levels are found to be independent of the applied gate overdrive in weak inversion for both structures. This suggests that carrier number fluctuations due to electron trapping in the oxide dominate at this cryogenic temperature for both structures. Therefore, the carrier number fluctuation model [29,30] can be used to explain the origin of the noise in weak inversion and to extract an average oxide trap density N_{it} (/eV/cm^3) (see Table 2). Assuming uncorrelated noise sources in the channel and source/drain regions, the total 1/*f* voltage noise spectral density in the linear region of operation can be described by the following equation [21,31,32]:

$$\frac{K_f}{f} = \frac{(r_T - r_{access})^2}{r_T^2} S_{V_{FB}} + \frac{K_r}{f} \frac{r_{access}^2}{2r_T^2} \frac{I_D^2}{g_m^2} \quad (2)$$

where K_r is the access resistance noise level. From Fig. 5 one can observe a good correlation between the experimental points and the model of Eq. (2). This suggests that the increase of the noise

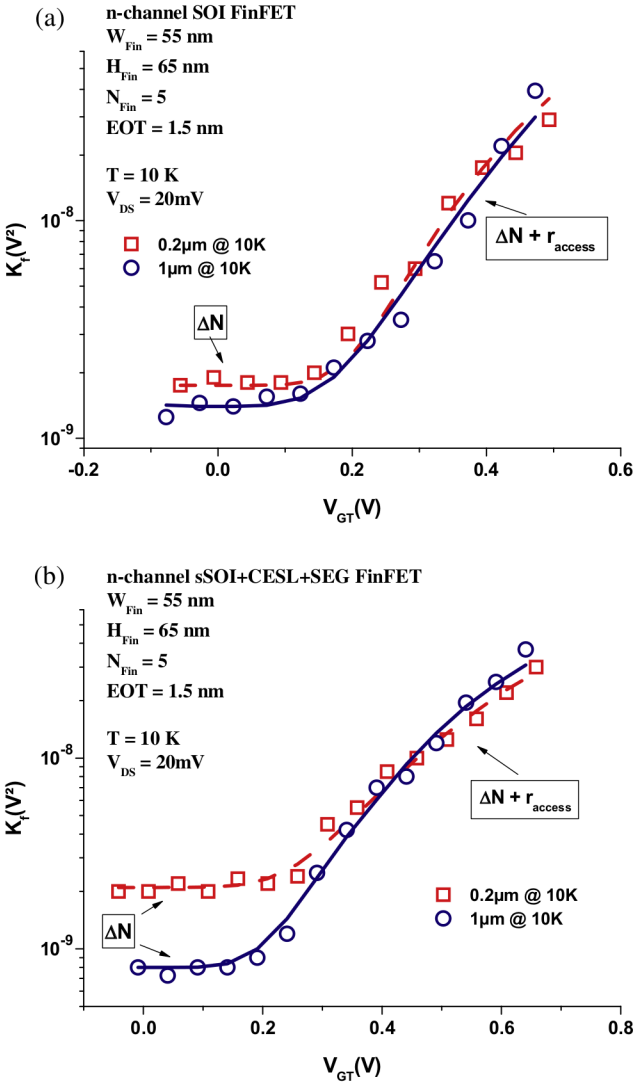

Fig. 5. The extracted $1/f$ noise level K_f at 10 K versus the applied gate overdrive $V_{GT} = V_{GS} - V_{TH}$ for $L_G = 0.2$ µm and $L_G = 1$ µm. (a) Standard devices. (b) Strained devices. Good correlation between the experimental data and model of Eq. (2) is observed.

in strong inversion can be explained by the parasitic access resistance contributions.

In Table 2 are summarised the main extracted noise parameters at 10 K and 300 K. It was already reported that reducing the temperature can lead to enhanced noise levels in n-MOSFETs [33]. An increase of the flat-band noise level is observed in our devices with temperature reduction from 300 K down to 10 K. This increase is more pronounced for strained devices (a factor of about 4.6) compared to unstrained ones (a factor of 1.8) for short-channel devices (*e.g.* $L_G = 0.2$ µm), while for the long channel devices ($L_G = 1$ µm) this increase seems to be not affected by the use of the strain (a factor of about 2.7 for unstrained devices against a factor of about 2.5 for the strained ones).

Except for the $L_G = 0.2$ µm at 10 K, a lowering of the $1/f$ noise level is observed in the studied devices with a sSOI substrate compared to standard ones. This reduction is in agreement with other reported experimental data [34–36]. The relatively small values of the slow insulator trap density are a good indication of the quality of the oxidation process despite the use of high-k dielectrics in such advanced devices. By lowering the temperature down to 10 K, an increase of the trap densities is observed. This behaviour was already reported [33] and can be explained by models which take into account the structure of the high-k dielectric stack considering two tunnelling barriers through the dielectric, corresponding to the interfacial layer and to the high-k layer, respectively [37–39].

It should be noticed that the impact of the carrier number fluctuations correlated to mobility fluctuations is no more observed at 10 K.

The access resistance noise levels are quite similar for both structures for $L_G = 1$ µm. On the contrary, a reduction of the K_r level with a factor of about 3 is observed for strained devices compared to unstrained ones. These may corroborate with the fact that the access resistance impact is more important for scaled down devices and with the access resistance reduction due to the use of SEG in the strained devices.

4. Conclusions

A survey of the short channel effects in standard and strained nFinFETs at cryogenic temperatures has been given. The benefit of the use of strain engineering techniques is kept at very low temperatures: boosted carrier mobility, lower threshold voltage, reduced access resistance, higher I_{ON} current and saturation drift velocity. The saturation velocity is near the non-stationary regime for the short-channel strained devices. The use of strain techniques can lead to opposite behaviours with the channel length reduction: amelioration of the DIBL effect, improvement of the Early voltage and of the intrinsic gain performances can be observed only for short-channel devices. Another drawback is the slight degradation of the turn-on capabilities for strain-engineered devices compared to standard ones for all investigated temperatures. Very low temperature operation improves the DIBL effect for both structures.

A lower $1/f$ noise amplitude was found for devices on sSOI substrates compared to SOI ones. The carrier number fluctuations explain the $1/f$ noise at cryogenic temperature in weak inversion. In strong inversion, the access resistance contribution prevails on the total $1/f$ noise. No correlated mobility fluctuations contributions are observed at 10 K. A lower access resistance noise level was found for short-channel devices which received SEG. The

Table 2
Summary of the extracted noise parameters for standard and strained devices at 10 K and 300 K.

	T (K)	L_G (µm)	$S_{VFB} \cdot 10^{-9}$ (V²/Hz)	$K_r \cdot 10^{-5}$	$\alpha_{sc} \cdot 10^4$ (Vs/C)	$N_{it} \cdot 10^{17}$ (/eV/cm³)
SOI	10	0.2	1.75	1.5		610
		1	1.25	18		2630
	300	0.2	0.96	0	0.5	11
		1	0.45	6.5	0.14	29
sSOI + CESL + SEG	10	0.2	2.1	0.55		730
		1	0.72	19		1490
	300	0.2	0.45	0	0.35	5.1
		1	0.28	0	0.3	17

relative small values of the oxide trap density highlight the quality of the oxidation process.

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