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The impact of different gate dielectrics on the low-frequency (LF) noise behavior is investigated in UTBOX SOI nMOSFETs. Hafnium silicate (HfSiO) devices are compared to silicon dioxide (SiO_2) ones in terms of low-frequency noise apart from the analysis of both front and back-channels. Despite the improvement of process steps for obtaining good dielectric layers, high-k devices have shown elevated current noise spectral density due to the higher number of traps which also degrades the front-channel mobility. Although the buried oxide (BOX) of both wafers is formed by thermal SiO_2, the strong electrostatic coupling between front and back-channels has resulted in a worse noise performance for high-k devices even at the back interface.

Introduction

Ultra-Thin Buried Oxide (UTBOX) transistors have shown attractive features for the sub-22nm technology node, combining a strong electrostatic coupling induced by front and back-channels and, therefore working as a double gate device with the possibility to control the threshold voltage (V_T) through the back biasing (1-3). To improve the immunity to short channel effects, the UTBOX structure has been applied without the source/drain extensions also known as Lightly Doped Drain (LDD) (4). The resulting structure called extensionless (or underlap) transistors were, firstly, more used in three-dimensional technology but, recently, it has also been adopted in the planar version since shortening the channel length has increased the influence of the overlap regions as well as the horizontal electric field into the transistor active region (5,6). Although these devices have presented improved subthreshold characteristics, so that they are being extensively used for ultra-low power applications, lately, they have also demonstrated a superior behavior working as 1-Transistor Dynamic Random-Access Memory (1T-DRAM) cells (7,8). In this case, in order to avoid the leakage current through the gate oxide, high-k materials have been used as the gate dielectric replacing the conventional silicon dioxide (SiO_2) (9). Despite of the improvement obtained in terms of dielectric isolation, high-k materials based on Hafnium result in a dielectric/silicon interface with defects which compromise the device performance. Therefore it becomes mandatory to use a thin layer of SiO_2 (ISSG) between the high-k dielectric and the silicon interface. One way to evaluate the quality of the gate oxide interface and to identify the traps in the depletion area of the transistors is through low frequency noise measurements (10-12). Based on that, the aim of this work is to investigate the low frequency noise performance of the conventional SiO_2 dielectric and the high-k one using

UTBOX nMOSFETs which have been optimized for1T-DRAM cell operation. Both front and back-channels are correlated due to the charge coupling between the two interfaces.

Device Description

The 1 µmx69nm (WxL) UTBOX FD SOI nMOSFETs have been processed at imec on 300 mm wafers with a BOX (t_{BOX}) and silicon thicknesses (t_{Si}) of about 18 and 6 nm, respectively (dimensions obtained after the device processing). The two measured wafers differ from each other only by the gate stack: a conventional silicon dielectric (5nm thermal SiO_2+Poly) and a high-k one (1.5nm ISSG + 4.2nm HfSiO + 5nm TiN + 2nm Si-cap). The devices of both splits present no source/drain extensions, i.e., the extensions below the ~15nm-wide nitride-spacers are left undoped as well as the channel region as can be seen in figure 1. Selective Epitaxial Growth (SEG) of the raised Source-Drain was applied and Phosphorus-HDD implantations are also performed in these wafers. The noise measurements have been performed using the BTA system controlled by the NoisePro software from ProPlus Design Solutions, Inc. The devices have been measured at room temperature along the vertical diameter of the wafer and in linear operation (V_{DS}=0.05V), with the front (V_{GS}) or the back-gate voltage (V_{GB}) stepped from weak to strong inversion. The front-channel noise was measured with V_{GB}=0V and the back-channel one at V_{GS}=0V.

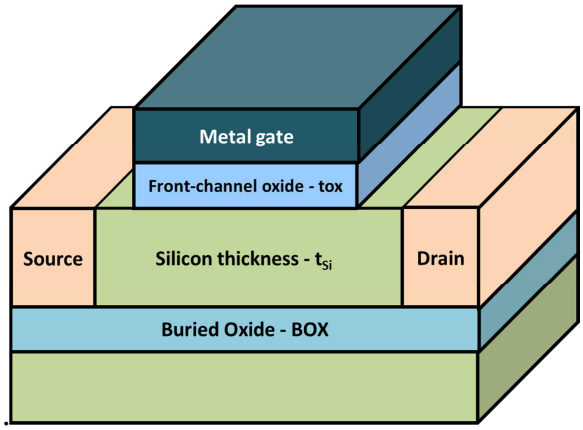

Figure 1. Schematic representation of an extensionless UTBOX transistor.

Results and Discussion

Figure 2 shows the front-channel low field mobility values extracted from the Y-function method (13) obtained for the different measured dies for high-k and SiO_2 wafers. The values scatter around the average point of 60cm^2/Vs for the SiO_2 split and 38cm^2/Vs for the high-k one, underlining that conventional SiO_2 devices present a higher electron mobility with an increase of around 35%. It is also noticed that high-k transistors suffer from a higher variability along the wafer diameter while for SiO_2 devices the spread is closer to the average value.

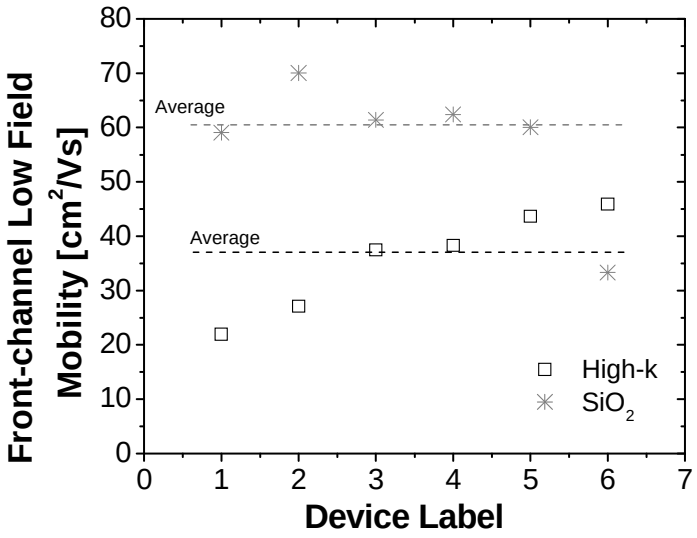

Figure 2: Front-channel low field mobility for each transistor measured along the vertical diameter of the wafer for high-k and SiO_2 splits.

On the other hand, the mobility values extracted from the back-channel is similar for SiO_2 and high-k wafers, being around 50cm^2/Vs and 60cm^2/Vs, respectively, what is consistent to the similarity of both wafers in terms of the BOX processing. The correlation between front and back-channel mobilities can be observed in figure 3 where a trend can be noticed in the sense that a higher back-channel mobility implies a higher front-channel one, mainly for high-k devices with a ratio of 2:1.

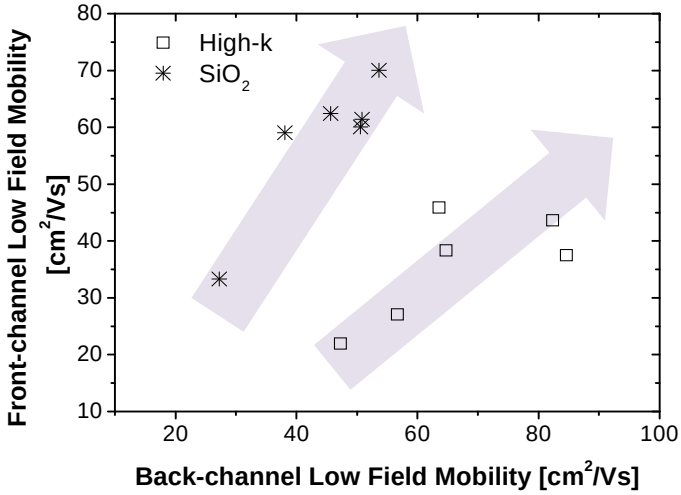

Figure 3: Correlation of front and back-channel low field mobility for high-k and SiO_2 splits.

The input-referred noise (S_{VG}) power spectral density (PSD) has been analyzed at 25Hz for front and back-channels for high-k and SiO_2 wafers as presented in figure 4.

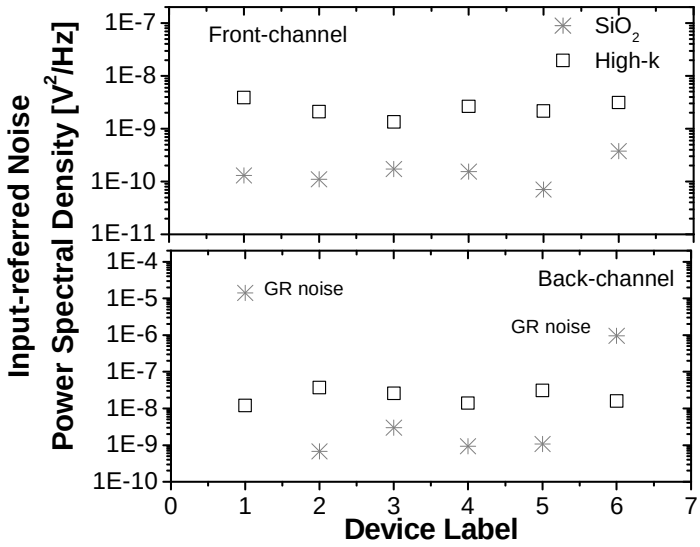

Figure 4: Front and back-channel S_{VG} for high-k and SiO_2 splits at 25 Hz.

As expected, a high-k dielectric results in a degraded noise performance due to the higher number of traps present in these layers. The S_{VG} values are about one order of magnitude higher for the high-k wafer in both channels although they present, predominantly, 1/f noise while excess generation-recombination (GR) Lorentzian noise appears in some of the SiO_2 transistors, indicating the occurrence of traps in the silicon layer. On the other hand, it was reported in (14) that thinner silicon films suffer from the influence of the strong electrostatic coupling between front and back-channels and a trap can induce a Lorentzian PSD profile even occupying different positions. The current-noise spectral density for front and back-channels is presented in figures 5a and 5b, respectively, considering three samples for each dielectric at the same gate overdrive voltage (V_{GT}~0V).

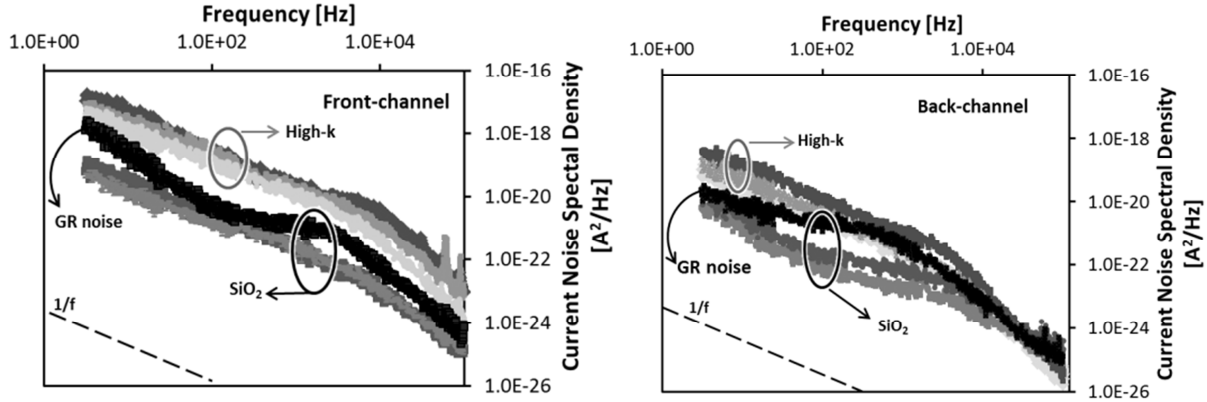

Figure 5: Front (a) and back-channel (b) current noise spectral density versus frequency for high-k and SiO_2 splits, showing the occurrence of a Lorentzian PSD in one of the spectra.

The similarity of the noise level at both interfaces is due to the coupling effect which increases the influence from one interface to the other. High-k devices present current noise levels at least one order of magnitude higher than the SiO_2 ones, even for the back-side where the dielectric is equal for the two wafers, the values change from $1.7x10^{-20}A^2/Hz$ for high-k to

$6.4x10^{-22}A^2/Hz$ for the SiO_2 split at 25Hz, suggesting that the low frequency noise of thin silicon film devices will be predominantly affected by the most degraded interface. Because of that it is difficult to determine the quality of the oxide or the position of the traps in the case of very thin silicon films. One can notice a Lorentzian spectrum in one of the SiO_2 devices that is normally due to deep energy levels in the silicon film which increase the noise value about one order of magnitude at low frequencies.

For the normalized spectral density (S_{id}/I_{DS}^2), represented in figures 6a and 6b, a plateau can be observed in weak inversion followed by a dropping off at the threshold voltage and in strong inversion, indicating that the 1/f noise is due to carrier number fluctuations (15).

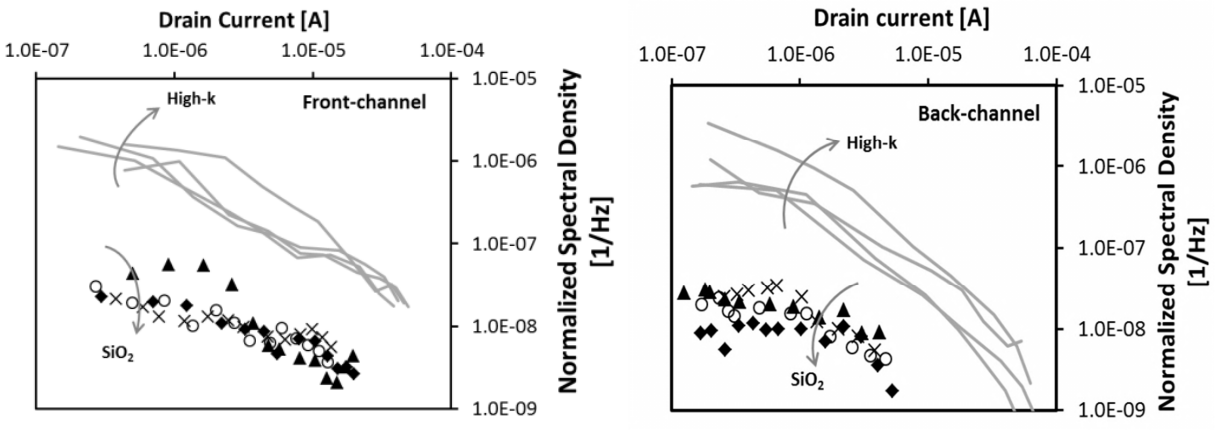

Figure 6: Front (a) and back-channel (b) normalized spectral density versus drain current for high-k and SiO_2 wafers.

The values of S_{VG} for front and back-channels are presented in Table I based on the 1/f-like PSD, including the density of traps calculated from the average of the S_{VG} values, according to the equation 1.

$$S_{VFB} = \frac{q^2 kTN_{ot}}{WLfC_{ox}^2 \alpha} \qquad [1]$$

Table I. S_{VG} at 25Hz and N_{ot} values for SiO_2 and high-k wafers.

		S_{VG} [V^2/Hz]		Density of Traps – N_{ot} [$cm^{-3}eV^{-1}$]
	Channel	**Average**	**Range**	
SiO_2	Front	$1.4x10^{-10}$	$7.0x10^{-11} \sim 3.7x10^{-10}$	$1.7x10^{17}$
	Back	$1.0x10^{-9}$	$6.7x10^{-10} \sim 2.9x10^{-9}$	$9.4x10^{16}$
High-k	Front	$1.9x10^{-9}$	$1.0x10^{-09} \sim 3.7x10^{-9}$	$7.1x10^{19}$
	Back	$2.4x10^{-8}$	$1.1x10^{-08} \sim 9.9x10^{-8}$	$2.2x10^{18}$

Through the values presented in Table I it is possible to notice the significant increase in the number of traps at the front-channel of the high-k devices, resulting in a N_{otb}/N_{otf} ratio of 0.03 against 0.55 for the SiO_2 split. However, even the back-channel presents elevated N_{ot} values, indicating an influence from the front-side in the results due to the strong electrostatic coupling effects.

Conclusions

In this paper we have shown a comparison between UTBOX nMOSFETs with different gate dielectrics based on the low frequency noise analysis. Hafnium silicate devices suffer from a larger number of traps which is about two orders of magnitude higher than for SiO_2. Consequently, the LF noise performance, predominantly consisting of 1/f noise, is worse for high-k transistors whose front-channel mobility is degraded by approximately 35%. Due to charge coupling effects, front and back-channels have demonstrated to be strongly correlated, so that it is becoming difficult to perform an individual analyze of each interface. In spite of the advances to improve the quality of high-k dielectrics, the LF noise behavior has shown to be still a challenge for future technologies.

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