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# Low-frequency noise for different gate dielectrics on state-of-the-art UTBOX SOI nMOSFETs

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#### 1. Abstract

The impact of different dielectrics has been compared in UTBOX SOI nMOSFETs, focusing on the low-frequency noise behaviour. High-k devices have shown higher current noise spectral density due to the higher number of traps that also degrades the front-channel mobility. The back interface presents similar performance in both SiO<sub>2</sub> and high-k wafers while generation-recombination (GR) centers have been noticed in the SiO<sub>2</sub> devices ascribed to traps presented in the silicon film.

#### 2. Introduction

Planar fully depleted (FD) devices with Ultra-thin Buried Oxide (UTBOX) is one of the most promising architectures for sub-22nm technology nodes, offering the ability to control the V<sub>T</sub> based on the back biasing. Moreover, UTBOX devices present an improved response in terms of short-channel effects due to the higher electrostatic coupling between gate and channel, [1],[2]. One of the latest applications for UTBOX technology is the capacitor-less or one-Transistor Dynamic Random-Access Memory cells (1T-DRAM) [3]. However, for reduced silicon film thickness the front-gate DC parameters have become more sensitive to the interface quality and charges in the BOX [4]. Hence, the charges present in the dielectric layers and at the interface affect the electron mobility ( $\mu_N$ ) and  $V_T$  as well as the low-frequency (LF) noise. This is a consequence of fluctuations governed by trapping/ detrapping through the traps positioned in different regions such as the front/back dielectric layers and the silicon film. Since high-k dielectrics have been introduced to avoid the gate leakage current in very thin silicon dioxide layers, the LF noise of these devices has been investigated in order to characterize the quality of the dielectric layer that, normally, presents more traps and a degraded noise performance [5],[6],[7]. It is the aim of the present work to compare the LF noise behaviour of the conventional SiO<sub>2</sub> with the high-k state-of-the-art FD SOI UTBOX nMOS devices, correlating the front and backchannels results for due to the charge coupling between the two interfaces.

#### 3. Device Characteristics

The 1 umx69 nm (WxL) FD SOI nMOSFETs with UTBOX have been processed on 300 mm wafers. The BOX thickness is about 18 and the silicon thickness (t<sub>Si</sub>) is about 6 nm (after the device processing). Two wafers were measured, differing from each other only by the gate stack: a conventional silicon dielectric (5nm thermal SiO<sub>2</sub>+Poly) and a high-k one (1.5 nm ISSG + 4.2nm HfSiO + 5 nm TiN + 2 nm Si-cap). In both cases, the channel is left undoped, as well as the extensions below the ~15 nm-wide nitride-spacers. resulting in extensionless structures [8]. More process details are also reported in [4]. The devices have been measured at room temperature along the vertical diameter of the wafer and in linear operation (drain voltage  $V_{DS}$ =0.05 V), with the front  $(V_{GS})$  or back gate voltage (V<sub>GB</sub>) stepped from weak to strong inversion. The front-channel noise was measured with  $V_{GB}=0$  V and the back-channel one at  $V_{GS}=0$  V.

## 4. Results and Discussion

Figure 1 presents the input-referred noise (S<sub>VG</sub>) power spectral density (PSD) at 25Hz for the front (a) and back (b)-channels, comparing the high-k and SiO<sub>2</sub> splits. As expected, the use of a high-k dielectric results in a degradation of the noise behaviour since these dielectrics present a higher number of traps [6]. The S<sub>VG</sub> values are about one order of magnitude higher for high-k devices in both interfaces (front and back-channels) except for the two highlighted points which indicate the occurrence of GR noise. The current-noise spectral density for front and back-channels is presented in figures 2 and 3, respectively, considering three samples for each dielectric at the same overdrive voltage (V<sub>GT</sub>~0V). One can observe the similarity of the noise level at both interfaces due to the coupling effects in thin silicon films, increasing the influence from one interface to the other. As the backchannel is formed by thermal-SiO<sub>2</sub> one should expect a similar behaviour in both wafers but the influence of the front-side keeps the back noise level around  $1.7x10^{-20}A^2/Hz$  against  $6.4x10^{-22}A^2/Hz$  for the  $SiO_2$  split for 25Hz. It is also possible to notice a Lorentzian

spectrum in one of the SiO2 devices, caused by deep energy levels in the silicon film which increase the noise value about one order of magnitude at low frequencies. For the normalized spectral density (Sid/I<sub>DS</sub><sup>2</sup>), represented by figures 4 (front) and 5 (back), a plateau can be observed in weak inversion followed by a dropping off at the threshold voltage and in strong inversion, indicating that the LF is due to carrier number fluctuations [9]. The correlation between front and back S<sub>VG</sub> can be seen in figure 6. Only the values obtained for 1/f-trend devices are compared and a subtle tendency in the sense that high front-channel noise increases the back-channel one is observed. The mobility correlation presented in figure 7 follows the same trend. Moreover, high-k devices show clearly that the frontmobility is about 40% smaller than for the SiO<sub>2</sub> ones which also present values 1.2 times higher for the front side due to the defects in the back induced by the STI oxidation step [4].

### 5. Conclusions

High-k UTBOX nMOSFETs were compared to  ${\rm SiO_2}$  ones in terms of LF noise performance. In spite of the advances to improve the quality of high-k devices, the LF noise is still a challenge: higher noise level and greater number of traps were obtained in these devices which also present low-field mobility degraded by 40%. Due to the charge coupling effect, front and back- channels are strongly correlated what requires greater attention in the analysis of the properties of both interfaces especially in thinner Si film devices.

#### Acknowledgments

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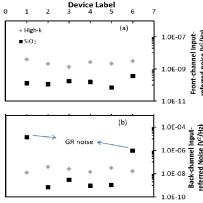


Fig.1: Front (a) and back-channel (b) input-referred noise (SVG) power spectral density for the measured transistors at 25Hz.

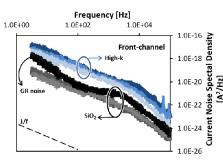


Fig.2: Front-channel current noise spectral density as a function of frequency for three samples with  $SiO_2$  and high-k dielectrics.

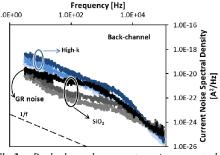


Fig.3: Back-channel current noise spectral density as a function of frequency for three samples with SiO<sub>2</sub> and high-k dielectrics.

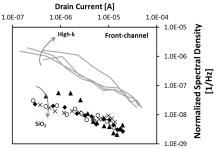


Fig. 4: Front-channel normalized spectral density as a function of drain current for high-k and  $SiO_2$  wafers.

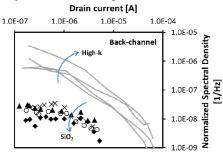
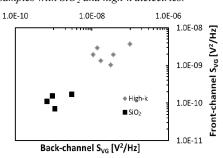


Fig. 5: Back-channel normalized spectral density as a function of drain current for high-k and SiO<sub>2</sub> wafers.



**Fig. 6:** Front-channel versus back-channel  $S_{VG}$  for the two studied wafers.

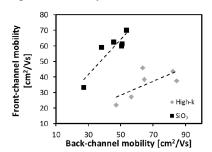


Fig. 7: Front-channel versus back-channel mobility for high-k and  $SiO_2$  splits.