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Low frequency noise assessment in advanced UTBOX SOI n-channel MOSFETs

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1. Abstract

Low frequency noise measurements were performed in n-channel UTBOX transistors fabricated on silicon on insulator (SOI) substrates. The noise spectra contain 1/f and Lorentzian components; it was found that the carrier number fluctuations are responsible for the 1/f noise; the variation of the low frequency noise versus temperature permits to identify traps in the silicon film and to make a correlation between the observed traps and some technological steps.

2. Introduction

The fully depleted (FD) ultra-thin buried oxide (UTBOX) transistors present a growing interest in the development of 16 nm technology node and below, in particular because of the very thin BOX which allows an extra control of the short channel effects due to electrostatic coupling between gate and channel and of the threshold voltage by applying a back bias voltage [1,2].

The low frequency noise measurements versus temperature can be used as a non-destructive device characterization tool in order to evaluate the quality of the gate oxide interface and to identify the traps in the depletion area of the transistors. One of the methods used for material characterization is provided by the study of the generation–recombination (GR) noise, corresponding to a Lorentzian type of spectra and allowing to do the so-called noise spectroscopy when performed as a function of temperature [3,4].

The aim of this work is to investigate the low frequency excess noise sources (1/f and Lorentzian spectra) versus temperature as a diagnostic tool in order to characterize the traps present at the front (back) gate oxide/Si film interface and in the depletion area (Si film) of these advanced n-channel UTBOX devices.

3. Experimental

The tested devices were processed at IMEC in a fully depleted (FD) SOI technology on 300 nm wafers, with various gate lengths (from 55 nm up to 935 nm), fixed gate width (1µm), an equivalent gate oxide thickness (EOT) of the high-k dielectric of 2.6 nm, a BOX thickness of about 18 nm and a buried silicon film thickness of 14 nm. Further processing details can be found in [5].

The low frequency noise measurements were performed directly on wafer-level using a "Lakeshore TTP4" prober. The devices were biased in the linear regime with an applied drain voltage $V_{DS} = 50mV$. At room temperature, the front (back) gate noise were investigated as a function of the front (back) gate voltage V_{GS} (V_{BS}) for a fixed applied $V_{BS} = 0V$ ($V_{GS} = 0V$); the front gate noise measurements versus temperature were carried out at fixed drain current (the front gate voltage was adjusted in order to keep the drain current constant at $I_D = 9\mu A$ for a fixed applied $V_{BS} = 0V$) from 80 K up to room temperature using a step of 10 K.

4. Results and discussion

In general, the low frequency noise observed in the devices can contain a combination of three non-correlated noise sources: white noise, flicker noise (1/f) and Lorentzian noise. The following equation enables to model the frequency dependence of the noise spectral density at the input:

$$S_{V_G}(f) = B + \frac{K_f}{f^\gamma} + \sum_{i=0}^{N} \frac{A_i}{1+\left(f/f_{0i}\right)^2}. \qquad (1)$$

where B presents the white noise level, K_f/f^γ presents the flicker noise (the frequency exponent may deviate from 1 if the trap density is not uniform in depth), and the third term of the equation presents a sum of Lorentzian components, with A_i the plateau value and f_{0i} the characteristic frequency. Typical experimental frequency normalized noise spectra observed in our devices is represented in figure 1, it contain a combination of these three noise sources and can be perfectly modeled by equation (1).

The evolutions of the extracted surface normalized 1/f noise contributions on the total noise of the front gate $\left(K_{f1}\right)$ and of the back gate $\left(K_{f2}\right)$ with the applied gate

overdrives are represented in figure 2. The extracted $K_{f1,2}$ levels seem to be independent of the applied gate voltage overdrive in weak inversion; this suggests that carrier number fluctuations due to carrier trapping in the oxide layer dominate the 1/f noise in weak inversion.

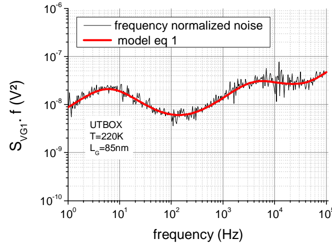

Fig.1: *Modelling of a noise spectrum using equation 1.*

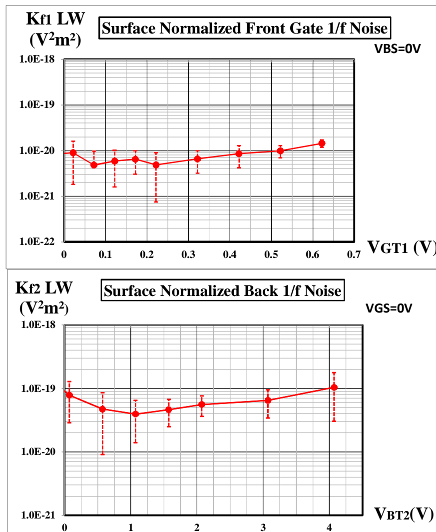

Fig.2: *The extracted surface normalized $K_{f1,(2)}$ levels versus the applied front (back) gate voltage overdrive*

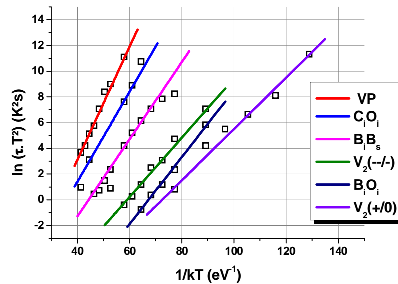

Fig.3: *Example of an Arrhenius plot for UTBOX with physical gate length of 85 nm*
V_2(+/0): *ΔE=0.20 eV, $\sigma_n=10^{-15}cm^2$;* ***V_2(--/-):*** *ΔE=0.23 eV, $\sigma_n=10^{-15}$-$10^{-16}cm^2$;* ***B_iO_i:*** *ΔE=0.26 eV, $\sigma_n=10^{-13}$-$10^{-14}cm^2$.***B_iB_s:*** *ΔE=0.3 eV, $\sigma_n=3.10^{-16}cm^2$.* ***C_iO_i****(0/-): ΔE=0.35 eV, $\sigma_n=10^{-16}cm^2$;* ***VP:*** *ΔE=0.44 eV, $\sigma_n=10^{-14}$-$10^{-15}cm^2$*

Therefore, the carrier number fluctuation model [6] can be used to explain the origin of the noise; and taking into account the coupling effect on the front and back-gate input gate voltage 1/f noise [7], the oxide trap density N_{it} ($eV^{-1}cm^{-3}$) at front and back interface can be evaluated. We found that the back oxide the trap density (about $6 \cdot 10^{17} eV^{-1}cm^{-3}$) is smaller than the front oxide one (which is about $3 \cdot 10^{18} eV^{-1}cm^{-3}$).

Low frequency noise was performed also at constant drain current for the front channel at different temperatures. The characteristic frequency f_{0i} and the plateau value A_i were extracted from the total noise using the model of equation 1. According to [8], if the characteristic frequency of a Lorentzian does not change with the applied gate voltage, this Lorentzian can be assigned to a trap located in the depletion area (Si film). The variation of the characteristic time constant of the Lorentzians (τ) as a function of the temperature allows to plot an Arrhenius diagram; according to [4] from the slope and the y-intercept of the evolution of $\ln\left(\tau T^2\right)$ versus $1/(kT)$ one can extract the energy difference between the appropriate band energy and the trap energy (i.e. $\Delta E = E_C - E_T$) and the capture cross section σ_n of the trap, respectively. The physical nature of these traps can be identified by comparing the energy level and the capture cross section of the traps with data in the literature.
A typical Arrhenius diagram is presented in figure 3. In this example, 6 kinds of traps can be clearly identified. For all studied devices, 6 kind of traps were identified: divacancies V_2(+/0) and V_2(-/--), interstitial boron-interstitial-oxygen complex (B_iO_i), interstitial boron-substitutional-boron complex (B_iB_s), interstitial carbon-interstitial-oxygen complex (C_iO_i) and vacancies-phosphor (VP). The traps related to Boron and Phosphor may be related to the doping implantation.

4. Conclusions

Carrier number fluctuations dominate the 1/f noise for both front and back interface. Taking into account the contribution of both interfaces the interface trap densities were estimated. The quality of the front and back gate oxide interfaces was evidenced by the relatively small values of the oxide trap densities.
The analysis of the temperature evolution of the Lorentzian time constants allowed to identify traps in the silicon film. For all the investigated n-channel UTBOX devices, 6 kinds of traps were clearly identified, and they may relate to the dry-etching process or implantation damage.

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