Study of CCD Transport on CMOS Imaging Technology: Comparison Between SCCD and BCCD, and Ramp Effect on the CTI

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***Abstract*— This paper presents measurements performed on charge-coupled device (CCD) structures manufactured on a deep micrometer CMOS imaging technology, in surface channel CCD and in buried channel CCD mode. The charge transfer inefficiency is evaluated for both CCD modes with regard to the injected charge, and the influence of the rising and falling time effect is explored. Controlling the ramp and especially reducing its abruptness allows to get much lower charge transfer inefficiency in buried CCD mode. On the contrary, we did not observe any effect of the ramp on surface channel CCD mode because of the presence of interface traps at the silicon–oxide interface.**

***Index Terms*— Charge, charge transfer, charge-coupled devices, CMOS image sensors (CIS), deep submicrometer process, transfer inefficiency, trapped charge.**

I. Introduction

CONVENTIONAL charge-coupled devices (CCDs) are systems allowing the charge transfer between devices on a semiconductor material. They have been extensively used for imaging application, like pixel CCD array or TDI sensors [1]–[3]. CCDs use the dedicated processes that allow overlapping of polysilicon gates to achieve very low charge transfer inefficiency (CTI). On the contrary, CMOS processes do not use overlapping, and the gates have to be separated by a minimum gap; therefore, a high-quality CCD structure is challenging to obtain. However, with the scaling down of the CMOS technology, it is now possible to realize very narrow polysilicon gap, and to come close to a true CCD device.

We propose in this paper to realize CCD structures on a deep micrometer CMOS imaging technology, using a gap of 130 nm between adjacent gates. The CTI is studied with regard to the injected charge in surface channel charge-coupled device (SCCD) mode and in buried channel charge-coupled device (BCCD) mode. On one hand we will show the benefit of the buried channel structure, and on the other hand the effect of controlling the ramp of the gate signals.

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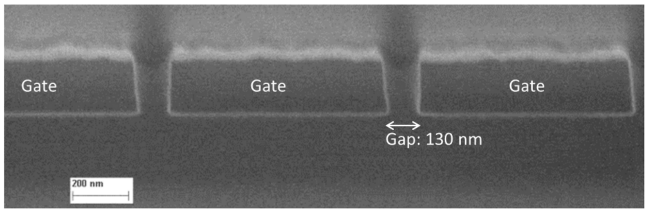

Fig. 1. SEM cross sectional view of a CCD test structure centered on three transfer gates.

The following section presents the tested devices and the experimental conditions. Section III details the CTI and conversion gain factor (CVF) evaluation method used. Section IV gives the experimental results and analyses, for both SCCD and BCCD devices.

II. Experimental Details

CCD test structures are manufactured on a 5 μm epitaxy layer of p-silicon doped at 1.0×10^{15} At/cm^3. The process used is a deep micrometer imaging CMOS process, including pinned photodiode devices. A special option allows the user to draw narrow polysilicon gap until 130 nm, using bottom antireflective coating (BARC) material etching. The gap length between adjacent gates was checked by a FEG-SEM observation in cross section prepared by a Focused Ion Beam (FIB) (Fig. 1).

The CCD test structures are of two types: one has six transfer gates and the other one has 60 transfer gates. Gates are drawn 0.8-μm wide and 1.0-μm long with a gap of 130 nm. Fig. 2 shows simplified cross sections of a CCD test structure.

The CCD test structures are realized with two options. In the first one, no implant is executed below the poly gates; the charge transport is therefore operated in a surface CCD mode. In the second one, a special implant is processed under the gates in order to get a buried CCD mode. This special implant was developed with the help of Synopsys TCAD tool in a way to get a buried phosphorus profile which can be depleted [Fig. 3(a)]. Considering these conditions, the buried phosphorus implant simulated has a concentration of 6×10^{16} P.cm^{-3} at 70 nm under the surface.

These CCD test structures are operated in a three-phase mode (Fig. 4), which means that three different signals control

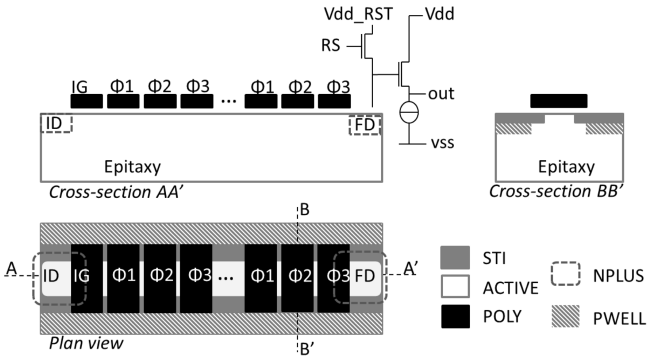

Fig. 2. Cross sectional views of a CCD test structure and corresponding designed plan view.

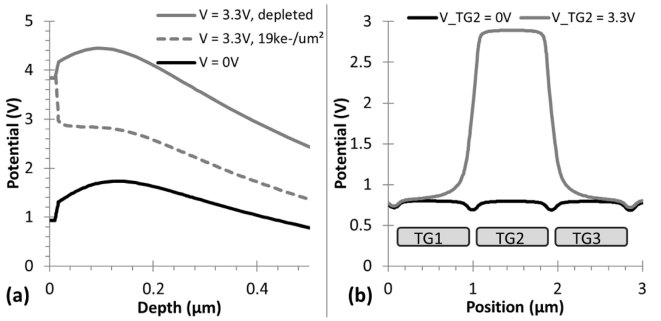

Fig. 3. (a) TCAD simulation of the potential distribution in BCCD below one gate polarized at 0 V, 3.3 V depleted or 3.3 V with stored electrons. (b) TCAD simulation of the potential profile 10 nm under the oxide, in the SCCD mode. V_TG1 = V_TG3 = 0 V.

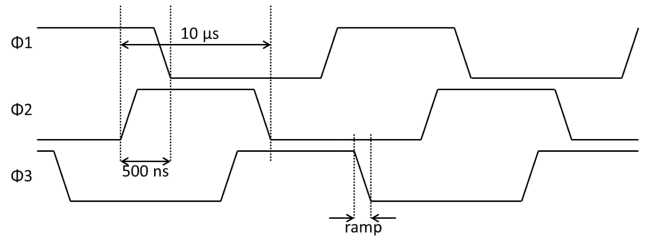

Fig. 4. CCD timing diagram showing the ramp and the overlap between two phases.

all gates. Charge are injected via an injection drain and an injection gate, using the fill-and-spill technique [4], [5]. The gate control signal is swung between 0 and 3.3 V relative to the substrate, according to the CMOS technology. Under these conditions, the surface is not inverted at the low transport voltage. Fig. 3(b) shows a simulation of the potential profile 10 nm under the gate in the SCCD mode.

All measurements were done with an overlapping of the clock signal of 500 ns between two phases, including ramps (Fig. 4).

The clock signal is generated by a Tektronix DG2020A data generator, and the transfer gates are controlled either by the Tektronix, or by Arbitrary Waveform Generator AWG Keithley 3390 elements. The floating diffusion (FD) of the CCD structure is read by a standard readout chain, as can be found in CMOS pixel array [6]. The output signal is monitored on a digital oscilloscope.

III. CTI and CVF Evaluation Method

A. CTI Evaluation Method

The CTI is defined as the fraction of charge lost from one phase gate to the adjacent phase gate in a charge transfer device. It characterizes the transfer quality of the device, and must be as small as possible. While CTI less than 10^{-5} [7], [8] could be obtained in real CCD device, it is much more tricky to get very good CTI on CMOS technology. The reason is the trapping of carriers at interface states and the gap between adjacent gates leading to energetic barrier [9].

The CTI parameter is estimated considering the number of injected charge Q_{inj} compared with the number of transferred charge Q_{tr}, for a given number of n transfers

$$\text{CTI} = \frac{1}{n} \times \frac{Q_{\text{inj}} - Q_{\text{tr}}}{Q_{\text{inj}}}. \tag{1}$$

CTI may be evaluated calculating the injected charge and measuring the transferred charge. Injected charge are estimated using straightforward formula, knowing the gate dimensions and the applied voltage [5]. Transferred charge are estimated from the potential shift of the floating node ΔV_{out}, and knowing the charge to voltage conversion gain (CVF) of the read out chain

$$Q_{\text{tr}}\,(e-) = \frac{\Delta V_{\text{out}}}{\text{CVF}}. \tag{2}$$

More accurate methods have been developed, like extended pixel edge response (EPER), first pixel response, or with an X-ray source, and are commonly employed to characterize CCD architectures [10]. These methods require a high number of transfer gates to measure the CTI.

In our case, we have used a different way to evaluate the CTI. We made the assumption that the CTI is constant over the entire CCD. One CCD structure is made of six transfer gates and is used as a reference of transferred charge

$$Q_{\text{tr\_6G}} = \frac{\Delta V_{\text{out\_6G}}}{\text{CVF}}. \tag{3}$$

A second CCD structure has 60 gates and gives a second transferred charge number, related to a higher number of transfer gates

$$Q_{\text{tr\_60G}} = \frac{\Delta V_{\text{out\_60G}}}{\text{CVF}}. \tag{4}$$

CTI is then calculated from the value of transferred charge of these two structures, via

$$\text{CTI} = \frac{\Delta V_{\text{out\_6G}} - \Delta V_{\text{out\_60G}}}{\Delta V_{\text{out\_6G}}} \frac{1}{(n_{60G} - n_{6G})} \tag{5}$$

where n_{6G} and n_{60G} are, respectively, the transfer number in the CCD test structure containing six transfer gates and 60 transfer gates. We assume that gate dimensions of structures with 6 and 60 gates are physically identical in a way that it does not affect the CTI calculation. This method takes advantage to avoid the calculation of injected charge and the measurement of CVF, which both introduce artifacts on the

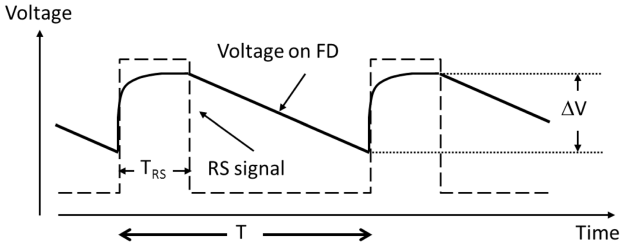

Fig. 5. Principle of the CVF measurement; measured elements are the voltage drop ΔV and the average current I_{ave} knowing the signal period T.

final result. In addition, the extraction of ΔV_{out} is averaged on more than 200 samples, and the standard deviation σ given by the oscilloscope is used to calculate the error made on CTI measurement by means of the following equation:

$$\text{Err}_{\text{CTI}} = \frac{\sigma_{6G} + \sigma_{60G}}{\Delta V_{\text{out\_6G}}\,(n_{60G} - n_{6G})}. \tag{6}$$

In all measurements we did, the CTI is evaluated for different charge injections via the injection gate control.

To confirm and compare results with other works, the CTI was also evaluated using the EPER method [10], [11], although our longer CDD structures have only 60 gates. The EPER gives a CTI based on the number of deferred charge, while our method gives a CTI depending both on deferred and lost charge. Consequently, one should expect a higher CTI in our case compare with the EPER one.

B. CVF Evaluation Method

Using (5) allows obtaining a value of the CTI without the need to know the value of the CVF. However, measurements of the CVF have been performed to be able to get the variation of the CTI with regards to the number of injected charge. To do so, all transfer gates are off in order to isolate the CCD part to the readout part. In addition, the CCD structure is uniformly illuminated which creates photoelectrons in the FD. When RS gate is activated (Fig. 2), a current flows in the RS transistor drain. It represents the current necessary to reset the floating node and is related to the voltage drop due to illumination by (Fig. 5)

$$I = \frac{q}{\text{CVF}} \frac{\Delta V}{T_{\text{RS}}} \tag{7}$$

where q is the elementary charge, CVF is the conversion gain, ΔV is the voltage drop, and T_{RS} is the time during when RS transistor gate is activated. Actually, the average current I_{ave} is measured during the signal period T, which is equivalent to the measurement of the current I during the reset time T_{RS}.

Using different illumination levels yields to different voltage drops and different drain currents, allowing to get a measurement of the CVF more accurate (not influenced by leakage currents), as shown in Fig. 6 [12].

The CVF is therefore extracted from the slope of the curve $\Delta V(I_{\text{ave}})$ using (7).

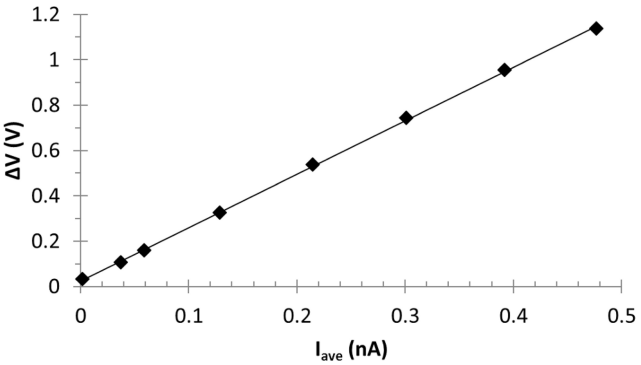

Fig. 6. Voltage drop ΔV against the average current I_{ave} for different illumination levels. The CVF is deduced from the slope.

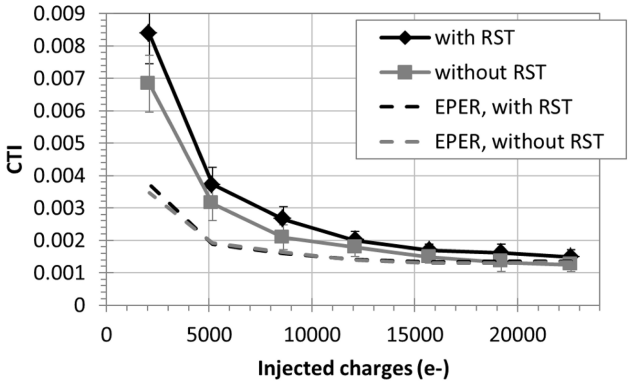

Fig. 7. CTI against charge injection in the SCCD structures. A reset procedure is applied on the structure before injecting and transferring charge (with RST) or is not applied (without RST). The CTI is evaluated using our method and the EPER method.

IV. Experimental Results and Discussion

A. SCCD Transport

1) Use of Digital Command for the Gate Control: The Tektronix data generator controls all gates. Rising/falling edges applied are less than 10 ns according to oscilloscope monitoring, and the overlap between two transfer gate signals is 500 ns including the rising/falling edges. The structures are evaluated using two methods; in one case a reset procedure is applied to the CCD structure before charge injection and transfer, and in the other case the reset procedure is not applied. The reset procedure is to empty the entire CCD structure, by keeping "on" the reset transistor (RS) during a complete CCD cycle. The CTI is measured with regard to the injected charge and is shown in Fig. 7.

As it can be seen on the figure, the lower is the number of injected charge, the higher is the CTI. The increase of CTI measured by our method is even higher when less than 5000 electrons are transferred. This trend is known in CCD [10], [13]–[15], and is mostly attributed to interface traps. Indeed, smaller amount of charge packets have a lower charge density, and therefore the smaller packets interact with more traps per electron of signal, leading to an increase of the CTI. This is also shown by a TCAD simulation in Fig. 8, where the structure is simulated in 2-D, with

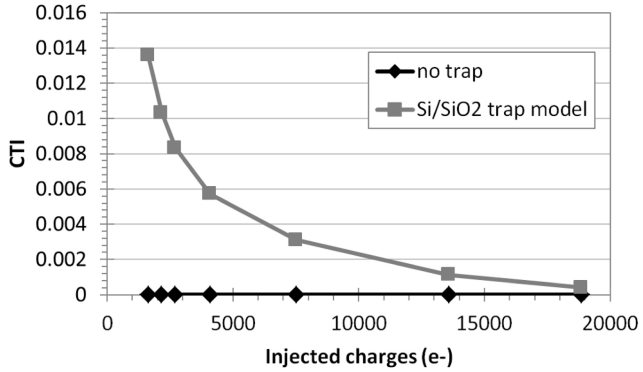

Fig. 8. TCAD simulation of the CTI against injected charge for a six transfer gates structure with an injection gate and an injection drain. CTI is measured by comparing the injected charge with the stored charge under the last gate. In the case of the interface trap model at the Si/SiO_2 interface, the acceptor concentration is 5×10^9 cm^{-2} and the capture cross section is 1×10^{-15} cm^2.

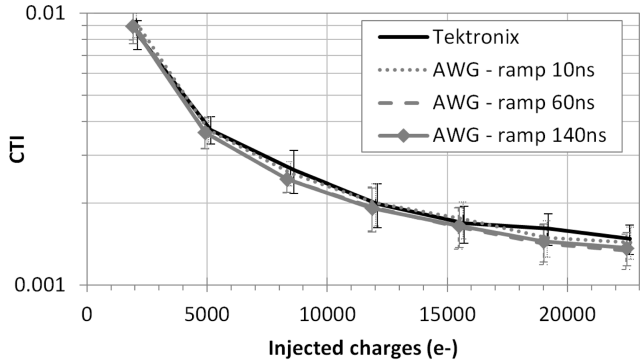

Fig. 9. CTI against charge injection in the SCCD structures, with a reset procedure before charge injection. Transfer gates are controlled by the Tektronix data generator or by Keithley AWG with three different rising or falling edges. The CTI is evaluated using our method.

1.0-μm-long transfer gate. Without trap model, CTI is ideally null. Using a Si/SiO_2 interface trap model CTI is showing a more realistic trend, which means that it increases with the diminution of injected charge.

However, this behavior might be also attributed to other factors [16]–[18], like:

1) silicon bulk defects;
2) weak fringing fields;
3) potential barrier between gates due to the polygap.

As our device is realized on an epitaxy, one may suppose that the crystalline quality is not degraded by a significant presence of defects and does not affect the transfer efficiency. The fringing field drift is coming from the potential difference between adjacent gates, and it generally dominates the end of the transfer. An approximate expression for the fraction of charge remaining under the gate after the transfer time due to fringing field drift is given by [18]

$$\varepsilon(t) = \exp\left(-\frac{t}{\tau_{\text{ff}}}\right), \quad \tau_{\text{ff}} = \frac{L}{\mu_n E_{\text{ff}}} \tag{8}$$

where t is the transfer time, τ_{ff} is the fringing field induced drift lifetime, E_{ff} is the fringing field, μ_n is the average electron mobility in the channel, and L is the gate length. Applied here, it yields a fringing field induced drift lifetime of 2 ps in SCCD mode, which gives a negligible contribution to the CTI. Therefore, the main contributors to the CTI increase at low charge injection level are most likely the interface traps and the energetic barrier between gates.

If we compare the case with and without reset procedure before charge injection, we see that without reset the CTI is slightly reduced. This trend is enhanced when only a few electrons are injected, because when the reset is not applied before the charge injection, some interface traps are already occupied and therefore do not capture signal electrons. This result shows that interface states play a major role in the increase of CTI with regards to the decrease of charge injection.

Fig. 7 also shows the CTI evaluated by means of the EPER method. This method is showing the deferred charge and not the lost charge and consequently gives better CTI. The comparison between the two methods giving the CTI shows that the transfer inefficiency is dominated by deferred charge at high injection level, and by lost charge (interface states) at low injection level.

An average CTI based on our measurement method is extracted for more than 5000 electrons and gives $\text{CTI} = 2,2 \times 10^{-3}$ with reset and $\text{CTI} = 1,8 \times 10^{-3}$ without reset. These CTI values are comparable with other devices found in the literature, like in the papers by Borg *et al* [19]. ($5.7 \times 10^{-4} < \text{CTI} < 7 \times 10^{-3}$) and Fife *et al*. [20] ($\text{CTI} = 1 \times 10^{-3}$).

2) Use of AWG for the Gate Control: To investigate the effect of the rising or falling edges on the CTI, the same experiment was done with AWG Keithley controlling the transfer gates. Rising or falling edges are set and monitored on oscilloscope from 10 to 140 ns, and the overlap between two transfer gates signal is kept at 500 ns (Fig. 4). Fig. 9 shows the obtained results.

Only a small effect is visible for a high number of transferred charge. CTI is very slightly reduced when the rising or falling edges are 60 and 140 ns. Interface traps still have a strong effect on the CTI, and the impact of longer ramp is only visible on large amount of charge.

B. BCCD Transport

1) Use of Digital Command for the Gate Control: The BCCD structures are identical to the SCCD structures, except the buried channel implant below the transfer gates from the injection drain to the floating diffusion. As in the SCCD test structures, the devices are evaluated using two methods; in one case a reset procedure is applied to the CCD structure before charge injection and transfer, and in the other case the reset procedure is not applied (Fig. 10).

Contrary to the SCCD structures, the BCCD structures show a slight decrease of the CTI with the diminution of injected charge for more than 5000 electrons, using our CTI measurement method. This shows the buried channel benefit, which means that charge are carried away from the silicon–oxide interface and much less charge are captured by

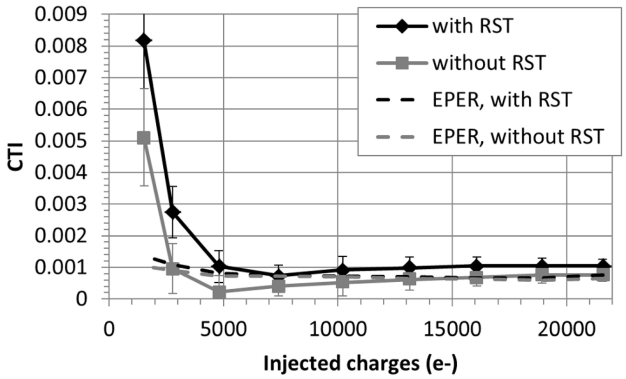

Fig. 10. CTI against charge injection in BCCD structures. A reset procedure is applied on the structure before injecting and transferring electrons (with RST) or is not applied (without RST). The CTI is evaluated using our method and the EPER method.

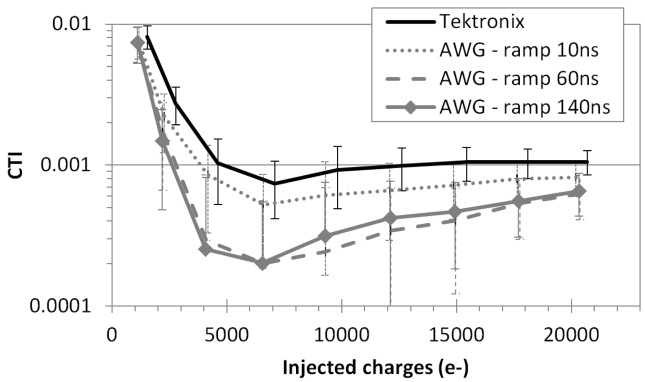

Fig. 11. CTI against charge injection in the BCCD structures with a reset procedure before charge injection. Transfer gates are controlled by the Tektronix data generator or by Keithley AWG with three different rising or falling edges. The CTI is evaluated using our method.

interface traps. The higher is the amount of injected charge; the closer is the SCCD CTI to the BCCD one. The reason is the increase of the charge packets, which leads to a volume extension and a rapprochement between the surface and the charge packets. However, as it can be seen for less than 5000 injected electrons, an important increase of the CTI with the decrease of injected charge takes place. The root cause of this trend might be the interface traps on the STI oxide along the channel, and probably the energetic barrier between gates. Indeed, in this particular design, STI edges are not passivated and are in contact with the buried channel (Fig. 2, crosssection BB'), which create interface traps. This is also confirmed by the curves showing the CTI measured by the EPER method. In this case, the CTI measurement does not consider the trapped charge, and one cannot see any strong increase of the CTI for less than 5000 injected electrons. A limitation due to weak fringing fields is excluded as we found a fringing field drift lifetime of 30 ps in BCCD mode, yielding again to a CTI contribution because of negligible fringing field.

An average CTI based on our measurement method is extracted for more than 5000 electrons and gives $\mathrm{CTI} = 9,8 \times 10^{-4}$ with reset and $\mathrm{CTI} = 5,7 \times 10^{-4}$ without reset. The CTI is well decreased by the use of a buried channel.

2) Use of AWG for the Gate Control: The effect of the rising or falling edges on the transfer quality is investigated with AWG Keithley wave generators. The measurements performed on the buried channel structures are shown in Fig. 11.

In the case of the buried transport, the effect of the rising or falling edges on the transfer efficiency is strongly visible. For more than 5000 injected electrons, the use of an AWG and especially the slow ramp improve the transfer efficiency and low value of CTI may be obtained ($\mathrm{CTI} = 2 \times 10^{-4}$). Similar results are obtained with 60 and 140 ns ramps. However, the error made during the measurement might hide a small difference between the two ramps. The higher is the amount of charge, the higher is the CTI. However, for less than 5000 electrons interface traps strongly impact the transfer and the CTI increases until near 0.01. One can deduce here that slow rising or falling edges improve the buried transport and help to go through the barrier pocket between gates, but do not influence the trapping mechanism of interface traps. Average CTI are extracted for more than 5000 electrons and gives very good value: $\mathrm{CTI} = 7.1 \times 10^{-4}$ (ramp 10 ns), $\mathrm{CTI} = 4.1 \times 10^{-4}$ (ramp 60 ns), and $\mathrm{CTI} = 3.8 \times 10^{-4}$ (ramp 140 ns).

V. Conclusion

We have studied in this paper CCD structures manufactured on a deep micrometer CMOS imaging technology with gaps of 130 nm between transfer gates. In surface channel mode, the CTI obtained are comparable with other works and usable for a CCD device. The transfer is strongly impacted by interface traps for a low level of injected electrons, and adjustment of AWG rising or falling edges do not have any impact on it. However, the use of a buried channel device improves significantly the transfer efficiency. We found that the CTI of BCCD structures were decreasing with the reduction of the amount of injected electrons until $\mathrm{CTI} = 2 \times 10^{-4}$, which is a very good result. Moreover, we showed that slow rising or falling edges help to go through energetic barriers between gates in the BCCD mode. As with the SCCD structure, for small charge packets, the transfer is most likely impacted by interface traps and the CTI increases a lot. Further work is necessary, in particular in optimizing the design to limit the interface trap impact. For example, one could think about passivating the STI sides with Pwell implant, or shifting the STI away from the CCD canal with the restriction to draw poly contact on active area.

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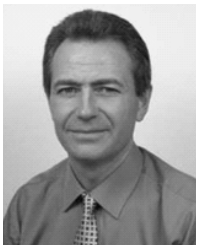

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