Effect of Aging on Power Integrity and Conducted Emission of Digital Integrated Circuits

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Abstract *— Recent studies have shown that integrated circuit aging modifies electromagnetic emission significantly. The proposed paper aims at evaluating the impact of aging on the power integrity and the conducted emission of digital integrated circuits, clarifying the origin of electromagnetic emission evolution and proposing a methodology to predict this evolution. On-chip measurements of power supply voltage bounces in a CMOS 90 nm technology test chip and conducted emission measurements are combined with electric stress to characterize the influence of aging. Simulations based on ICEM modeling modified by an empirical coefficient to model the evolution of the emission induced by device aging is proposed and tested.*

Keywords — Integrated circuits, power integrity, conducted emission, accelerated aging, ICEM modeling.

1 INTRODUCTION

Recently, many publications have forecast a decrease of new CMOS technology device lifetime down to few years [1], with anticipated appearance of hard or soft failures due to wear-out mechanisms (e.g. hot carrier injection (HCI), negative bias instability (NBTI), electromigration…) [2] [3]. The drift of the electrical characteristics of semiconductor devices have direct consequences on integrated circuit (IC) electromagnetic emission (EME) and power integrity (PI) [4]. The management of both constraints constitutes a serious challenge for electronic industry to ensure a reliable operation of digital circuits and comply with electromagnetic compatibility (EMC) requirements. Recently, some publications have shown experimentally that accelerated aging tests such as high or low temperature operating life, thermal cycling, or electrical overstress induce a significant variation of EME produced by power supply units [5], high side switch devices [6] digital circuits or I/O buffers [7]. However, these studies do not clarify the origins of EME changes and do not address the modeling and prediction issues.

This paper intends to clarify the impact of IC aging on PI and conducted emission (CE) experimentally and by simulation. A test chip designed in Freescale CMOS 90 nm technology, which includes a digital core and on-chip sensors dedicated to the measurement of power supply ripple, has been developed to characterize the evolution of PI vs. time. In order to explain the effect of IC aging on PI and CE, an equivalent model of the circuit based on the Integrated Circuit Emission Model (ICEM) approach [8] is developed. A simple empirical coefficient is included in the model to predict the evolution of EME of ICs with time.

The paper is organized as follows: after a description of the circuit under test, the on-chip sensors and the experimental set-up, the measurement results of the evolution of the power supply voltage bounces and CE are presented and discussed. Then, the proposed modeling approach of the circuit PI

and CE is described and, finally, simulation and measurement results are compared in order to validate both our hypothesis about PI and CE evolution with time and the proposed modeling method.

2 TEST CHIP AND EXPERIMENTAL SET-UP PRESENTATION

2.1 Test chip description

A dedicated test chip has been designed in Freescale CMOS 90 nm technology for IC emission and susceptibility modeling, and characterization of aging impact on EMC of ICs. In particular, the test chip includes a digital core with a dedicated power supply voltage equal to 1.2 V. The structure of the core is a basic 100-stage shift register, synchronized by a 40 MHz clock, as described in Fig. 1.

2.2 On-chip voltage sensor

In order to monitor the voltage drops on the power supply of the digital core, an on-chip voltage sensor is placed along the power supply rail of the core. This sensor is able to acquire the waveform of signals on non accessible nodes with a precise time resolution (up to 15 ps). Its analog bandwidth is equal to 10 GHz. Its principle and its implementation in the test chip are explained in [9]. In order to prevent noise coupling with the digital core, the designed sensor has a dedicated power supply and is isolated from the IC substrate by a buried N layer. Due to its small input capacitance (4 fF), the sensor is not intrusive and does not influence the circuit under test. Although the electrical stress applied to the circuit under test can partially alter the performances of the sensor, it can be recalibrated before any measurements. The calibration process is necessary to compensate effects of imperfections due to non ideal behavior and mismatches on voltage and frequency responses.

2.3 Description of the experimental set-up

The experiment is based on a measure-stress-measure flow (Fig. 2), which consists in applying electrical stress on the circuit under test and interrupting the stress during short periods regularly for

characterization purpose. With this procedure, the characteristics of the circuit are monitored at various degrees of aging. The choice of stress conditions (stress voltage and duration) is based on a preliminary failure analysis of MOS devices developed in this technology [10] [11]. At ambient temperature, for DC stress voltages ranging from 3 to 4 V and applied between the drain and source of NMOS and PMOS devices, significant degradations of threshold voltage and carrier mobility are induced either by HCI or NBTI after several hundreds of seconds. The amount of degradation and the activated degradation mechanisms are related to stress voltage, duration, transistor geometry and gate oxide thickness. HCI is activated in NMOS devices for large drain-source voltages (between 3 V and 4 V). The gate-source voltage is selected to optimize the current injected in the substrate, which is an effect of HCI. The Ids (Vds;Vgs) characteristic of the tested NMOS device is measured regularly during the stress to extract the increase of threshold voltage and the decrease of carrier mobility. NBTI arises in PMOS devices for negative gate-source voltage (between 3 V and 4 V). The drain, the source and the bulk are set to the same potential. The Ids (Vgs) characteristic of the testes PMOS device is measured regularly during the stress to extract the increase of threshold voltage.

In a circuit, degradation mechanisms such as NBTI and HCI coexist and participate to the change of circuit performances. These characterizations are important for failure analysis at circuit level because the voltage conditions which activate the degradation mechanisms can be determined. For the digital core under test, a 3.6 V electrical stress is applied on the power supply during 120 minutes in order to validate the influence of the stress voltage on PI and CE changes. This stress activates NBTI on PMOS devices of digital gates if their output is set to logical state ‘1’. If the inverters of the clock tree are considered, NBTI is activated half of the stress time. HCI is activated on NMOS devices only during logical state transitions.

The measurements of power supply voltage fluctuations with the on-chip sensor are performed after

each stress interval. The sensor is not supplied during stress phases in order to limit its aging. Recalibration is done after each stress period, although experimental characterizations have not shown any significant degradation of the sensor. In addition, conducted emission measurements according to the "1 Ω" method [12] are performed after each stress interval, in order to monitor the variations of the transient current that returns to the ground. The conducted emission measurements are done on a dedicated board which is not stressed to prevent from any changes of the 1 Ω probe characteristics. During power supply voltage fluctuations and conducted emission measurements, only the clock tree is activated in order to keep a simple and repetitive core activity.

All the experiments have been repeated on several samples to ensure that similar results are obtained. Nevertheless, the uncertainties linked to the process dispersions which affect the circuit are not taken into account in this study.

3 EXPERIMENTAL RESULTS: EVOLUTION OF POWER INTEGRITY AFTER ELECTRICAL STRESS

3.1 Initial measurement of power integrity

Fig. 3 presents the power supply voltage fluctuations produced by the digital core activity measured by the on-chip sensor. Positions of clock edges are indicated. Rapid drops appear at each clock switching. These events are linked to the rapid current demand from every gate and latch of the core. A damped oscillation with a pseudo-period equal to 4.5 ns follows the first rapid current impulsion. This oscillation is linked to the anti-resonance due to the equivalent parallel LC circuit formed by the on-chip capacitor and parasitic inductances associated to power and ground package pins [13]. Similar voltage fluctuations are also measured on the ground node of the circuit.

3.2 Impact of electrical stress on digital core power integrity

After stress, the core remains operational and the average current consumption has not changed.

However, the core timing characteristics have evolved. A specific part of the core has been designed to measure the propagation delay through one D-latch and 100 inverters. The propagation delay through the core after stress increases up to 31 % depending on the stress duration. The electrical stress applied on core power supply accelerates wear-out mechanisms such as HCI for NMOS devices and/or NBTI for PMOS devices, which lead to an increase of the propagation delay of each gate of the core.

Fig. 4 presents the power supply voltage bounces measured by the on-chip sensor before and after 3.6 V stresses. A -30 % reduction of the peak-to-peak amplitude is observed. The waveform of the signal is also modified. The first peak is less steep and the period of the resonance oscillation has not changed. Its amplitude is reduced, but it is still damped at the same rate. This observation indicates that the package inductance, the equivalent capacitance of the digital and resistance linked to the power distribution network (PDN) have not been affected by the electrical stress significantly. This hypothesis is confirmed by impedance measurement of the PDN with a vector network analyzer, as shown in Fig. 5. Whatever the electrical stress amplitude and duration, the impedance of the circuit power distribution network remains constant over a large frequency range.

From these experimental results, the following hypothesis can be proposed to explain the evolution of power integrity of the circuit: the reduction of power supply voltage bounce is only linked to the change of transient current produced by the core activity. Wear-out mechanisms accelerated by electrical stress have reduced mobility of carrier in MOS devices so the switching transient current has been spread.

3.3 Impact of electrical stress on digital core conducted emission

Fig. 6 presents the evolution of the spectrum of conducted emission of the digital core during the exposition to the 3 V electrical stress. Only the spectrum envelop is shown to facilitate the

comparison between the different curves. The result shows a time-dependent gradual reduction of the conducted emission spectrum, which is more important at high frequency. Above 400 MHz, the emission level decrease exceeds 5 dB after a 3 V stress applied during 240 minutes. Above 1 GHz, the reduction of the CE level reaches 15 dB.

This experimental result confirms the previous hypothesis about the effect of the electrical stress on the PI: the degradation mechanisms accelerated by the electrical stress not only reduces the amplitude of the transient current produced by the circuit activity, but also spread it because of a slowing down of the circuit. The next part intends to validate the proposed explanation about PI and CE evolution by simulation and thus to propose a method to predict the amount of variation of emission due to circuit aging.

4 MODELING OF DIGITAL CORE AGING EFFECT ON POWER INTEGRITY AND CONDUCTED EMISSION

4.1 Emission model construction and validation

The EME model is based on ICEM approach [8]. The model includes two main parts: the internal activity (IA) block which models the transient current produced by circuit operation, and the power distribution network (PDN) which models the filtering effect of the transient current due to IC and package. Fig. 7 presents a simplified structure of the ICEM model of the digital core.

A linear model based on an equivalent RLC circuit is proposed for the PDN. The parameters of the model are extracted from measurements. The passive element values are fitted from an impedance measurement between Vdd and Vss pins of the digital core made with vector network analyzer, as shown in Fig. 5. A very simple approach is used for IA modeling: two triangular waveform current sources describe the current produced at each clock edge. They are associated to one activity state of the core. Three parameters describe the current pulse waveform: the amplitude Δi, the rise and fall

times Tr and Tf. Even though such a waveform is quite simplistic, it provides a good estimation of the actual current waveform which can be tuned without a precise analysis of the circuit power consumption. Initially, the IA parameters are extracted from a SPICE transient simulation on the core model. Then, they are tuned in order to fit the simulation results on PI measurements done on a "fresh" device. As only the clock tree of circuit is activated, the circuit activity is simple and periodic. Only one IA block is necessary to model the current produced by the clock tree switching.

SPICE transient simulations are performed to compute the waveform of the power supply and the spectrum of the conducted emission of the digital core from the ICEM model. Fig. 8 presents a comparison between the measurement and the simulation of the power supply voltage bounce before electrical stress. The simulated waveform is similar in term of peak-to-peak amplitude, pseudo-oscillation period and damping. Although the correlation between measured and simulated curves is not totally perfect, the model offers a sufficient accuracy for the aim of the study. A better correlation would rely on a more complex transient current waveform, extracted from a precise analysis of the power consumption of the digital core.

Fig. 9 presents a comparison between the measured and simulated spectra of the core CE before electrical stress. The correlation between measurement and simulation is also acceptable up to 1 GHz. Extending the validity range of the model requires a more complex model of the PCB and IC substrate coupling. However, as the noise produced by the circuit becomes negligible above 1 GHz, the model precision is enough for the rest of the study.

4.2 Modeling of degradation mechanisms induced by electrical stress

Continuous electrical stresses have been carried on 90 nm transistors and have shown that HCI and NBTI were activated on NMOS and PMOS transistors respectively, and were dependent on the stress voltage [11]. Both degradation mechanisms are activated in the digital core by the large voltage

amplitude applied on the power supply. However, the contribution of the PMOS degradation on the PI and CE evolution is predominant. It can be verified by a SPICE simulation of the digital core with a modified model of PMOS transistors which takes into account NBTI effect. In the rest of the study, only the NBTI on PMOS transistor will be considered. NBTI is activated when a negative gate-source voltage is applied and leads to an increase of the threshold voltage V_{TH} of PMOS transistor and thus a reduction of the saturation current. Fig. 10 presents the experimental characterization of the PMOS transistor V_{TH} evolution with time when a constant gate-source voltage is applied. Two stress voltages ware applied: 1.2 V and 3.2 V. The time evolution of V_{TH} can be estimated by a power law model given by equation (1), where A and γ are fitting coefficients [14].

$$\Delta V_{TH}(\%) = A \times t^{\gamma} \quad (1)$$

The effect of NBTI can be taken into account in a transistor model such as BSIM4 by changing parameters which deal with the threshold voltage [15]. The modeling of threshold voltage is complex and depends on numerous parameters, such as the substrate bias, channel geometry, doping profile and gate-oxide thickness [16]. Changing the parameter V_{TH0}, which defines the threshold voltage for a long channel without substrate bias, provides a simple method to model NBTI effect. Thus SPICE simulations can be done to predict the evolution of IC transient current vs. the V_{TH} drift. If the models of time evolution of V_{TH} such as shown in Fig. 10 are known, the evolution of IC transient current vs. stress time can be estimated. For example, in this CMOS technology, applying a 3 V stress for 4 hours induces an increase of V_{TH} of 19 %. SPICE simulations done on the digital core model with a modification of PMOS V_{TH} model leads to a division by 2 of the transient current amplitude and a spreading of the current peak.

4.3 Integration of aging in ICEM model

In order to take into account the aging of the circuit in the ICEM model, the following simple

methodology is proposed. The methodology relies on the assumption that the charge transfer associated to each gate switching does not change after stress. Although degradation mechanisms can increase leakage current and thus modify the dynamic current consumption, the measurement of average current consumption of the circuit does not evolve after stress, which confirms the validity of the hypothesis. Only three parameters of the equivalent current sources in IA block are changed to spread the current pulse created by the digital core: the rise and fall times Tr and Tf of the current pulse are increased while its amplitude Δi is reduced. As the charge transfer associated to each gate switching does not change after stress, the evolution of these parameters must ensure that transient current integration over time remains constant. Their evolution is governed by an empirical coefficient δ called “degradation ratio”, as shown by equations (2) and (3). δ equal to 0 means that the digital core is not degraded and the current pulse is not spread. If δ increases, a larger amount of degradation is considered and the current pulse is spread. In our ICEM model, the degradation ratio is applied on both current sources of the IA block symmetrically.

$$\Delta i_{stress} = \Delta i_{initial}(1-\delta), \quad 0 \le \delta \le 1 \quad (2)$$

$$t_{r\ stress} = \frac{t_{r\ initial}}{1-\delta}, \quad 0 \le \delta \le 1 \quad (3)$$

4.4 Simulation of electrical stress impact on power integrity

By simulation, the effect of δ on the PI can be studied. Fig. 11 presents the evolution of the peak-to-peak amplitude of the power supply bounce when δ is increased in both current sources. The result confirms that the power supply bounce is reduced when the current pulse is spread. However, we need to confirm that our approach is able to model the evolution of the power supply voltage waveform by a comparison with the on-chip measurements done in stressed cores.

Except if information about transistor degradation is available, the coefficient δ value for a given amount of stress is unknown initially. However, the curve shown in Fig. 11 can help us to choose a

reasonable value to fit with EME measurement. From on-chip measurement results, a value of δ is selected to obtain the same voltage fluctuation amplitude. Fig. 12 presents the comparison between the measurements and simulations of the power supply voltage bounces before and after a 120 minutes 3.6 V electrical stress. The coefficient δ is set to 0.58 to model the effect of the stress in the ICEM model. The correlation between measurement and simulation curves is acceptable. The ICEM model modified by the empirical degradation ratio is able to reproduce the evolution of the power supply voltage bounce with a reasonable accuracy.

4.5 Simulation of electrical stress impact on conducted emission

In order to evaluate the relevance of our prediction methodology, the conducted emission of the core after a 120 minutes 3.6 V electrical stress is simulated with the modified ICEM model. The degradation ratio value is also set to 0.58. Fig. 13 presents the comparison between measurement and simulation results which are in a good agreement up to 1 GHz. The simulation reproduces the observed reduction of the CE spectrum at high frequency with a good precision.

The ICEM model is reused to simulate the effect of a different value of stress voltage. In Fig. 14, the measurement and the simulation of the evolution of the CE spectrum with time are compared when the core is exposed to a 3 V stress. According to the measured power supply voltage bounces and the graph presented in Fig. 11, the degradation ratio values are 0.4 and 0.5 for 180 and 240 minutes respectively. The model is able to predict with a quite good accuracy the time-dependent reduction of the CE spectrum up to 1 GHz.

4.6 Prediction of the evolution of the degradation ratio

The prediction of the evolution of EME of an IC with ICEM relies on an accurate evaluation of the degradation ratio. It can be extracted from data about transistor degradation mechanisms and an electrical model of the circuit to simulate how the transient current is spread. In this case study, the

experimental data about NBTI helps us to evaluate the threshold voltage increase vs. stress time, for a given electrical stress condition. SPICE simulations on the digital core netlist are performed to estimate the degradation ratio evolution vs. the stress time, for stress voltage equal to 1.2 V and 3.2 V, which is plotted in Fig. 15.

For example, according to Fig. 10, a 3 V stress applied for 4 hours leads to an increase of V_{TH} of 19 %. SPICE simulation of the digital core shows that the transient current amplitude is divided by 2 while its duration is nearly multiplied by 2. This current spread can be characterized by a degradation ratio equal to 0.5, which correlates with the choice made in the previous part to simulate the evolution of CE. According to Fig. 15, under a nominal power supply voltage equal to 1.2 V, the same variation of V_{TH} and, thus the same PI and CE change, would be obtained after 6×10^7 s, i.e. nearly 2 years.

5 Discussion and Perspectives

The simulation results confirm our hypothesis about the origin of the evolution of the PI and CE after circuit aging. The degradation mechanisms induced at MOS device level, especially the NBTI mechanism, tend to spread the current pulses produced by the switching of the gates of the digital circuit. It leads both to a decrease of the power supply voltage bounce and a reduction of the conducted emission spectrum, especially the contribution of high frequency harmonics. Moreover, these results demonstrate that the evolution of the power integrity can be predicted by a correct modeling of the change of the circuit current consumption. A complex methodology based on an accurate prediction of the power consumption from the circuit netlist combined with the modeling of MOS device degradation mechanisms could provide an accurate estimation of the evolution of the power supply voltage bounce. However, in this paper, it has been demonstrated that a more simple and non confidential approach based on an ICEM model can also a reasonable estimation of the evolution of the parasitic emission and power supply voltage bounce. A single empirical parameter

called degradation ratio is introduced in the model to take into account the current spread induced by the IC aging. This parameter can be estimated from data about degradation mechanisms in the considered technology and the electrical model of the tested circuit.

Modeling IC emission and integrating the effect of aging is fundamental in order to predict the emission at a larger scale, e.g. a board which integrates several ICs and numerous passive devices, whose characteristics may change with time. This work have several perspectives: firstly, validating the proposed method on more complex circuit and verify if a unique degradation ratio is enough to predict EME evolution with ICEM model; secondly, the development of a simple method based on simulation aiming at extracting the degradation ratio according to the stress conditions and duration without a complete simulation of the tested circuit; thirdly, the integration of technological process dispersion which adds a non negligible uncertainty to the prediction of the evolution of the EME ; finally, validating the experimental results and the modeling approach on circuits designed in scaled down technologies.

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REFERENCES

[1] J. Srinivasan, S. V. Adve, P Bose, J. A. Rivers, “The impact of technology scaling on lifetime reliability”, Proceedings of the International Conference on Dependable Systems and Networks, (**2004**), pp.1-10.

[2] J. W. McPherson, “Reliability trends with advanced CMOS scaling and the implications for design”, Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), (**2007**), pp.405-412.

[3] M. White, Y. Chen, “Scaled CMOS technology reliability user’s guide”, NASA WBS 939904.01.11.10, 2008, http://nepp.nasa.gov.

[4] S. Ben Dhia, M. Ramdani, E. Sicard, Electromagnetic Compatibility of Integrated Circuits: Techniques for Low Emission and Susceptibility, New York, USA, Springer-Verlag, (**2006**).

[5] I. Montanari, A. Tacchini, M. Maini, “Impact of thermal stress on the characteristics of conducted emissions”, Proceedings of the IEEE Int. Symposium on Electromagnetic Compatibility, (**2008**), pp. 1-4.

[6] A. Boyer, A. C. Ndoye, S. Ben Dhia, L. Guillot, B. Vrignon, “Characterization of the evolution of IC emissions after accelerated aging”, IEEE Trans. on EMC, (**2009**), Vol. 51, N° 4, pp 892–900.

[7] S. Ben Dhia, A. Boyer, B. Li, A. C. Noye, “Characterization of the electromagnetic modelling drifts of a nanoscale IC after accelerated life tests”, Electronic Letters, (**2010**), Vol. 46, N° 4, PP. 278-280.

[8] IEC62433-2, “Models of Integrated Circuits for EMI behavioral simulation – ICEM-CE, ICEM Conducted Emission Model”, International Electrotechnical Commission, Geneva, Switzerland, (**2006**).

[9] A. Boyer, S. Ben Dhia, C. Lemoine, B. Vrignon, “Characterizing circuit susceptibility with on-chip sensors”, Proceedings of Asia-Pacific Int. Symposium on Electromagnetic Compatibility, (**2012**), pp. 73-76.

[10] B. Li, N. Berbel, A. Boyer, S. Ben Dhia, R. Fernandez-Garcia, “Study of the impact of hot carrier injection to immunity of MOSFET to electromagnetic interferences”, Microelectronics Reliability, (**2011**), vol. 51, pp. 1557-1560.

[11] B. Li, “Study of aging effects on electromagnetic compatibility of integrated circuits”, Thesis, University of Toulouse, (**2011**).

[12] IEC 61967-4 Ed. 1.1, “Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions - 1 Ω/150 Ω direct coupling method”, International Electrotechnical Commission, Geneva, Switzerland, (**2006**).

[13] M. Swaminathan, A. Ege Engin, “Power Integrity Modeling and Design for Semiconductors and Systems”, Prentice Hall Signal Integrity Library, (**2007**).

[14] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, S. Krishnan, “A comprehensive framework for predictive modeling of negative bias temperature instability”, Proceeding of IEEE Interrnational Reliability Physics Symposium, (**2004**), pp. 273-282.

[15] J. B. Bernstein, M. Gurfinkel, X. Li, J. Walters, Y. Shapira, M. Talmor, “Electronic Circuit Reliability Modeling”, Microelectronics Reliability, (**2006**), vol. 46, pp. 1957-1979.

[16] M. V. Dunga, et al., « BSIM46.1 MOSFET Model – Suser’s Manual », (**2007**), UC Berkeley.

FIGURES AND TABLES

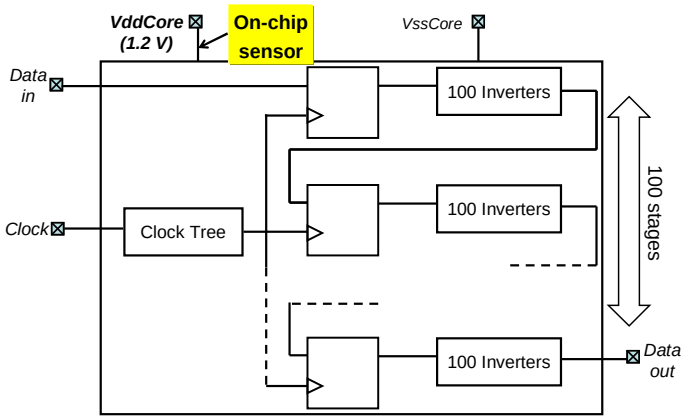


Figure 1. Structure of the circuit under test.

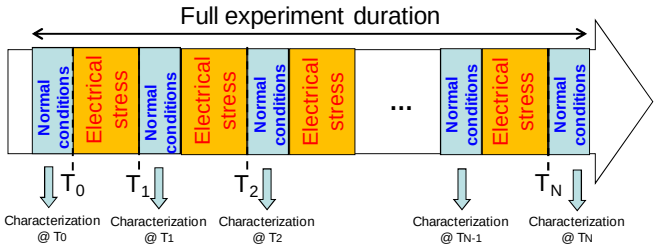


Figure 2. Principle of the characterization of aging effect on power integrity and conducted emission: measurement-stress-measurement flow.

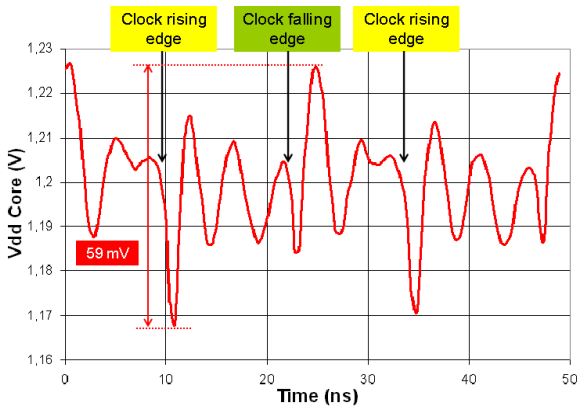


Figure 3. Measurement of the power supply voltage bounce of the digital core.

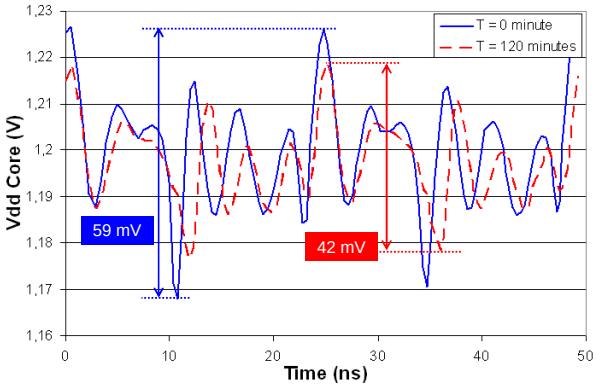


Figure 4. Evolution of the core power supply voltage bounce after 120 minutes of 3.6 V electrical stress.

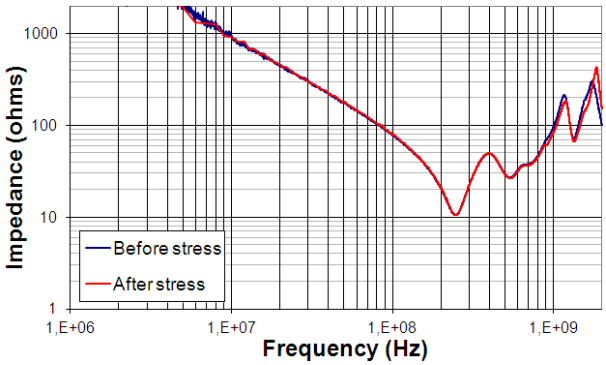


Figure 5. Measurements of the impedance of the power distribution network of the digital core before and after electrical stress.

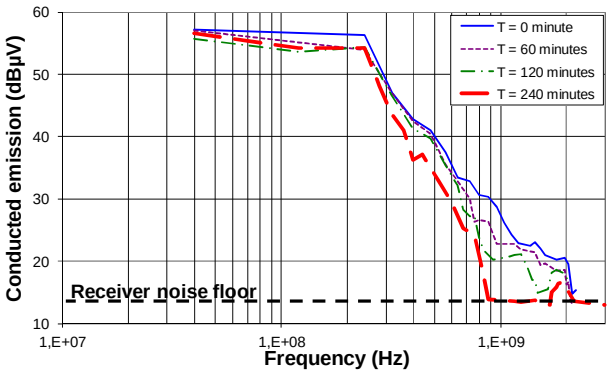


Figure 6. Evolution of the core conducted emission after 240 minutes of 3 V electrical stress.

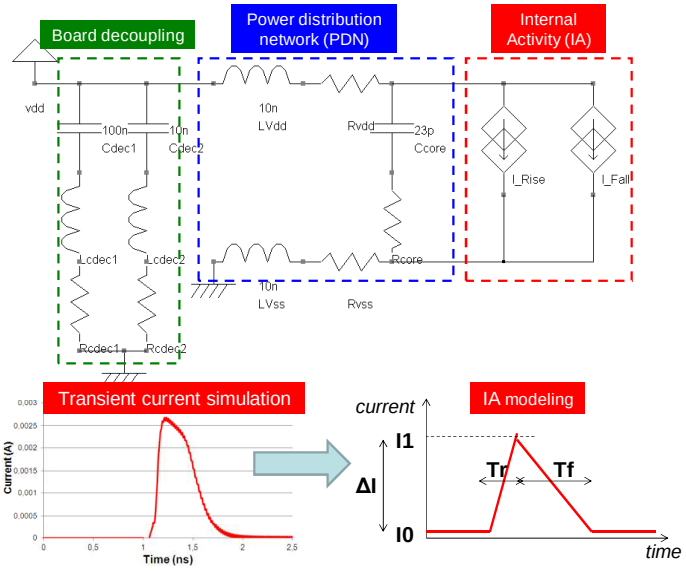


Figure 7. ICEM model of the digital core.

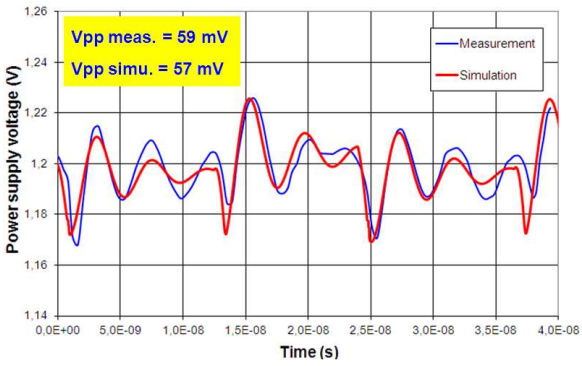


Figure 8. Comparison between measurement and simulation of the digital core power supply voltage bounce before electrical stress.

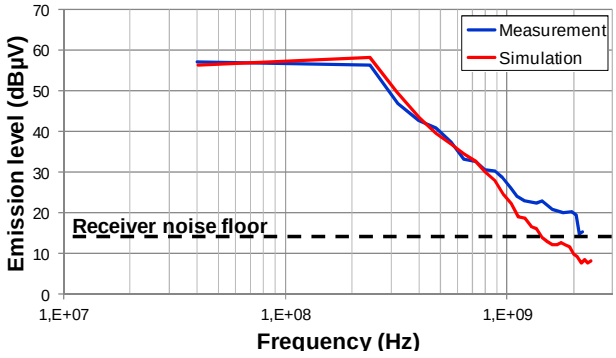


Figure 9. Comparison between the measurement and simulation of the digital core conducted emission before electrical stress.

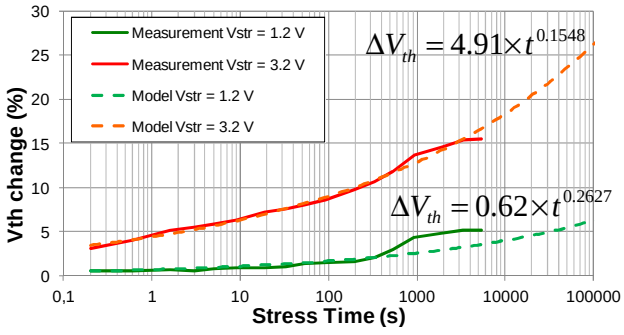


Figure 10. Measurement and modeling of VTH evolution of 90 nm low voltage PMOS device exposed to negative gate-source voltage.

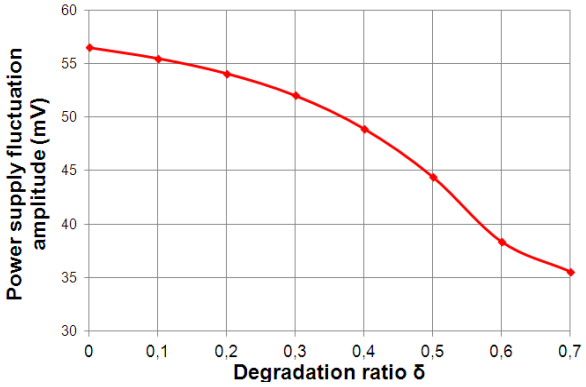


Figure 11. Simulated evolution of the peak-to-peak amplitude of the power supply voltage bounce vs. degradation ratio.

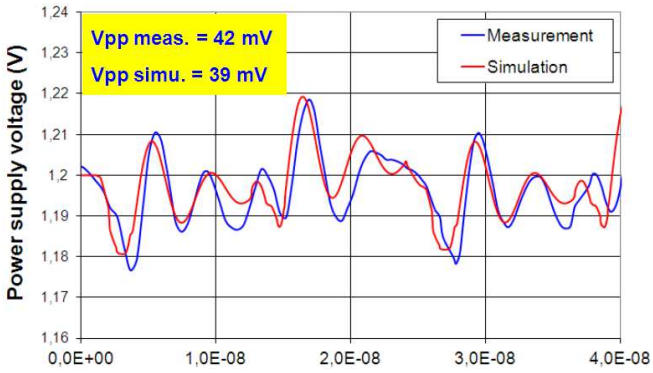


Figure 12. Comparison between simulated power supply voltage bounce after 120 minutes of 3.6 V electrical stress.

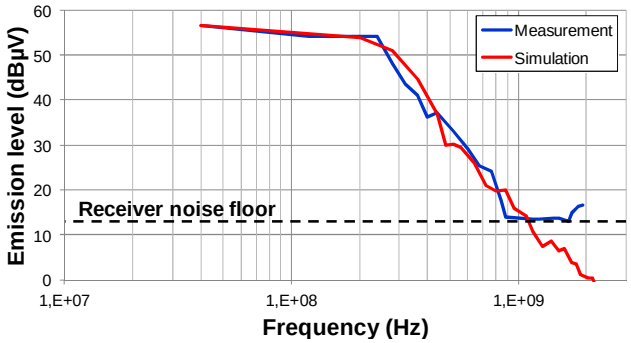


Figure 13. Comparison between the measurement and simulation of the digital core conducted emission after 120 minutes of 3.6 V electrical stress.

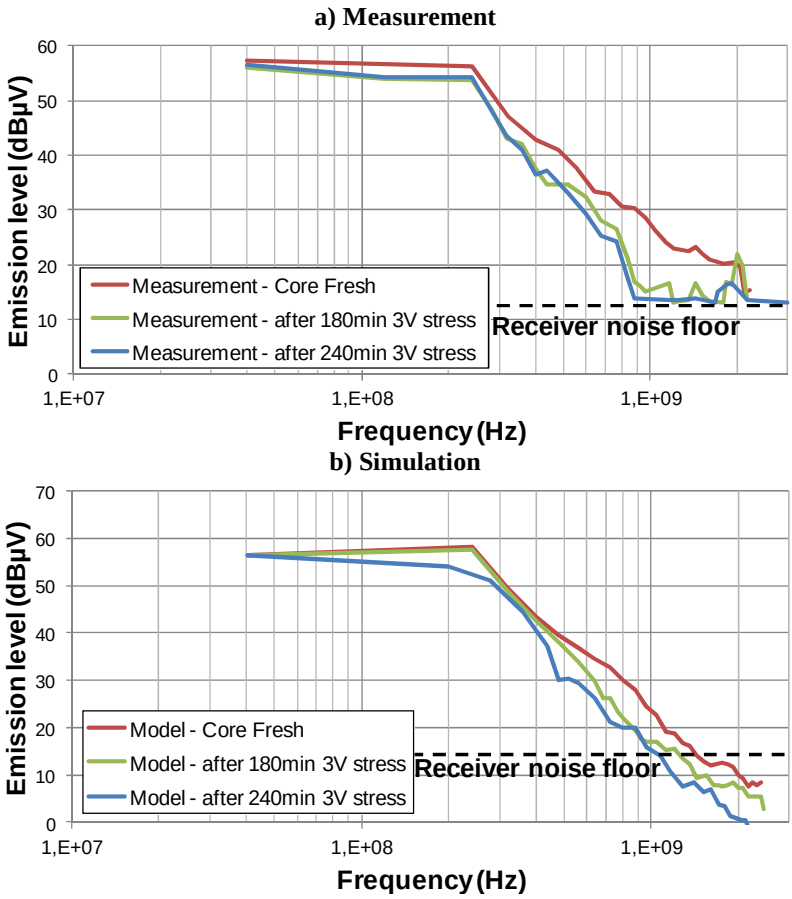


Figure 14. a) Measurement and b) simulation of the evolution of the CE spectrum of the digital core exposed to a 3 V electrical stress.

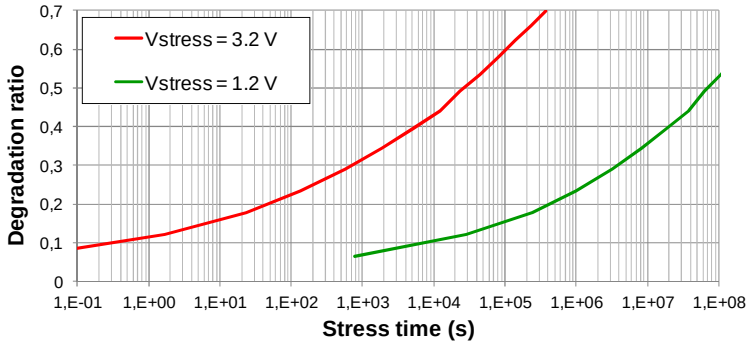


Figure 15. Simulated evolution of the degradation ratio vs. stress time.

BIOGRAPHIES

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